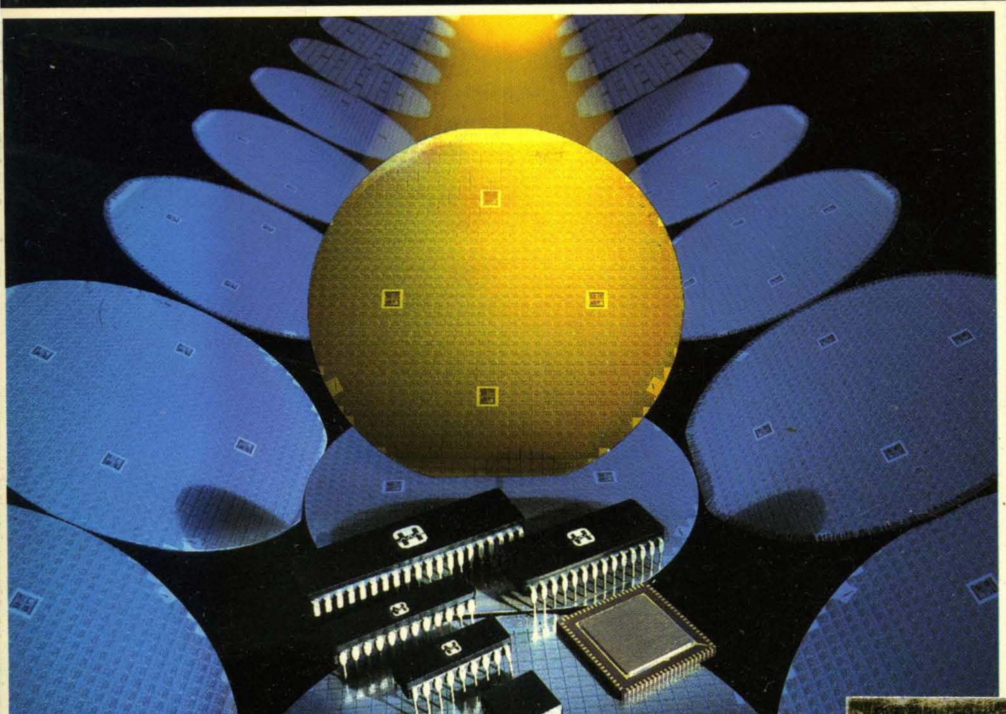
CMOS

DIGITAL DATA BOOK



HARRIS

Volume 5
$5.00

Harris Semiconductor Sector Capabilities

Harris Semiconductor, one of the top ten U.S. merchant semiconductor suppliers, is a sector of Harris Corporation — a producer of advanced information processing, communication and microelectronic products for the worldwide information technology market.

Harris Semiconductor is organized to address the standard products, custom products, and gallium arsenide semiconductor markets.

SEMICONDUCTOR PRODUCTS DIVISION

Harris Semiconductor offers a wide selection of standard analog and digital circuits through its Semiconductor Products Division:

Analog Products

Harris is a major force in analog integrated circuitry, offering a broad line of products including: analog-to-digital converters, digital-to-analog converters, sample-and-hold circuits, multiplexers, switches, voltage references, operational amplifiers, telecommunications and speech processing products, hybrid subsystems and active filters. (See complete analog product listing, page 12-2.)

Digital Products

Harris is a pioneer in developing and producing digital CMOS products including: CMOS RAMs, CMOS PROMs, CMOS microprocessors, CMOS peripherals, CMOS data communications products, and a full line of 80C86/88 microprocessors and peripherals. Semicustom circuit design problems are solved by a complete line of SSI, MSI, and LSI standard cells and programmable logic products featuring on-chip testability. (See complete digital product listing, page 1-3.)

CUSTOM INTEGRATED CIRCUITS DIVISION (CICD)

CICD is dedicated to the development and production of custom/semi-custom and specialized integrated circuits for use in such areas as tactical/strategic radiation environments and secure communications. CICD employs high performance CMOS and bipolar technologies to meet the needs of high-end major military and hi-reliability programs.

CICD is oriented to engineering and manufacturing to specific customer requirements. The division also has its own dedicated manufacturing operation and engineering, product assurance, and program manager representation to insure close customer interaction and tight control of the design and quality aspects of individual programs.

Data sheet products include devices that have a wider appeal, including those designed to operate in very severe environments. CICD's experience with radiation-hardened devices has made Harris Semiconductor the leading producer of circuits that meet a variety of Department of Defense environmental specifications. (See complete CICD product listing, page 12-8 & 12-9.)

MICROWAVE SEMICONDUCTOR DIVISION

Harris Microwave Semiconductor Division develops and manufactures gallium arsenide field effect transistors (GaAs FETs), digital integrated circuits, monolithic microwave integrated circuits, and GaAs FET microwave amplifiers. (See complete Microwave product listing, page 12-8.)

*VideoLog is a registered trademark of VideoLog Communications

Harris CMOS Digital Products

Harris Semiconductor continues to lead the way in offering advanced CMOS digital products for the most demanding system applications in this world — and beyond. Total control of system operation is now possible with Harris' static CMOS 80C86/88-based microprocessor and peripheral family. True low power Programmable Logic, the world's largest library of LSI Standard Cells, and advanced CMOS Memory and Memory modules are all available at Harris — just turn the pages for more on these and other advanced CMOS digital products.

This data book fully describes Harris Semiconductor's line of CMOS digital products by including a complete set of data sheets for product specifications; application notes with design details for specific applications of Harris products; and a description of Harris' quality and reliability program.

If you need more information on these and other Harris products, please contact the nearest Harris sales office listed in the back of this data book. Or return the reply card attached inside back cover.

HARRIS

CMOS

1986 Digital Data Book

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General Information

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GENERAL INFORMATION

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CMOS Alpha-Numeric Index

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CMOS Devices by Families

CMOS Devices by Families

Classification of Literature

CLASSIFICATION	PRODUCT STAGE	DISCLAIMERS
Preview DATA SHEET	Formative or Design	This document contains the design specifications for product under development. Specifications may be changed in any manner without notice.
Advance Information DATA SHEET	Sampling or Pre-Production	This is advanced information, and specifications are subject to change without notice.

Harris reserves the right to make changes at anytime without notice, in order to improve design and supply the best product possible.

Symbols and Abbreviations

This data sheet utilizes a new set of specification nomenclature. This new format is an IEEE and JEDEC supported standard for semiconductor memories. It is intended to clarify the symbols, abbreviations and definitions, and to make all memory data sheets consistent. We believe that, once acclimated, you will find this standardized format easy to read and use.

Electrical Parameter Abbreviations

All abbreviations use upper case letters with no subscripts. The initial symbol is one of these four characters:

V (Voltage)
I (Current)
P (Power)
C (Capacitance)

The second letter specifies input (I) or output (O), and the third letter indicates the high (H), low (L) or off (Z) state of the pin during measurements. Examples:

VIL — Input Low Voltage
IQZ — Output Leakage Current

Timing Parameter Abbreviations

All timing abbreviations use upper case characters with no subscripts. The initial character is always T and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal point specify the signal name and the signal transitions. Thus the format is:

T X X X X

Signal name from which interval is defined
Transition direction for first signal
Signal name to which interval is defined
Transition direction for second signal

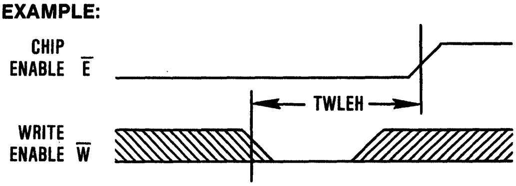
Signal Definitions:

A = Address
D = Data In
Q = Data Out
W = Write Enable
E = Chip Enable
S = Chip Select
G = Output Enable

Transition Definitions:

H = Transition to High
L = Transition to Low
V = Transition to Valid
X = Transition to Invalid or Don't Care
Z = Transition to Off (High Impedance)

EXAMPLE:

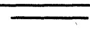
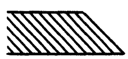
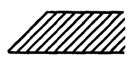
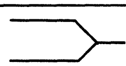


The example shows Write pulse setup time defined as TWLEH-Time from Write enable Low to chip Enable High.

Timing Limits

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address set-up time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

Waveforms

WAVEFORM SYMBOL	INPUT	OUTPUT
	Must Be Valid	Will be Valid
	Change From H to L	Will Change From H to L
	Change From L to H	Will Change From L to H
	Don't Care: Any Change Permitted	Changing: State Unknown
	—	High Impedance

CMOS

CMOS Memory

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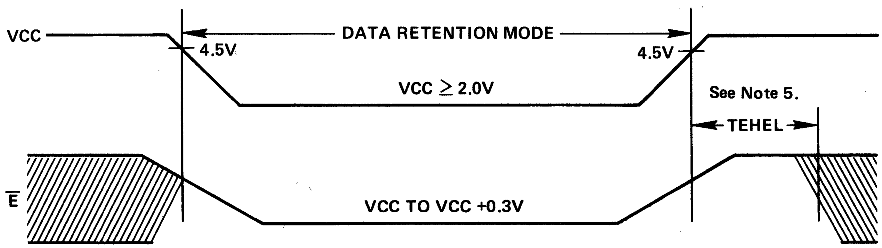
PAGE

Low Voltage Data Retention

HARRIS CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip Enable ($\overline{E}$) must be held high during data retention; within VCC to VCC +0.3V
2. On RAMs which have selects or output enables (e.g. $\overline{S}$, $\overline{G}$), one of the selects or output enables should be held in the deselected state to keep the RAM outputs high impedance, minimizing power dissipation.
3. All other inputs should be held either high (at CMOS VCC) or at ground to minimize ICCDR.
4. Inputs which are to be held high (e.g. $\overline{E}$) must be kept between VCC +0.3V and 70% of VCC during the power up and power down transitions.
5. The RAM can begin operation one TEHEL (for synchronous RAMs) and >55ns (for asynchronous RAMs) after VCC reaches the minimum operating voltage (4.5 volts).

DATA RETENTION TIMING



Industry CMOS RAM Cross Reference

HARRIS CMOS RAMs

DESCRIPTION	HARRIS	AMD	EDI	FUJ-ITSU	HIT-ACHI	IDT	MITSU-BISHI	MOT-OROLA	NAT-IONAL	NEC	OKI	RCA	SMOS	TOSH-IBA	NMOS, OTHER
1K CMOS RAMs															
1Kx1, 16 Pin Synchronous	HM-6508			8401				6508	6508 74C929	443		6508 1821		5508	2125, 4015
1Kx1, 18 Pin Synchronous	HM-6518							6518	6518 74C930						
256x4, 22 Pin Synchronous	HM-6551								6551 74C920			1822 5101		5101	2101
256x4, 18 Pin Synchronous	HM-6561														2111
4K CMOS RAMs															
4Kx1, 18 Pin Synchronous	HM-6504	92L44		8404	4315 6147			6504	6504		5104		6504	5504	2141, 2147 315D, 4104 4404
1Kx4, 18 Pin Synchronous	HM-6514	91L14 91L24		8414	4334 6148		58981	6514	6514	444	5114 5115	5114	6514	5514	2114, 2148 2149, 4045 314A
16K CMOS RAMs															
2Kx8, 24 Pin Synchronous	HM-6516								6516						
2Kx8, 24 Pin Asynchronous	HM-65162			8416	6116	6116	5117	65116	6116	446	5128	6116	2016	5517	4802, 2116 2016, 4016
16Kx1, 20 Pin Asynchronous	HM-65262			8167	6167	6167							2267 2367		2167, 8167 1400
64K CMOS RAMs															
8Kx8, 28 Pin Asynchronous	HM-65642 HM-8808A* HM-8808*	99C88	8808A 8808	8464	6264	7164 7M864 8M864	5164	6164	6164	4464		6264	2064 2264	5564 5565	
128K CMOS RAM MODULE															
16Kx8, 28 Pin Asynchronous	HM-8816H		8816H												
256K CMOS RAM MODULE															
32Kx8/16Kx16 48 Pin Module Asynchronous	HM-92560 HM-92570														

HARRIS

HM-6508

1024 x 1 CMOS RAM

Features

- **Low Standby Power .... 50µW Max.**
- **Low Operating Power .... 20mW/MHz Max.**
- **Fast Access Time .... 180nsec Max.**
- **Data Retention Voltage .... 2.0 Volts Min.**
- **TTL Compatible In/Out**
- **High Output Drive — 2 TTL Loads**
- **High Noise Immunity**
- **On Chip Address Register**
- **Wide Operating Temperature Ranges:**
  - **HM-6508-5 .... 0°C to +70°C**
  - **HM-6508-9 .... -40°C to +85°C**
  - **HM-6508-2/-8 .... -55°C to +125°C**

Description

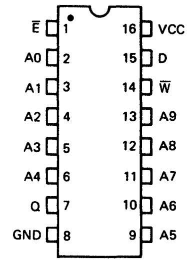
The HM-6508 is a 1024 by 1 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for address allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HM-6508 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

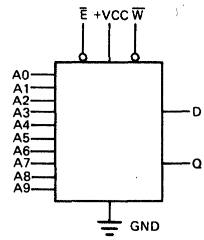
Pinout

TOP VIEW

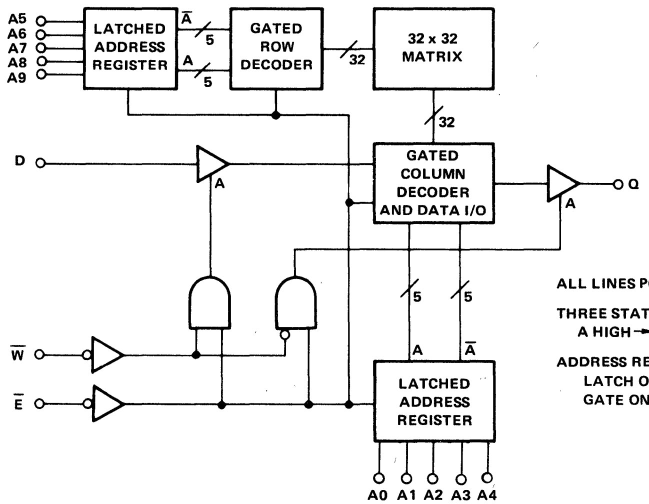


A — Address Input
Ē — Chip Enable
W̄ — Write Enable
D — Data Input
Q — Data Output

Logic Symbol



Functional Diagram



ALL LINES POSITIVE LOGIC — ACTIVE HIGH

THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE

ADDRESS REGISTER AND DECODERS:
LATCH ON FALLING EDGE OF Ē
GATE ON FALLING EDGE OF Ē

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) ....-0.3V to +8.0V
Input or Output Voltage Applied.................. (GND -0.3V) to (VCC +0.3V)
Storage Temperature..............................-65°C to +150°C

Operating Range

Operating Supply Voltage - VCC
HM-6508B-2/-8 ....4.5V to 5.5V
HM-6508B-9 .... 4.5V to 5.5V
Operating Temperature
HM-6508B-2/-8 ....-55°C to +125°C
HM-6508B-9..-40°C to +85°C

**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications ①

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	mA	Ē = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		5	μA	VCC = 2.0, IO = 0 VI = VCC or GND Ē = VCC
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	-1.0	+1.0	μA	VI = VCC or GND
	IOZ	Output Leakage Current	-1.0	+1.0	μA	VO = VCC or GND
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 3.2mA
	VOH	Output High Voltage	2.4		V	IO = -0.4mA
	CI	Input Capacitance ③		6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		180	ns	④
	TAVQV	Address Access Time		180	ns	④
	TELQX	Chip Enable Output Enable Time	20	120	ns	③④
	TWLQZ	Write Enable Output Disable Time		120	ns	③④
	TEHQZ	Chip Enable Output Disable Time		120	ns	③④
	TELEH	Chip Enable Pulse Negative Width	180		ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		ns	④
	TAVEL	Address Setup Time	0		ns	④
	TELAX	Address Hold Time	40		ns	④
	TDVWH	Data Setup Time	80		ns	④
	TWHDX	Data Hold Time	0		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	100		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	100		ns	④
	TWLWH	Write Enable Pulse Width	100		ns	④
	TELEL	Read or Write Cycle Time	280		ns	④

NOTES:
① All devices tested at worst case temperature and V_{CC}.
② Operating supply current (ICCOP) is proportional to operating frequency. Example: typical ICCOP = 1.5mA/MHz.
③ Tested at initial design and after major design changes.
④ Input rise and fall times: 20ns max. Input and output timing reference level: 1.5V. Output load: 1 TTL gate equivalent and C_L = 50 to 300pF. For C_L greater than 50pF, access time is derated 0.15ns/pF.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) .... -0.3V to +8.0V
Input or Output Voltage Applied .... (GND -0.3V) to (VCC +0.3V)
Storage Temperature .... -65°C to +150°C

Operating Range

Operating Supply Voltage - VCC
HM-6508-2/-8 .... 4.5V to 5.5V
HM-6508-9 .... 4.5V to 5.5V
Operating Temperature
HM-6508-2/-8 .... -55°C to +125°C
HM-6508-9 .... -40°C to +85°C

*CAUTION: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications ①

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	mA	E̅ = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10	μA	VCC = 2.0, IO = 0 VI = VCC or GND E̅ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	-1.0	+1.0	μA	VI = VCC or GND
	IOZ	Output Leakage Current	-1.0	+1.0	μA	VO = VCC or GND
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 3.2mA
	VOH	Output High Voltage	2.4		V	IO = -0.4mA
	CI	Input Capacitance ③		6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		250	ns	④
	TAVQV	Address Access Time		250	ns	④
	TELQX	Chip Enable Output Enable Time	20	160	ns	③④
	TWLQZ	Write Enable Output Disable Time		160	ns	③④
	TEHQZ	Chip Enable Output Disable Time		160	ns	③④
	TELEH	Chip Enable Pulse Negative Width	250		ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		ns	④
	TAVEL	Address Setup Time	0		ns	④
	TELAX	Address Hold Time	50		ns	④
	TDVWH	Data Setup Time	110		ns	④
	TWHDX	Data Hold Time	0		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	130		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	130		ns	④
	TWLWH	Write Enable Pulse Width	130		ns	④
	TELEL	Read or Write Cycle Time	350		ns	④

NOTES:
① All devices tested at worst case temperature and V_{CC}.
② Operating supply current (ICCOP) is proportional to operating frequency. Example: typical ICCOP = 1.5mA/MHz.
③ Tested at initial design and after major design changes.
④ Input rise and fall times: 20ns max. Input and output timing reference level: 1.5V. Output load: 1 TTL gate equivalent and C_L = 50 to 300pF. For C_L greater than 50pF, access time is derated 0.15ns/pF.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) ....-0.3V to +8.0V
Input or Output Voltage Applied.................. (GND -0.3V) to (VCC +0.3V)
Storage Temperature..............................-65°C to +150°C

Operating Range

Operating Supply Voltage - VCC
HM-6508-5 .... 4.5V to 5.5V
Operating Temperature
HM-6508-5 .... 0°C to +70°C

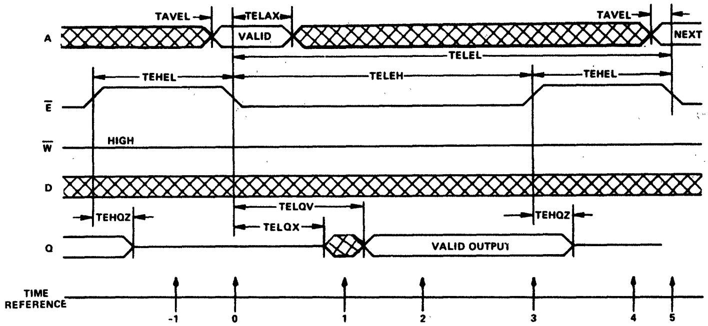
**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications ①

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	mA	Ē = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		100	μA	VCC = 2.0, IO = 0 VI = VCC or GND Ē = VCC
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	-1.0	+1.0	μA	VI = VCC or GND
	IOZ	Output Leakage Current	-1.0	+1.0	μA	VO = VCC or GND
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		V	IO = -0.2mA
	CI	Input Capacitance ③		6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300	ns	④
	TAVQV	Address Access Time		310	ns	④
	TELQX	Chip Enable Output Enable Time	20	200	ns	③④
	TWLQZ	Write Enable Output Disable Time		200	ns	③④
	TEHQZ	Chip Enable Output Disable Time		200	ns	③④
	TELEH	Chip Enable Pulse Negative Width	300		ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		ns	④
	TAVEL	Address Setup Time	10		ns	④
	TELAX	Address Hold Time	70		ns	④
	TDVWH	Data Setup Time	130		ns	④
	TWHDX	Data Hold Time	0		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	160		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	160		ns	④
	TWLWH	Write Enable Pulse Width	160		ns	④
	TELEL	Read or Write Cycle Time	450		ns	④

NOTES:
① All devices tested at worst case temperature and V_{CC}.
② Operating supply current (ICCOP) is proportional to operating frequency. Example: typical ICCOP = 1.5mA/MHz.
③ Tested at initial design and after major design changes.
④ Input rise and fall times: 20ns max. Input and output timing reference level: 1.5V. Output load: 1 TTL gate equivalent and C_L = 50 to 300pF. For C_L greater than 50pF, access time is derated 0.15ns/pF.

Read Cycle

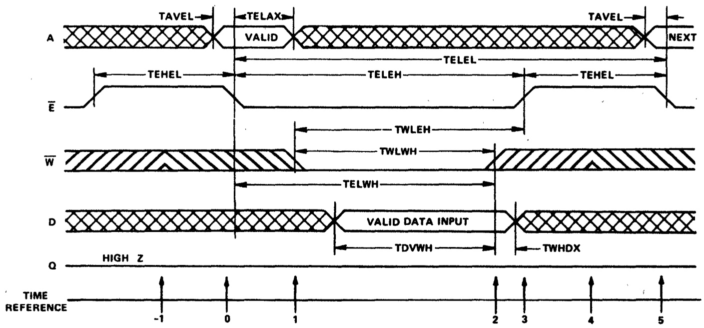


TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	A	D	OUTPUTS Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↓	H	V	X	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	X	OUTPUT ENABLED
2	L	H	X	X	V	OUTPUT VALID
3	↑	H	X	X	V	READ ACCOMPLISHED
4	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↓	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

In the HM-6508 Read Cycle, the address information is latched into the on chip registers on the falling edge of Ē (T = 0). Minimum address setup and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the data output becomes enabled; however, the data is not valid until during time (T = 2). W̄ must remain high for the read cycle. After the output data has been read, Ē may return high (T = 3). This will disable the chip and force the output buffer to a high impedance state. After the required Ē high time (TEHEL) the RAM is ready for the next memory cycle (T = 4).

Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	A	D	OUTPUTS Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↓	X	V	X	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	↓	X	X	Z	WRITE PERIOD BEGINS
2	L	↑	X	V	Z	DATA IS WRITTEN
3	↑	H	X	X	Z	WRITE COMPLETED
4	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↓	X	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The write cycle is initiated by the falling edge of $\overline{E}$ which latches the address information into the on chip registers. The write portion of the cycle is defined as both $\overline{E}$ and $\overline{W}$ being low simultaneously. $\overline{W}$ may go low anytime during the cycle provided that the write enable pulse setup time (TWLEH) is met. The write portion of the cycle is terminated by the first rising edge of either $\overline{E}$ or $\overline{W}$. Data setup and hold times must be referenced to the terminating signal.

If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may remain low until all desired locations have been written. When this method is used, data setup and hold times must be referenced to the rising edge of $\overline{E}$. By positioning the $\overline{W}$ pulse at different times within the $\overline{E}$ low time (TELEH), various types of write cycles may be performed.

If the $\overline{E}$ low time (TELEH) is greater than the $\overline{W}$ pulse (TWLWH) plus an output enable time (TELQX), a combination read write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH). The data input and data output pins may be tied together for use with a common I/O data bus structure. When using the RAM in this method allow a minimum of one output disable time (TWLQZ) after $\overline{W}$ goes low before applying input data to the bus. This will insure that the output buffers are not active.

HM-6518

1024 x 1 CMOS RAM

Features

- HM-6100 Compatible
- Low Standby Power .... 50μW Max.
- Low Operating Power .... 20mW/MHz Max.
- Fast Access Time .... 180nsec Max.
- Data Retention Voltage .... 2.0 Volts Min.
- TTL Compatible In/Out
- High Output Drive — 2 TTL Loads
- High Noise Immunity
- On Chip Address Register
- Two Chip Selects for Easy Array Expansion
- Three-State Outputs
- Wide Operating Temperature Ranges:
  - ▸ HM-6518-5 .... 0°C to +70°C
  - ▸ HM-6518-9 .... -40°C to +85°C
  - ▸ HM-6518-2/-8 .... -55°C to +125°C

Description

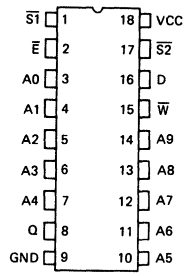
The HM-6518 is a 1024 by 1 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for addıess and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HM-6518 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

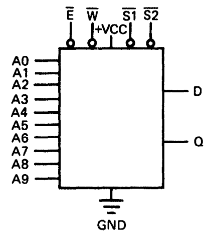
Pinout

TOP VIEW

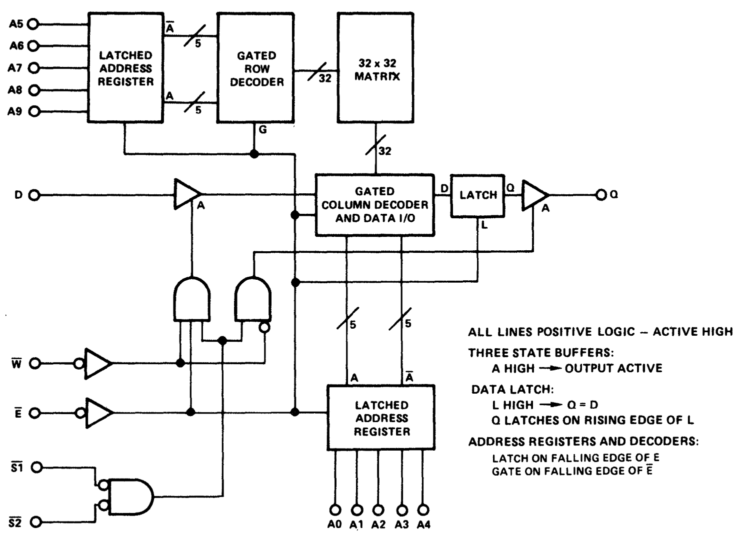


A - ADDRESS INPUT
Ē - CHIP ENABLE
S̄ - CHIP SELECT
W̄ - WRITE ENABLE
D - DATA INPUT
Q - DATA OUTPUT

Logic Symbol



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow standard IC Handling Procedures.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) .... -0.3V to +8.0V
Input or Output Voltage Applied .... (GND -0.3V) to (VCC +0.3V)
Storage Temperature .... -65°C to +150°C

Operating Range

Operating Supply Voltage - VCC
HM-6518B-2/-8 .... 4.5V to 5.5V
HM-6518B-9 .... 4.5V to 5.5V
Operating Temperature
HM-6518B-2/-8 .... -55°C to +125°C
HM-6518B-9 .... -40°C to +85°C

*CAUTION: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications ①

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10	μA	IO = 0, VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	mA	Ē = 1MHz, IO = 0, VI = VCC or GND
	ICCDR	Data Retention Supply Current		5	μA	VCC = 2.0, IO = 0, VI = VCC or GND, Ē = VCC
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	-1.0	+1.0	μA	VI = VCC or GND
	IOZ	Output Leakage Current	-1.0	+1.0	μA	VO = VCC or GND
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 3.2mA
	VOH	Output High Voltage	2.4		V	IO = -0.4mA
	CI	Input Capacitance ③		6	pF	VI = VCC or GND, f = 1MHz
	CO	Output Capacitance ③		10	pF	VO= VCC or GND, f = 1MHz
A.C.	TELQV	Chip Enable Access Time		180	ns	④
	TAVQV	Address Access Time		180	ns	④
	TSLQX	Chip Select Output Enable Time	20	120	ns	③④
	TWLQZ	Write Enable Output Disable Time		120	ns	③④
	TSHQZ	Chip Select Output Disable Time		120	ns	③④
	TELEH	Chip Enable Pulse Negative Width	180		ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		ns	④
	TAVEL	Address Setup Time	0		ns	④
	TELAX	Address Hold Time	40		ns	④
	TDVWH	Data Setup Time	80		ns	④
	TWHDX	Data Hold Time	0		ns	④
	TWLSH	Chip Select Write Pulse Setup Time	100		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	100		ns	④
	TSLWH	Chip Select Write Pulse Hold Time	100		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	100		ns	④
	TWLWH	Write Enable Pulse Width	100		ns	④
	TELEL	Read or Write Cycle Time	280		ns	④

NOTES:
① All devices tested at worst case temperature and V_{CC}.
② Operating supply current (ICCOP) is proportional to operating frequency. Example: typical ICCOP = 1.5mA/MHz.
③ Tested at initial design and after major design changes.
④ Input rise and fall times: 20ns max. Input and output timing reference level: 1.5V. Output load: 1 TTL gate equivalent and C_L = 50 to 300pF. For C_L greater than 50pF, access time is derated 0.15ns/pF.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) .... -0.3V to +8.0V
Input or Output Voltage Applied .... (GND -0.3V) to (GND +0.3V)
Storage Temperature .... -65°C to +150°C

Operating Range

Operating Supply Voltage - VCC
HM-6518-2/-8 .... 4.5V to 5.5V
HM-6518-9 .... 4.5V to 5.5V
Operating Temperature
HM-6518-2/-8 .... -55°C to +125°C
HM-6518-9 .... -40°C to +85°C

*CAUTION: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications ①

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	mA	$\overline{E}$ = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10	μA	VCC = 2.0, IO = 0 VI = VCC or GND $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	-1.0	+1.0	μA	VI = VCC or GND
	IOZ	Output Leakage Current	-1.0	+1.0	μA	VO = VCC or GND
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 3.2mA
	VOH	Output High Voltage	2.4		V	IO = -0.4mA
	CI	Input Capacitance ③		6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		250	ns	④
	TAVQV	Address Access Time		250	ns	④
	TSLQX	Chip Select Output Enable Time	20	160	ns	③ ④
	TWLQZ	Write Enable Output Disable Time		160	ns	③ ④
	TSHQZ	Chip Select Output Disable Time		160	ns	③ ④
	TELEH	Chip Enable Pulse Negative Width	250		ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		ns	④
	TAVEL	Address Setup Time	0		ns	④
	TELAX	Address Hold Time	50		ns	④
	TDVWH	Data Setup Time	110		ns	④
	TWHDX	Data Hold Time	0		ns	④
	TWLSH	Chip Select Write Pulse Setup Time	130		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	130		ns	④
	TSLWH	Chip Select Write Pulse Hold Time	130		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	130		ns	④
	TWLWH	Write Enable Pulse Width	130		ns	④
	TELEL	Read or Write Cycle Time	350		ns	④

NOTES:
① All devices tested at worst case temperature and V_{CC}.
② Operating supply current (ICCOP) is proportional to operating frequency. Example: typical ICCOP = 1.5mA/MHz.
③ Tested at initial design and after major design changes.
④ Input rise and fall times: 20ns max. Input and output timing reference level: 1.5V. Output load: 1 TTL gate equivalent and C_L = 50 to 300pF. For C_L greater than 50pF, access time is derated 0.15ns/pF.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) ....-0.3V to +8.0V
Input or Output Voltage Applied.................. (GND -0.3V) to (VCC +0.3V)
Storage Temperature..............................-65°C to +150°C

Operating Range

Operating Supply Voltage - VCC
HM-6518-5 ....4.5V to 5.5V
Operating Temperature
HM-6518-5 ....0°C to +70°C

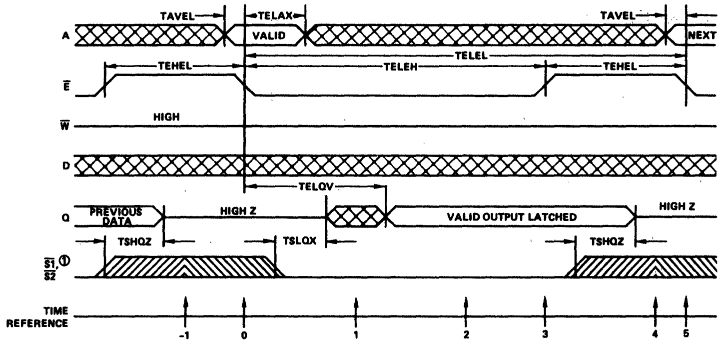
*CAUTION: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications ①

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	mA	Ē = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		100	μA	VCC = 2.0, IO = 0 VI = VCC or GND Ē = VCC
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	-1.0	+1.0	μA	VI = VCC or GND
	IOZ	Output Leakage Current	-1.0	+1.0	μA	VO = VCC or GND
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		V	IO = -0.2mA
	CI	Input Capacitance ③		6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10	pF	VO= VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300	ns	④
	TAVQV	Address Access Time		310	ns	④
	TSLQX	Chip Select Output Enable Time	20	200	ns	③④
	TWLQZ	Write Enable Output Disable Time		200	ns	③④
	TSHQZ	Chip Select Output Disable Time		200	ns	③④
	TELEH	Chip Enable Pulse Negative Width	300		ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		ns	④
	TAVEL	Address Setup Time	10		ns	④
	TELAX	Address Hold Time	50		ns	④
	TDVWH	Data Setup Time	130		ns	④
	TWHDX	Data Hold Time	0		ns	④
	TWLSH	Chip Select Write Pulse Setup Time	160		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	160		ns	④
	TSLWH	Chip Select Write Pulse Hold Time	160		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	160		ns	④
	TWLWH	Write Enable Pulse Width	160		ns	④
	TELEL	Read or Write Cycle Time	450		ns	④

NOTES:
① All devices tested at worst case temperature and V_{CC}.
② Operating supply current (ICCOP) is proportional to operating frequency. Example: typical ICCOP = 1.5mA/MHz.
③ Tested at initial design and after major design changes.
④ Input rise and fall times: 20ns max. Input and output timing reference level: 1.5V. Output load: 1 TTL gate equivalent and C_L = 50 to 300pF. For C_L greater than 50pF, access time is derated 0.15ns/pF.

Read Cycle



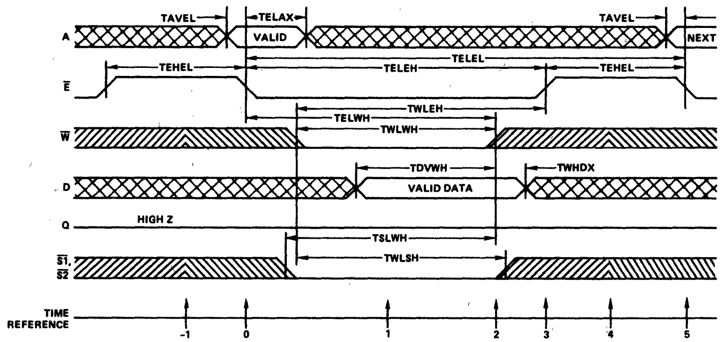
TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{S}$①	$\overline{W}$	A	D	OUTPUT Q	FUNCTION
-1	H	H	X	X	X	Z	MEMORY DISABLED
0	↓	X	H	V	X	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	H	X	X	X	OUTPUT ENABLED
2	L	L	H	X	X	V	OUTPUT VALID
3	↑	L	H	X	X	V	OUTPUT LATCHED
4	H	H	X	X	X	Z	DEVICE DISABLED, PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↓	X	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

NOTES: ① Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

In the HM-6518 read cycle the address information is latched into the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address setup and hold time requirements must be met. After the required hold time the addresses may change state without affecting device operation. In order for the output to be read $\overline{S1}$, $\overline{S2}$, and $\overline{E}$ must be low, $\overline{W}$ must be high. When $\overline{E}$ goes high the output data is latched into an on chip register. Taking either or both $\overline{S1}$ or $\overline{S2}$ high forces the output buffer to a high impedance state. The output data may be re-enabled at any time by taking $\overline{S1}$ and $\overline{S2}$ low. On the falling edge of $\overline{E}$ the data will be unlatched.

Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	$\overline{S}$①	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	X	Z	MEMORY DISABLED
0	↓	X	X	V	X	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	L	X	V	Z	WRITE MODE HAS BEGUN
2	L	↑	L	X	V	Z	DATA IS WRITTEN
3	↑	X	X	X	X	Z	WRITE COMPLETED
4	H	X	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↓	X	X	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

NOTES: ① Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

The write cycle is initiated by the falling edge of $\overline{E}$ which latches the address information into the on chip registers. The write portion of the cycle is defined as $\overline{E}$, $\overline{W}$, $\overline{S1}$, and $\overline{S2}$ being low simultaneously. $\overline{W}$ may go low anytime during the cycle provided that the write enable pulse setup time (TWLEH) is met. The write portion of the cycle is terminated by the first rising edge of either $\overline{E}$, $\overline{W}$, $\overline{S1}$ or $\overline{S2}$. Data setup and hold times must be referenced to the terminating signal.

If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may remain low until all desired locations have been written. When this method is used data setup and hold times must be referenced to the rising edge of $\overline{E}$.

By positioning the $\overline{W}$ pulse at different times within the $\overline{E}$ low time (TELEH), various types of write cycles may be performed. If the $\overline{E}$ low time (TELEH) is greater than the $\overline{W}$ pulse (TWLWH) plus an output enable time (TSLQX), a combination read-write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH).

The data input and data output pins may be tied together for use with a common I/O data bus structure. When using the RAM in this method allow a minimum of one output disable time (TWLQZ) after $\overline{W}$ goes low before applying input data to the bus. This will insure that the output buffers are not active.

HARRIS

HM-6551

256 x 4 CMOS RAM

Features

- **Low Standby Power .... 50μW Max.**
- **Low Operating Power .... 20mW/MHz Max.**
- **Fast Access Time .... 220nsec Max.**
- **Data Retention Voltage .... 2.0 Volts Min.**
- **TTL Compatible In/Out**
- **High Output Drive — 1 TTL Load**
- **Internal Latched Chip Select**
- **High Noise Immunity**
- **On Chip Address Registers**
- **Latched Outputs**
- **Three-State Outputs**
- **Wide Operating Temperature Ranges:**
  - ▸ **HM-6551-5 .... 0°C to +70°C**
  - ▸ **HM-6551-9 .... -40°C to +85°C**
  - ▸ **HM-6551-2/-8 .... -55°C to +125°C**

Description

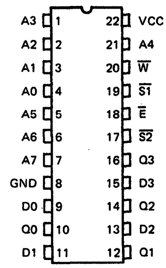
The HM-6551 is a 256 by 4 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for addresses and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HM-6551 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

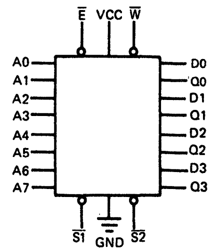
Pinout

TOP VIEW

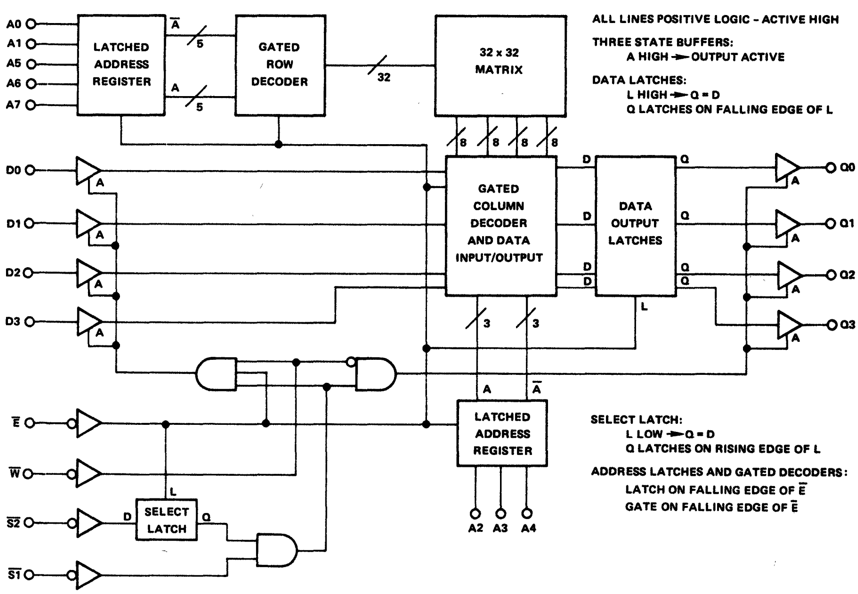


A – Address Input
Ē – Chip Enable
S̄ – Chip Select
W̄ – Write Enable
D – Data Input
Q – Data Output

Logic Symbol



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow standard IC Handling Procedures.

Absolute Maximum Ratings *

Supply Voltage - (VCC - GND)...................-0.3V to +8.0V
Input or Output Voltage Applied.................. (GND -0.3V) to (VCC +0.3V)
Storage Temperature..............................-65°C to +150°C

Operating Range

Operating Supply Voltage - VCC
HM-6551B-2/-8 .... 4.5V to 5.5V
HM-6551B-9.. 4.5V to 5.5V
Operating Temperature
HM-6551B-2/-8 ....-55°C to +125°C
HM-6551B-9..-40°C to +85°C

*CAUTION: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications ①

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10	μA	IO = 0, VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	mA	$\overline{E}$ = 1MHz, IO = 0, VI = VCC or GND, $\overline{W}$ = GND
	ICCDR	Data Retention Supply Current		10	μA	VCC = 2.0, IO = 0, VI = VCC or GND, $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	-1.0	+1.0	μA	V1 = VCC or GND
	IOZ	Output Leakage Current	-1.0	+1.0	μA	V0 = VCC or GND
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		V	IO = -0.4mA
	CI	Input Capacitance ③		6	pF	VI = VCC or GND, f = 1MHz
	CO	Output Capacitance ③		10	pF	VO= VCC or GND, f = 1MHz
A.C.	TELQV	Chip Enable Access Time		220	ns	④
	TAVQV	Address Access Time		220	ns	④
	TS1LQX	Chip Select 1 Output Enable Time	20	130	ns	③④
	TWLQZ	Write Enable Output Disable Time		130	ns	③④
	TS1HQZ	Chip Select 1 Output Disable Time		130	ns	③④
	TELEH	Chip Enable Pulse Negative Width	220		ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		ns	④
	TAVEL	Address Setup Time	0		ns	④
	TS2LEL	Chip Select 2 Setup Time	0		ns	④
	TELAX	Address Hold Time	40		ns	④
	TELS2X	Chip Select 2 Hold Time	40		ns	④
	TDVWH	Data Setup Time	100		ns	④
	TWHDX	Data Hold Time	0		ns	④
	TWLS1H	Chip Select 1 Write Pulse Setup Time	120		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	120		ns	④
	TS1LWH	Chip Select 1 Write Pulse Hold Time	120		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	120		ns	④
	TWLWH	Write Enable Pulse Width	120		ns	④
	TELEL	Read or Write Cycle Time	320		ns	④

NOTES:
① All devices tested at worst case temperature and V_{CC}.
② Operating supply current (ICCOP) is proportional to operating frequency. Example: typical ICCOP = 1.5mA/MHz.
③ Tested at initial design and after major design changes.
④ Input rise and fall times: 20ns max. Input and output timing reference level: 1.5V. Output load: 1 TTL gate equivalent and C_L = 50 to 300pF. For C_L greater than 50pF, access time is derated 0.15ns/pF.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) ....-0.3V to +8.0V
Input or Output Voltage Applied.................. (GND -0.3V) to (VCC +0.3V)
Storage Temperature..............................-65°C to +150°C

Operating Range

Operating Supply Voltage - VCC
HM-6551-2/-8.. 4.5V to 5.5V
HM-6551-9 .... 4.5V to 5.5V
Operating Temperature
HM-6551-2/-8......................................-55°C to +125°C
HM-6551-9 ....-40°C to +85°C

**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications ①

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	mA	$\overline{E}$ = 1MHz, IO = 0 VI = VCC or GND $\overline{W}$ = GND
	ICCDR	Data Retention Supply Current		10	μA	VCC = 2.0, IO = 0 VI = VCC or GND $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	-1.0	+1.0	μA	VI = VCC or GND
	IOZ	Output Leakage Current	-1.0	+1.0	μA	VO = VCC or GND
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		V	IO = -0.4mA
	CI	Input Capacitance ③		6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10	pF	VO= VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300	ns	④
	TAVQV	Address Access Time		300	ns	④
	TS1LQX	Chip Select 1 Output Enable Time	20	150	ns	③④
	TWLQZ	Write Enable Output Disable Time		150	ns	③④
	TS1HQZ	Chip Select 1 Output Disable Time		150	ns	③④
	TELEH	Chip Enable Pulse Negative Width	300		ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		ns	④
	TAVEL	Address Setup Time	0		ns	④
	TS2LEL	Chip Select 2 Setup Time	0		ns	④
	TELAX	Address Hold Time	50		ns	④
	TELS2X	Chip Select 2 Hold Time	50		ns	④
	TDVWH	Data Setup Time	150		ns	④
	TWHDX	Data Hold Time	0		ns	④
	TWLS1H	Chip Select 1 Write Pulse Setup Time	180		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	180		ns	④
	TS1LWH	Chip Select 1 Write Pulse Hold Time	180		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	180		ns	④
	TWLWH	Write Enable Pulse Width	180		ns	④
	TELEL	Read or Write Cycle Time	400		ns	④

NOTES:
① All devices tested at worst case temperature and V_{CC}.
② Operating supply current (ICCOP) is proportional to operating frequency. Example: typical ICCOP = 1.5mA/MHz.
③ Tested at initial design and after major design changes.
④ Input rise and fall times: 20ns max. Input and output timing reference level: 1.5V. Output load: 1 TTL gate equivalent and C_L = 50 to 300pF. For C_L greater than 50pF, access time is derated 0.15ns/pF.

Absolute Maximum Ratings *

Supply Voltage - (VCC - GND) ....-0.3V to +8.0V
Input or Output Voltage Applied.................. (GND -0.3V) to (VCC +0.3V)
Storage Temperature..............................-65°C to +150°C

Operating Range

Operating Supply Voltage - VCC
HM-6551-5 ....4.5V to 5.5V
Operating Temperature
HM-6551-5 ....0°C to +70°C

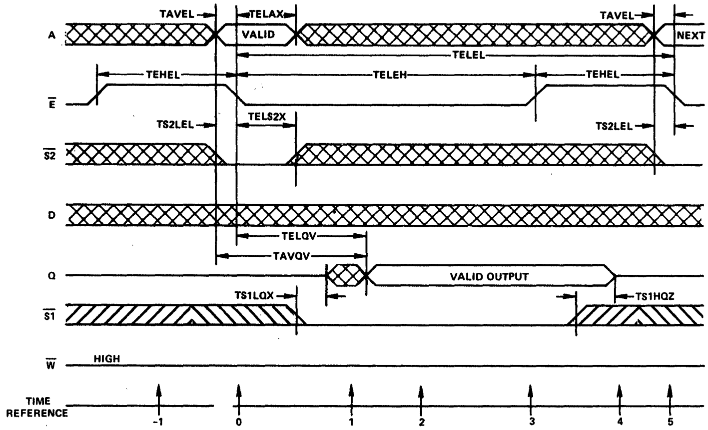
**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications ①

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100	μA	IO = 0, VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	mA	$\overline{E}$ = 1MHz, IO = 0, VI = VCC or GND, $\overline{W}$ = GND
	ICCDR	Data Retention Supply Current		100	μA	VCC = 2.0, IO = 0, VI = VCC or GND, $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	-1.0	+1.0	μA	VI = VCC or GND
	IOZ	Output Leakage Current	-1.0	+1.0	μA	VO = VCC or GND
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		V	IO = -0.2mA
	CI	Input Capacitance ③		6	pF	VI = VCC or GND, f = 1MHz
	CO	Output Capacitance ③		10	pF	VO= VCC or GND, f = 1MHz
A.C.	TELQV	Chip Enable Access Time		350	ns	④
	TAVQV	Address Access Time		360	ns	④
	TS1LQX	Chip Select 1 Output Enable Time	20	180	ns	③④
	TWLQZ	Write Enable Output Disable Time		180	ns	③④
	TS1HQZ	Chip Select 1 Output Disable Time		180	ns	③④
	TELEH	Chip Enable Pulse Negative Width	350		ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		ns	④
	TAVEL	Address Setup Time	10		ns	④
	TS2LEL	Chip Select 2 Setup Time	10		ns	④
	TELAX	Address Hold Time	70		ns	④
	TELS2X	Chip Select 2 Hold Time	70		ns	④
	TDVWH	Data Setup Time	170		ns	④
	TWHDX	Data Hold Time	0		ns	④
	TWLS1H	Chip Select 1 Write Pulse Setup Time	210		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	210		ns	④
	TS1LWH	Chip Select 1 Write Pulse Hold Time	210		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	210		ns	④
	TWLWH	Write Enable Pulse Width	210		ns	④
	TELEL	Read or Write Cycle Time	500		ns	④

NOTES:
① All devices tested at worst case temperature and V_{CC}.
② Operating supply current (ICCOP) is proportional to operating frequency. Example: typical ICCOP = 1.5mA/MHz.
③ Tested at initial design and after major design changes.
④ Input rise and fall times: 20ns max. Input and output timing reference level: 1.5V. Output load: 1 TTL gate equivalent and C_L = 50 to 300pF. For C_L greater than 50pF, access time is derated 0.15ns/pF.

Read Cycle



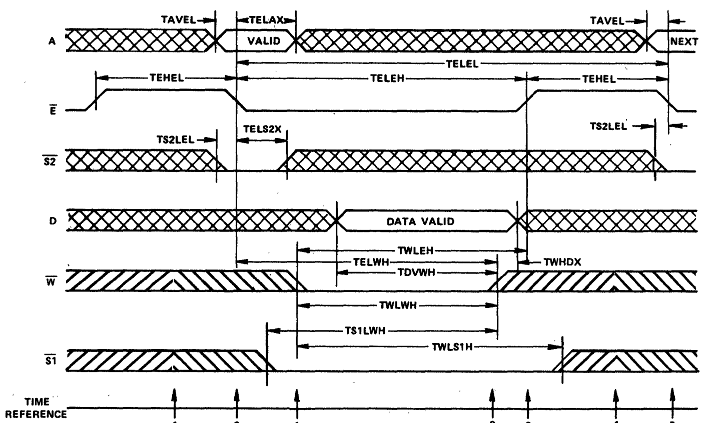
TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{S1}$	$\overline{S2}$	$\overline{W}$	A	D	OUTPUTS Q	FUNCTION
-1	H	H	X	X	X	X	Z	MEMORY DISABLED
0	↘	X	L	H	V	X	Z	ADDRESSES AND $\overline{S2}$ ARE LATCHED, CYCLE BEGINS
1	L	L	X	H	X	X	X	OUTPUT ENABLED BUT UNDEFINED
2	L	L	X	H	X	X	V	DATA OUTPUT VALID
3	↗	L	X	H	X	X	V	OUTPUTS LATCHED, VALID DATA, $\overline{S2}$ UNLATCHES
4	H	H	X	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	L	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The HM-6551 Read Cycle is initiated by the falling edge of $\overline{E}$. This signal latches the input address word and $\overline{S2}$ into on chip registers providing that minimum setup and hold times are met. After the required hold time, these inputs may change state without affecting device operation. $\overline{S2}$ acts as a high order address and simplifies decoding. For the output to be read, $\overline{E}$, $\overline{S1}$ must be low and $\overline{W}$ must be high. $\overline{S2}$ must have been latched low on the falling edge of $\overline{E}$. The output data will be valid at access time (TELQV).

The HM-6551 has output data latches that are controlled by $\overline{E}$. On the rising edge of $\overline{E}$ the present data is latched and remains in that state until $\overline{E}$ falls. Also on the rising edge of $\overline{E}$, $\overline{S2}$ unlatches and controls the outputs along with $\overline{S1}$. Either or both $\overline{S1}$ or $\overline{S2}$ may be used to force the output buffers into a high impedance state.

Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS E	S1	S2	W	A	D	OUTPUTS Q	FUNCTION
-1	H	H	X	X	X	X	Z	MEMORY DISABLED
0	↓	X	L	X	V	X	Z	CYCLE BEGINS, ADDRESSES AND $\overline{S2}$ ARE LATCHED
1	L	L	X	↓	X	X	Z	WRITE PERIOD BEGINS
2	L	L	X	↑	X	V	Z	DATA IN IS WRITTEN
3	↑	X	X	H	X	X	Z	WRITE IS COMPLETED
4	H	H	X	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↓	X	L	X	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

In the Write Cycle the falling edge of $\overline{E}$ latches the addresses and $\overline{S2}$ into on chip registers. $\overline{S2}$ must be latched in the low state to enable the device. The write portion of the cycle is defined as $\overline{E}$, $\overline{W}$, $\overline{S1}$ being low and $\overline{S2}$ being latched low simultaneously. The $\overline{W}$ line may go low at any time during the cycle providing that the write pulse setup times (TWLEH and TWLS1H) are met. The write portion of the cycle is terminated on the first rising edge of either $\overline{E}$, $\overline{W}$, or $\overline{S1}$.

If a series of consecutive write cycles are to be executed, the $\overline{W}$ line may be held low until all desired locations have been written. If this method is used, data setup and hold times must be referenced to the first rising edge of $\overline{E}$ or $\overline{S1}$. By positioning the write pulse at different times within the $\overline{E}$ and $\overline{S1}$ low time (TELEH) various types of write cycles may be performed. If the $\overline{S1}$ low time (TS1LS1H) is greater than the $\overline{W}$ pulse plus an output enable time (TS1LQX), a combination read-write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH).

The HM-6551 may be used on a common I/O bus structure by tying the input and output pins together. The multiplexing is accomplished internally by the $\overline{W}$ line. In the write cycle, when $\overline{W}$ goes low, the output buffers are forced to a high impedance state. One output disable time delay (TWLQZ) must be allowed before applying input data to the bus.

HARRIS

HM-6561

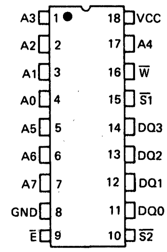
256 x 4 CMOS RAM

Features

- HM-6100 Compatible
- Low Standby Power .... 50μW Max.
- Low Operating Power .... 20mW/MHz Max.
- Fast Access Time .... 220nsec Max.
- Data Retention Voltage .... 2.0 Volts Min.
- TTL Compatible In/Out
- High Output Drive — 1 TTL Load
- On Chip Address Registers
- Common Data In/Out
- Three State Outputs
- Easy Microprocessor Interfacing
- Wide Operating Temperature Ranges:
  - HM-6561-5 .... 0°C to +70°C
  - HM-6561-9 .... -40°C to +85°C
  - HM-6561-2/-8 .... -55°C to +125°C

Pinout

TOP VIEW



A — Address Input
E̅ — Chip Enable
S̅ — Chip Select
W̅ — Write Enable
DQ — Data In/Out

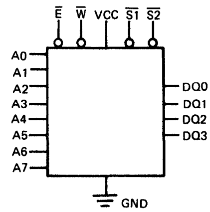
Description

The HM-6561 is a 256 by 4 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

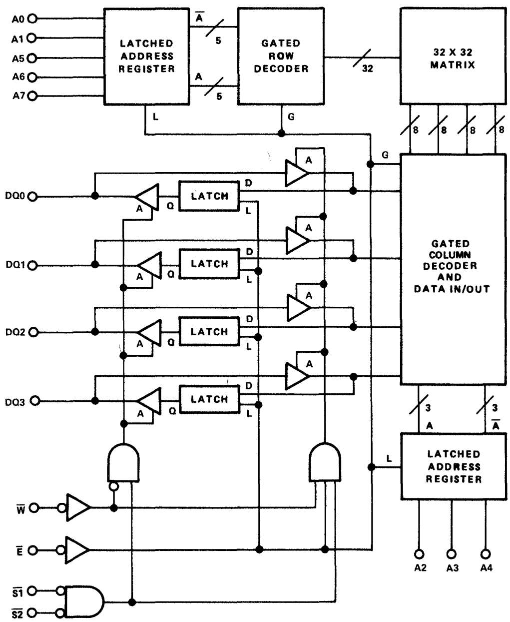
On chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays. The data inputs and outputs are multiplexed internally for common I/O bus compatibility.

The HM-6561 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

Logic Symbol



Functional Diagram



ALL LINES POSITIVE LOGIC - ACTIVE HIGH

THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE

DATA LATCHES:
L HIGH → Q = D
Q LATCHES ON FALLING EDGE OF L

ADDRESS LATCHES AND GATED DECODERS:
LATCH ON FALLING EDGE OF E̅
GATE ON FALLING EDGE OF E̅

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) ....-0.3V to +8.0V
Input or Output Voltage Applied.................. (GND -0.3V) to (VCC +0.3V)
Storage Temperature..............................-65°C to +150°C

Operating Range

Operating Supply Voltage - VCC
HM-6561B-2/-8 .... 4.5V to 5.5V
HM-6561B-9 .... 4.5V to 5.5V
Operating Temperature
HM-6561B-2/-8 .... -55°C to +125°C
HM-6561B-9 .... -40°C to +85°C

**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications ①

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10	μA	IO = 0, VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	mA	$\overline{E}$ = 1MHz, IO = 0, VI = VCC or GND, $\overline{W}$ = GND
	ICCDR	Data Retention Supply Current		10	μA	VCC = 2.0, IO = 0, VI = VCC or GND, $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	-1.0	+1.0	μA	VI = VCC or GND
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	μA	VIO = VCC or GND
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		V	IO = -0.4mA
	CI	Input Capacitance ③		6	pF	VI = VCC or GND, f = 1MHz
	CIO	Input/Output Capacitance ③		10	pF	VIO = VCC or GND, f = 1MHz
A.C.	TELQV	Chip Enable Access Time		220	ns	④
	TAVQV	Address Access Time		220	ns	④
	TSLQX	Chip Select Output Enable Time	20	120	ns	③④
	TSHQZ	Chip Select Output Disable Time		120	ns	③④
	TELEH	Chip Enable Pulse Negative Width	220		ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		ns	④
	TAVEL	Address Setup Time	0		ns	④
	TELAX	Address Hold Time	40		ns	④
	TDVWH	Data Setup Time	100		ns	④
	TWHDX	Data Hold Time	0		ns	④
	TWLDV	Write Data Delay Time	20		ns	④
	TWLSH	Chip Select Write Pulse Setup Time	120		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	120		ns	④
	TSLWH	Chip Select Write Pulse Hold Time	120		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	120		ns	④
	TWLWH	Write Enable Pulse Width	120		ns	④
	TWLSL	Early Output High Z Time	0		ns	④
	TSHWH	Late Output High Z Time	0		ns	④
	TELEL	Read or Write Cycle Time	320		ns	④

NOTES:
① All devices tested at worst case temperature and V_{CC}.
② Operating supply current (ICCOP) is proportional to operating frequency. Example: typical ICCOP = 1.5mA/MHz.
③ Tested at initial design and after major design changes.
④ Input rise and fall times: 20ns max. Input and output timing reference level: 1.5V. Output load: 1 TTL gate equivalent and C_L = 50 to 300pF. For C_L greater than 50pF, access time is derated 0.15ns/pF.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) .... -0.3V to +8.0V
Input or Output Voltage Applied .... (GND -0.3V) to (VCC +0.3V)
Storage Temperature .... -65°C to +150°C

Operating Range

Operating Supply Voltage - VCC
HM-6561-2/-8 .... 4.5V to 5.5V
HM-6561-9 .... 4.5V to 5.5V
Operating Temperature
HM-6561-2/-8 .... -55°C to +125°C
HM-6561-9 .... -40°C to +85°C

**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications ①

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10	μA	IO = 0, VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	mA	$\overline{E}$ = 1MHz, IO = 0, VI = VCC or GND
	ICCDR	Data Retention Supply Current		10	μA	$\overline{W}$ = GND, VCC = 2.0, IO = 0, VI = VCC or GND, $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	-1.0	+1.0	μA	VI = VCC or GND
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	μA	VIO = VCC or GND
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		V	IO = -0.4mA
	CI	Input Capacitance ③		6	pF	VI = VCC or GND, f = 1MHz
	CIO	Input/Output Capacitance ③		10	pF	VIO = VCC or GND, f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300	ns	④
	TAVQV	Address Access Time		300	ns	④
	TSLQX	Chip Select Output Enable Time	20	150	ns	③④
	TSHQZ	Chip Select Output Disable Time		150	ns	③④
	TELEH	Chip Enable Pulse Negative Width	300		ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		ns	④
	TAVEL	Address Setup Time	0		ns	④
	TELAX	Address Hold Time	50		ns	④
	TDVWH	Data Setup Time	150		ns	④
	TWHDX	Data Hold Time	0		ns	④
	TWLDV	Write Data Delay Time	30		ns	④
	TWLSH	Chip Select Write Pulse Setup Time	180		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	180		ns	④
	TSLWH	Chip Select Write Pulse Hold Time	180		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	180		ns	④
	TWLWH	Write Enable Pulse Width	180		ns	④
	TWLSL	Early Output High Z Time	0		ns	④
	TSHWH	Late Output High Z Time	0		ns	④
	TELEL	Read or Write Cycle Time	400		ns	④

NOTES:
① All devices tested at worst case temperature and V_{CC}.
② Operating supply current (ICCOP) is proportional to operating frequency. Example: typical ICCOP = 1.5mA/MHz.
③ Tested at initial design and after major design changes.
④ Input rise and fall times: 20ns max. Input and output timing reference level: 1.5V. Output load: 1 TTL gate equivalent and C_L = 50 to 300pF. For C_L greater than 50pF, access time is derated 0.15ns/pF.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) ....-0.3V to +8.0V
Input or Output Voltage Applied.................. (GND -0.3V) to (VCC +0.3V)
Storage Temperature..............................-65°C to +150°C

Operating Range

Operating Supply Voltage - VCC
HM-6561-5 .... 4.5V to 5.5V
Operating Temperature
HM-6561-5 .... 0°C to +70°C

*CAUTION: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications ①

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4	mA	Ē = 1MHz, IO = 0 VI = VCC or GND W̄ = GND
	ICCDR	Data Retention Supply Current		100	μA	VCC = 2.0, IO = 0 VI = VCC or GND Ē = VCC
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	-1.0	+1.0	μA	VI = VCC or GND
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	μA	VIO = VCC or GND
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		V	IO = -0.2mA
	CI	Input Capacitance ③		6	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance ③		10	pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		350	ns	④
	TAVQV	Address Access Time		360	ns	④
	TSLQX	Chip Select Output Enable Time	20	180	ns	③④
	TSHQZ	Chip Select Output Disable Time		180	ns	③④
	TELEH	Chip Enable Pulse Negative Width	350		ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		ns	④
	TAVEL	Address Setup Time	10		ns	④
	TELAX	Address Hold Time	70		ns	④
	TDVWH	Data Setup Time	170		ns	④
	TWHDX	Data Hold Time	0		ns	④
	TWLDV	Write Data Delay Time	40		ns	④
	TWLSH	Chip Select Write Pulse Setup Time	210		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	210		ns	④
	TSLWH	Chip Select Write Pulse Hold Time	210		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	210		ns	④
	TWLWH	Write Enable Pulse Width	210		ns	④
	TWLSL	Early Output High Z Time	0		ns	④
	TSHWH	Late Output High Z Time	0		ns	④
	TELEL	Read or Write Cycle Time	500		ns	④

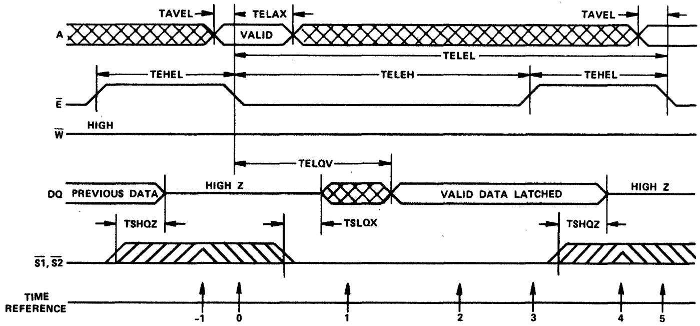
NOTES: ① All devices tested at worst case temperature and V_{CC}.

② Operating supply current (ICCOP) is proportional to operating frequency. Example: typical ICCOP = 1.5mA/MHz.

③ Tested at initial design and after major design changes.

④ Input rise and fall times: 20ns max. Input and output timing reference level: 1.5V. Output load: 1 TTL gate equivalent and C_L = 50 to 300pF. For C_L greater than 50pF, access time is derated 0.15ns/pF.

Read Cycle



TRUTH TABLE

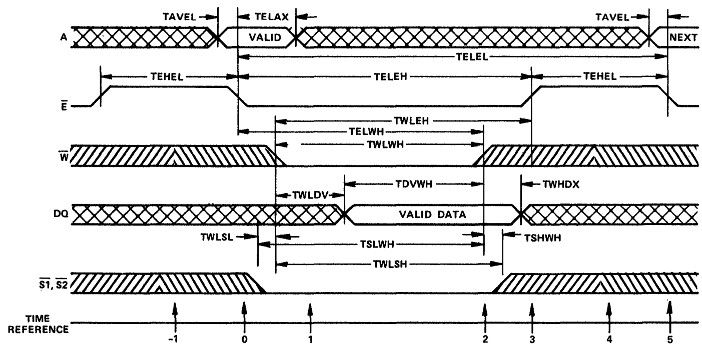
TIME REFERENCE	INPUTS $\overline{E}$	$\overline{S1}$	$\overline{W}$	A	OUTPUT DQ	FUNCTION
-1	H	H	X	X	Z	MEMORY DISABLED
0	↓	X	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	H	X	X	OUTPUT ENABLED
2	L	L	H	X	V	OUTPUT VALID
3	↑	L	H	X	V	OUTPUT LATCHED
4	H	H	X	X	Z	DEVICE DISABLED, PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↓	X	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

NOTES: 1) Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

The HM-6561 Read Cycle is initiated on the falling edge of $\overline{E}$. This signal latches the input address word into on chip registers. Minimum address setup and hold times must be met. After the required hold time, the address lines may change state without affecting device operation. In order to read the output data $\overline{E}$, $\overline{S1}$ and $\overline{S2}$ must be low and $\overline{W}$ must be high. The output data will be valid at access time (TELQV).

The HM-6561 has output data latches that are controlled by $\overline{E}$. On the rising edge of $\overline{E}$ the present data is latched and remains latched until $\overline{E}$ falls. Either or both $\overline{S1}$ or $\overline{S2}$ may be used to force the output buffers into a high impedance state.

Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{S1}$	$\overline{W}$	A	DQ	FUNCTION
-1	H	H	X	X	X	MEMORY DISABLED
0	↓	X	X	V	X	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	L	X	X	WRITE PERIOD BEGINS
2	L	L	↑	X	V	DATA IN IS WRITTEN
3	↑	X	H	X	X	WRITE IS COMPLETED
4	H	H	X	X	X	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↓	X	X	V	X	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

NOTES: 1) Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

The write cycle begins with the $\overline{E}$ falling edge latching the address. The write portion of the cycle is defined by $\overline{E}$, $\overline{S1}$, $\overline{S2}$ and $\overline{W}$ all being low simultaneously. The write portion of the cycle is terminated by the first rising edge of any control line, $\overline{E}$, $\overline{S1}$, $\overline{S2}$ or $\overline{W}$. The data setup and data hold times (TDVWH and TWHDX) must be referenced to the terminating signal. For example, if $\overline{S2}$ rises first, data setup and hold times become TDVS2H and TS2HDX; and are numerically equal to TDVWH and TWHDX.

Data input/output multiplexing is controlled by $\overline{W}$. Care must be taken to avoid data bus conflicts, where the RAM outputs become enabled when another device is driving the data inputs. The following two examples illustrate the timing required to avoid bus conflicts.

Case 1: Both $\overline{S1}$ and $\overline{S2}$ fall before $\overline{W}$ falls.

If both selects fall before $\overline{W}$ falls, the RAM outputs will become enabled. $\overline{W}$ is used to disable the outputs, so a disable time (TWLQZ = TWLDV) must pass before any other device can begin to drive the data inputs. This method of operation requires a wider write pulse, because TWLDV + TDVWH is greater than TWLWH. In this case TWLSL and TSHWH are meaningless and can be ignored.

Case 2: $\overline{W}$ falls before both $\overline{S1}$ and $\overline{S2}$ fall.

If one or both selects are high until $\overline{W}$ falls the outputs are guaranteed not to enable at the beginning of the cycle. This eliminates the concern for data bus conflicts and simplifies data input timing. Data input may be applied as early as convenient, and TWLDV is ignored. Since $\overline{W}$ is not used to disable the outputs it can be shorter than in case 1; TWLWH is the minimum write pulse. At the end of the write period, if $\overline{W}$ rises before either select the outputs will enable, reading the data just written. They will not disable until either select goes high (TSHQZ).

	IF	OBSERVE	IGNORE
Case 1	Both $\overline{S1}$ and $\overline{S2}$ = low before $\overline{W}$ = low	TWLQZ TWLDV TDVWH	TWLWH TWLSL TSHWH
Case 2	$\overline{W}$ = low before both $\overline{S1}$ and $\overline{S2}$ = low	TWLWH TDVWH TWLSL TSHWH	TWLQZ TWLDV

If a series of consecutive write cycles are to be performed, $\overline{W}$ may remain low until all desired locations are written. This is an extension of Case 2.

Read-Modify-Write cycles and Read-Write-Read cycles can be performed (extension of Case 1). In fact, data may be modified as many times as desired with $\overline{E}$ remaining low.

HARRIS

HM-6504

4096 x 1 CMOS RAM

Features

- **Low Power Standby .... 125µW Max.**
- **Low Power Operation .... 35mW/MHz Max.**
- **Extremely Low Speed-Power Product**
- **Data Retention .... @ 2.0V Min.**
- **TTL Compatible Input/Output**
- **Three-State Output**
- **Standard JEDEC Pinout**
- **Fast Access Time .... 120/200nsec Max.**
- **Wide Operating Temperature Ranges:**
  - **HM-6504-5 .... 0°C to +70°C**
  - **HM-6504-9 .... -40°C to +85°C**
  - **HM-6504-2/-8 .... -55°C to +125°C**
- **18 Pin Package for High Density**
- **On-Chip Address Register**
- **Gated Inputs—No Pull up or Pull Down Resistors Required**

Description

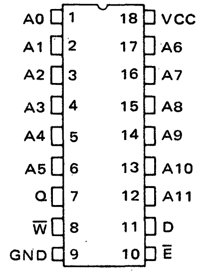
The HM-6504 is a 4096 x 1 static CMOS RAM fabricated using self-aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

On chip latches are provided for addresses, data input and data output allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance for use in expanded memory arrays. Gated inputs allow lower operating current and also eliminates the need for pull-up or pull-down resistors. The HM-6504 is a fully static RAM and may be maintained in any state for an indefinite period of time.

Data retention supply voltage and supply current are guaranteed over temperature.

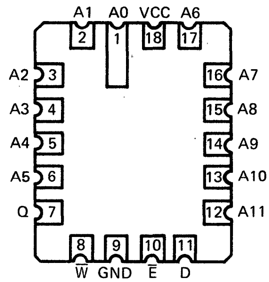
Pinouts

TOP VIEW



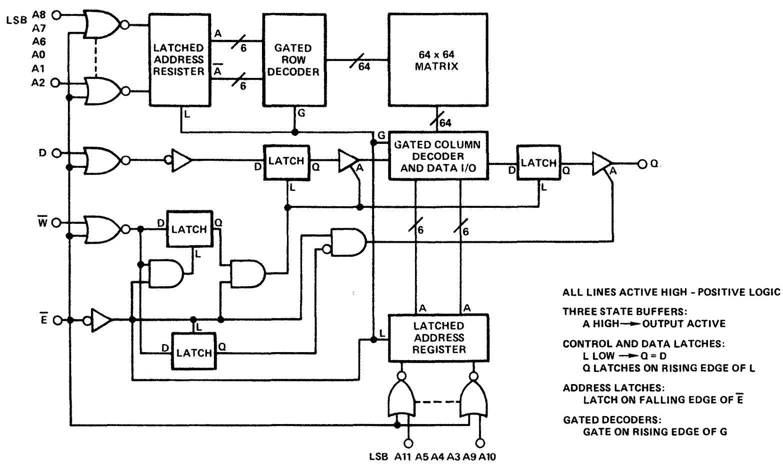
LCC

TOP VIEW



A — Address Input
Ē — Chip Enable
W̄ — Write Enable
D — Data Input
Q — Data Output

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow standard IC Handling Procedures.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) ....-0.3V to +8.0V
Input or Output Voltage Applied .... (GND -0.3V) to (VCC +0.3V)
Storage Temperature ....-65°C to +150°C

Operating Range

Operating Supply Voltage
HM-6504S-2/-8 .... 4.5V to 5.5V
Operating Temperature
HM-6504S-2/-8 ....-55°C to +125°C

**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications ①

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50	μA	IO = 0, Ē = VCC −0.3V
	ICCOP	Operating Supply Current②		7	mA	Ē = 1MHz, IO = 0, VI = GND
	ICCDR	Data Retention Supply Current		25	μA	IO = 0, VCC = 2.0V, Ē = VCC
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	-1.0	+1.0	μA	VI = VCCor GND
	IOZ	Output Leakage Current	-1.0	+1.0	μA	VO= VCC or GND
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		V	IO = -1.0mA
	CI	Input Capacitance③		8.0	pF	f = 1MHz, VI = VCC or GND
	CO	Output Capacitance③		10.0	pF	f = 1MHz, VO = VCC or GND
A.C.	TELQV	Chip Enable Access Time		120	ns	④
	TAVQV	Address Access Time		120	ns	④
	TELQX	Chip Enable Output Enable Time	10		ns	③④
	TEHQZ	Chip Enable Output Disable Time		50	ns	③④
	TELEH	Chip Enable Pulse Negative Width	120		ns	④
	TEHEL	Chip Enable Pulse Positive Width	50		ns	④
	TAVEL	Address Setup Time	0		ns	④
	TELAX	Address Hold Time	40		ns	④
	TWLWH	Write Enable Pulse Width	20		ns	④
	TWLEH	Write Enable Pulse Setup Time	70		ns	④
	TWLEL	Early Write Pulse Setup Time	0		ns	④
	TWHEL	Write Enable Read Mode Setup Time	0		ns	③④
	TELWH	Early Write Pulse Hold Time	40		ns	④
	TDVWL	Data Setup Time	0		ns	④
	TDVEL	Early Write Data Setup Time	0		ns	④
	TWLDX	Data Hold Time	25		ns	④
	TELDX	Early Write Data Hold Time	25		ns	④
	TELEL	Read or Write Cycle Time	170		ns	④

NOTES:
① All devices tested at worst case temperature and V_{CC}.
② Operating supply current (ICCOP) is proportional to operating frequency. Example: typical ICCOP = 5mA/MHz.
③ Tested at initial design and after major design changes.
④ Input rise and fall times: 5ns max. Input and output timing reference level: 1.5V. Output load: 1 TTL gate equivalent and C_L = 50 to 300pF. For C_L greater than 50pF, access time is derated 0.15ns/pF.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) ....-0.3V to +8.0V
Input or Output Voltage Applied .... (GND -0.3V) to (VCC +0.3V)
Storage Temperature ....-65°C to +150°C

Operating Range

Operating Supply Voltage
HM-6504S-9 .... 4.5V to 5.5V
Operating Temperature
HM-6504S-9 ....-40°C to +85°C

*CAUTION: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications ①

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		25	μA	IO = 0, Ē = VCC −0.3V
	ICCOP	Operating Supply Current②		7	mA	Ē = 1MHz, IO = 0, VI = GND
	ICCDR	Data Retention Supply Current		15	μA	VCC = 2.0V, IO = 0, Ē = VCC
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	-1.0	+1.0	μA	VI = VCC or GND
	IOZ	Output Leakage Current	-1.0	+1.0	μA	VO = VCC or GND
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		V	IO = -1.0mA
	CI	Input Capacitance③		8.0	pF	f = 1MHz, VI = VCC or GND
	CO	Output Capacitance③		10.0	pF	f = 1MHz, VO = VCC or GND
A.C.	TELQV	Chip Enable Access Time		120	ns	④
	TAVQV	Address Access Time		120	ns	④
	TELQX	Chip Enable Output Enable Time	10		ns	③④
	TEHQZ	Chip Enable Output Disable Time		50	ns	③④
	TELEH	Chip Enable Pulse Negative Width	120		ns	④
	TEHEL	Chip Enable Pulse Positive Width	50		ns	④
	TAVEL	Address Setup Time	0		ns	④
	TELAX	Address Hold Time	40		ns	④
	TWLWH	Write Enable Pulse Width	20		ns	④
	TWLEH	Write Enable Pulse Setup Time	70		ns	④
	TWLEL	Early Write Pulse Setup Time	0		ns	④
	TWHEL	Write Enable Read Mode Setup Time	0		ns	③④
	TELWH	Early Write Pulse Hold Time	40		ns	④
	TDVWL	Data Setup Time	0		ns	④
	TDVEL	Early Write Data Setup Time	0		ns	④
	TWLDX	Data Hold Time	25		ns	④
	TELDX	Early Write Data Hold Time	25		ns	④
	TELEL	Read or Write Cycle Time	170		ns	④

NOTES:
① All devices tested at worst case temperature and V_{CC}.
② Operating supply current (ICCOP) is proportional to operating frequency. Example: typical ICCOP = 5mA/MHz.
③ Tested at initial design and after major design changes.
④ Input rise and fall times: 5ns max. Input and output timing reference level: 1.5V. Output load: 1 TTL gate equivalent and C_L = 50 to 300pF. For C_L greater than 50pF, access time is derated 0.15ns/pF.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) ....-0.3V to +8.0V
Input or Output Voltage Applied.................. (GND -0.3V) to (VCC +0.3V)
Storage Temperature..............................-65°C to +150°C

Operating Range

Operating Supply Voltage
HM-6504B-2/-8 ....4.5V to 5.5V
Operating Temperature
HM-6504B-2/-8 .... -55°C to +125°C

***CAUTION:** *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications ①

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50	µA	IO = 0, $\overline{E}$ = VCC −0.3V
	ICCOP	Operating Supply Current②		7	mA	$\overline{E}$ = 1MHz, IO = 0, VI = GND
	ICCDR	Data Retention Supply Current		25	µA	VCC = 2.0 V, IO = 0, $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	-1.0	+1.0	µA	VI = VCC or GND
	IOZ	Output Leakage Current	-1.0	+1.0	µA	VO = VCC or GND
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		V	IO = -1.0mA
	CI	Input Capacitance③		8.0	pF	f = 1MHz, VI = VCC or GND
	CO	Output Capacitance③		10.0	pF	f = 1MHz, VO = VCC or GND
A.C.	TELQV	Chip Enable Access Time		200	ns	④
	TAVQV	Address Access Time		220	ns	④
	TELQX	Chip Enable Output Enable Time	20		ns	③④
	TEHQZ	Chip Enable Output Disable Time		80	ns	③④
	TELEH	Chip Enable Pulse Negative Width	200		ns	④
	TEHEL	Chip Enable Pulse Positive Width	90		ns	④
	TAVEL	Address Setup Time	20		ns	④
	TELAX	Address Hold Time	50		ns	④
	TWLWH	Write Enable Pulse Width	60		ns	④
	TWLEH	Write Enable Pulse Setup Time	150		ns	④
	TWLEL	Early Write Pulse Setup Time	0		ns	④
	TWHEL	Write Enable Read Mode Setup Time	0		ns	③④
	TELWH	Early Write Pulse Hold Time	60		ns	④
	TDVWL	Data Setup Time	0		ns	④
	TDVEL	Early Write Data Setup Time	0		ns	④
	TWLDX	Data Hold Time	60		ns	④
	TELDX	Early Write Data Hold Time	60		ns	④
	TELEL	Read or Write Cycle Time	290		ns	④

NOTES:
① All devices tested at worst case temperature and V_{CC}.
② Operating supply current (ICCOP) is proportional to operating frequency. Example: typical ICCOP = 5mA/MHz.
③ Tested at initial design and after major design changes.
④ Input rise and fall times: 5ns max. Input and output timing reference level: 1.5V. Output load: 1 TTL gate equivalent and C_L = 50 to 300pF. For C_L greater than 50pF, access time is derated 0.15ns/pF.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) ....-0.3V to +8.0V
Input or Output Voltage Applied .... (GND -0.3V) to (VCC +0.3V)
Storage Temperature ....-65°C to +150°C

Operating Range

Operating Supply Voltage
HM-6504B-9 ....4.5V to 5.5V
Operating Temperature
HM-6504B-9 ....-40°C to +85°C

*CAUTION: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications ①

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		25	μA	IO = 0, Ē = VCC –0.3V
	ICCOP	Operating Supply Current ②		7	mA	Ē = 1MHz, IO = 0, VI = GND
	ICCDR	Data Retention Supply Current		15	μA	VCC = 2.0V, IO = 0, Ē = VCC
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	-1.0	+1.0	μA	VI = VCC or GND
	IOZ	Output Leakage Current	-1.0	+1.0	μA	VO = VCC or GND
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		V	IO = -1.0mA
	CI	Input Capacitance③		8.0	pF	f = 1MHz, VI = VCC or GND
	CO	Output Capacitance③		10.0	pF	f = 1MHz, VO = VCC or GND
A.C.	TELQV	Chip Enable Access Time		200	ns	④
	TAVQV	Address Access Time		220	ns	④
	TELQX	Chip Enable Output Enable Time	20		ns	③④
	TEHQZ	Chip Enable Output Disable Time		80	ns	③④
	TELEH	Chip Enable Pulse Negative Width	200		ns	④
	TEHEL	Chip Enable Pulse Positive Width	90		ns	④
	TAVEL	Address Setup Time	20		ns	④
	TELAX	Address Hold Time	50		ns	④
	TWLWH	Write Enable Pulse Width	60		ns	④
	TWLEH	Write Enable Pulse Setup Time	150		ns	④
	TWLEL	Early Write Pulse Setup Time	0		ns	④
	TWHEL	Write Enable Read Mode Setup Time	0		ns	③④
	TELWH	Early Write Pulse Hold Time	60		ns	④
	TDVWL	Data Setup Time	0		ns	④
	TDVEL	Early Write Data Setup Time	0		ns	④
	TWLDX	Data Hold Time	60		ns	④
	TELDX	Early Write Data Hold Time	60		ns	④
	TELEL	Read or Write Cycle Time	290		ns	④

NOTES:
① All devices tested at worst case temperature and V_{CC}.
② Operating supply current (ICCOP) is proportional to operating frequency. Example: typical ICCOP = 5mA/MHz.
③ Tested at initial design and after major design changes.
④ Input rise and fall times: 5ns max. Input and output timing reference level: 1.5V. Output load: 1 TTL gate equivalent and C_L = 50 to 300pF. For C_L greater than 50pF, access time is derated 0.15ns/pF.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) ....-0.3V to +8.0V
Input or Output Voltage Applied.................. (GND -0.3V) to (VCC +0.3V)
Storage Temperature..............................-65°C to +150°C

Operating Range

Operating Supply Voltage
HM-6504-2/-8.. 4.5V to 5.5V
Operating Temperature
HM-6504-2/-8....................................-55°C to +125°C

**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications ①

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50	μA	IO = 0, E = VCC-0.3V
	ICCOP	Operating Supply Current②		7	mA	E = 1MHz, IO = 0, VI = GND
	ICCDR	Data Retention Supply Current		25	μA	VCC = 2.0V, IO = 0, E = VCC
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	-1.0	+1.0	μA	VI = VCC or GND
	IOZ	Output Leakage Current	-1.0	+1.0	μA	VO = VCC or GND
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		V	IO = -1.0mA
	CI	Input Capacitance③		8.0	pF	f = 1MHz, VI = VCC or GND
	CO	Output Capacitance③		10.0	pF	f = 1MHz, VO = VCC or GND
A.C.	TELQV	Chip Enable Access Time		300	ns	④
	TAVQV	Address Access Time		320	ns	④
	TELQX	Chip Enable Output Enable Time	20		ns	③④
	TEHQZ	Chip Enable Output Disable Time		100	ns	③④
	TELEH	Chip Enable Pulse Negative Width	300		ns	④
	TEHEL	Chip Enable Pulse Positive Width	120		ns	④
	TAVEL	Address Setup Time	20		ns	④
	TELAX	Address Hold Time	50		ns	④
	TWLWH	Write Enable Pulse Width	80		ns	④
	TWLEH	Write Enable Pulse Setup Time	200		ns	④
	TWLEL	Early Write Pulse Setup Time	0		ns	④
	TWHEL	Write Enable Read Mode Setup Time	0		ns	③④
	TELWH	Early Write Pulse Hold Time	80		ns	④
	TDVWL	Data Setup Time	0		ns	④
	TDVEL	Early Write Data Setup Time	0		ns	④
	TWLDX	Data Hold Time	80		ns	④
	TELDX	Early Write Data Hold Time	80		ns	④
	TELEL	Read or Write Cycle Time	420		ns	④

NOTES:
① All devices tested at worst case temperature and V_{CC}.
② Operating supply current (ICCOP) is proportional to operating frequency. Example: typical ICCOP = 5mA/MHz.
③ Tested at initial design and after major design changes.
④ Input rise and fall times: 5ns max. Input and output timing reference level: 1.5V. Output load: 1 TTL gate equivalent and C_L = 50 to 300pF. For C_L greater than 50pF, access time is derated 0.15ns/pF.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) ....-0.3V to +8.0V
Input or Output Voltage Applied.................. (GND -0.3V) to (VCC +0.3V)
Storage Temperature..............................-65°C to +150°C

Operating Range

Operating Supply Voltage
HM-6504-9 ....4.5V to 5.5V
Operating Temperature
HM-6504-9 ....-40°C to +85°C

*CAUTION: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications ①

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		25	µA	IO = 0, Ē = VCC-0.3V
	ICCOP	Operating Supply Current②		7	mA	Ē = 1MHz, IO = 0 VI = GND
	ICCDR	Data Retention Supply Current		15	µA	VCC = 2.0V, IO = 0 Ē = VCC
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	-1.0	+1.0	µA	VI = VCC or GND
	IOZ	Output Leakage Current	-1.0	+1.0	µA	VO = VCC or GND
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		V	IO = -1.0mA
	CI	Input Capacitance③		8.0	pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance③		10.0	pF	f = 1MHz VO = VCC or GND
A.C.	TELQV	Chip Enable Access Time		300	ns	④
	TAVQV	Address Access Time		320	ns	④
	TELQX	Chip Enable Output Enable Time	20		ns	③ ④
	TEHQZ	Chip Enable Output Disable Time		100	ns	③ ④
	TELEH	Chip Enable Pulse Negative Width	300		ns	④
	TEHEL	Chip Enable Pulse Positive Width	120		ns	④
	TAVEL	Address Setup Time	20		ns	④
	TELAX	Address Hold Time	50		ns	④
	TWLWH	Write Enable Pulse Width	80		ns	④
	TWLEH	Write Enable Pulse Setup Time	200		ns	④
	TWLEL	Early Write Pulse Setup Time	0		ns	④
	TWHEL	Write Enable Read Mode Setup Time	0		ns	③ ④
	TELWH	Early Write Pulse Hold Time	80		ns	④
	TDVWL	Data Setup Time	0		ns	④
	TDVEL	Early Write Data Setup Time	0		ns	④
	TWLDX	Data Hold Time	80		ns	④
	TELDX	Early Write Data Hold Time	80		ns	④
	TELEL	Read or Write Cycle Time	420		ns	④

NOTES:
① All devices tested at worst case temperature and V_{CC}.
② Operating supply current (ICCOP) is proportional to operating frequency. Example: typical ICCOP = 5mA/MHz.
③ Tested at initial design and after major design changes.
④ Input rise and fall times: 5ns max. Input and output timing reference level: 1.5V. Output load: 1 TTL gate equivalent and C_L = 50 to 300pF. For C_L greater than 50pF, access time is derated 0.15ns/pF.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) ....-0.3V to +8.0V
Input or Output Voltage Applied .... (GND -0.3V) to (VCC +0.3V)
Storage Temperature ....-65°C to +150°C

Operating Range

Operating Supply Voltage
HM-6504C-9 .... 4.5V to 5.5V
Operating Temperature
HM-6504C-9 ....-40°C to +85°C

**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications ①

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100	μA	IO = 0 $\overline{E}$ = VCC-0.3V
	ICCOP	Operating Supply Current②		7	mA	$\overline{E}$ = 1MHz, IO = 0 VI = GND
	ICCDR	Data Retention Supply Current		50	μA	VCC = 2.0V, IO = 0 $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	-1.0	+1.0	μA	VI = VCC or GND
	IOZ	Output Leakage Current	-1.0	+1.0	μA	VO = VCC or GND
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		V	IO = -1.0mA
	CI	Input Capacitance③		8.0	pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance③		10.0	pF	f = 1MHz VO = VCC or GND
A.C.	TELQV	Chip Enable Access Time		300	ns	④
	TAVQV	Address Access Time		320	ns	④
	TELQX	Chip Enable Output Enable Time	20		ns	③ ④
	TEHQZ	Chip Enable Output Disable Time		100	ns	③ ④
	TELEH	Chip Enable Pulse Negative Width	300		ns	④
	TEHEL	Chip Enable Pulse Positive Width	120		ns	④
	TAVEL	Address Setup Time	20		ns	④
	TELAX	Address Hold Time	50		ns	④
	TWLWH	Write Enable Pulse Width	80		ns	④
	TWLEH	Write Enable Pulse Setup Time	200		ns	④
	TWLEL	Early Write Pulse Setup Time	0		ns	④
	TWHEL	Write Enable Read Mode Setup Time	0		ns	③ ④
	TELWH	Early Write Pulse Hold Time	80		ns	④
	TDVWL	Data Setup Time	0		ns	④
	TDVEL	Early Write Data Setup Time	0		ns	④
	TWLDX	Data Hold Time	80		ns	④
	TELDX	Early Write Data Hold Time	80		ns	④
	TELEL	Read or Write Cycle Time	420		ns	④

NOTES:
① All devices tested at worst case temperature and V_{CC}.
② Operating supply current (ICCOP) is proportional to operating frequency. Example: typical ICCOP = 5mA/MHz.
③ Tested at initial design and after major design changes.
④ Input rise and fall times: 5ns max. Input and output timing reference level: 1.5V. Output load: 1 TTL gate equivalent and C_L = 50 to 300pF. For C_L greater than 50pF, access time is derated 0.15ns/pF.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) ....-0.3V to +8.0V
Input or Output Voltage Applied.................. (GND -0.3V) to (VCC +0.3V)
Storage Temperature...............................-65°C to +150°C

Operating Range

Operating Supply Voltage
HM-6504-5 .... 4.5V to 5.5V
Operating Temperature
HM-6504-5 ....0°C to +70°C

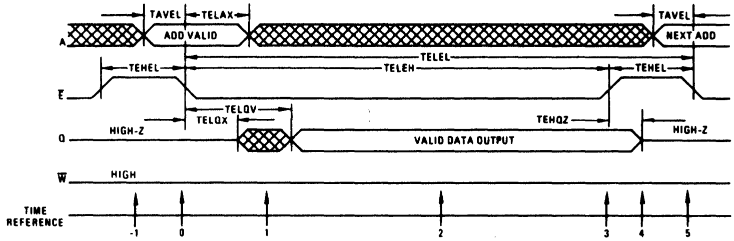
*CAUTION: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications ①

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		350	μA	IO = 0, $\overline{E}$ = VCC-0.3V
	ICCOP	Operating Supply Current②		7	mA	$\overline{E}$ = 1MHz, IO = 0, VI = GND
	ICCDR	Data Retention Supply Current		200	μA	VCC = 2.0V, IO = 0, $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	-10.0	+10.0	μA	VI = VCC or GND
	IOZ	Output Leakage Current	-10.0	+10.0	μA	VO = VCC or GND
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		V	IO = -1.0mA
	CI	Input Capacitance③		8.0	pF	f = 1MHz, VI = VCC or GND
	CO	Output Capacitance③		10.0	pF	f = 1MHz, VO = VCC or GND
A.C.	TELQV	Chip Enable Access Time		350	ns	④
	TAVQV	Address Access Time		370	ns	④
	TELQX	Chip Enable Output Enable Time	20		ns	③④
	TEHQZ	Chip Enable Output Disable Time		100	ns	③④
	TELEH	Chip Enable Pulse Negative Width	350		ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		ns	④
	TAVEL	Address Setup Time	20		ns	④
	TELAX	Address Hold Time	50		ns	④
	TWLWH	Write Enable Pulse Width	100		ns	④
	TWLEH	Write Enable Pulse Setup Time	250		ns	④
	TWLEL	Early Write Pulse Setup Time	0		ns	④
	TWHEL	Write Enable Read Mode Setup Time	0		ns	③④
	TELWH	Early Write Pulse Hold Time	100		ns	④
	TDVWL	Data Setup Time	30		ns	④
	TDVEL	Early Write Data Setup Time	30		ns	④
	TWLDX	Data Hold Time	100		ns	④
	TELDX	Early Write Data Hold Time	100		ns	④
	TELEL	Read or Write Cycle Time	500		ns	④

NOTES:
① All devices tested at worst case temperature and V_{CC}.
② Operating supply current (ICCOP) is proportional to operating frequency. Example: typical ICCOP = 5mA/MHz.
③ Tested at initial design and after major design changes.
④ Input rise and fall times: 5ns max. Input and output timing reference level: 1.5V. Output load: 1 TTL gate equivalent and C_L = 50 to 300pF. For C_L greater than 50pF, access time is derated 0.15ns/pF.

Read Cycle

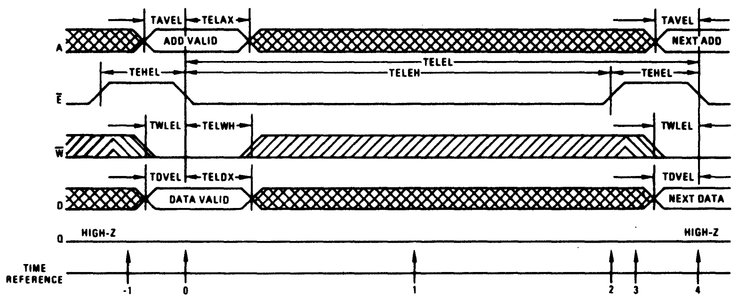


TRUTH TABLE

TIME REFERENCE	INPUTS E	W	A	OUTPUT Q	FUNCTION
-1	H	X	X	Z	MEMORY DISABLED
0	↘	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	OUTPUT ENABLED
2	L	H	X	V	OUTPUT VALID
3	↗	H	X	V	READ ACCOMPLISHED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address set up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but data is not valid until during time (T = 2). $\overline{W}$ must remain high until after time (T = 2). After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the output buffer and all inputs and ready the RAM for the next memory cycle (T = 4).

Early Write Cycle

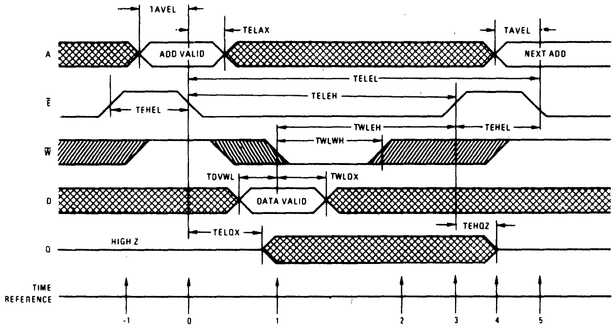


TRUTH TABLE

TIME REFERENCE	INPUTS E	W	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↘	L	V	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	X	X	X	Z	WRITE IN PROGRESS INTERNALLY
2	↗	X	X	X	Z	WRITE COMPLETED
3	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
4	↘	L	V	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The early write cycle is the only cycle where the output is guaranteed not to become active. On the falling edge of $\overline{E}$ (T = 0), the addresses, the write signal, and the data input are latched in on chip registers. The logic value of $\overline{W}$ at the time $\overline{E}$ falls determines the state of the output buffer for that cycle. Since $\overline{W}$ is low when $\overline{E}$ falls, the output buffer is latched into the high impedance state and will remain in that state until $\overline{E}$ returns high (T = 2). For this cycle, the data input is latched by $\overline{E}$ going low; therefore data set up and hold times should be referenced to $\overline{E}$. When $\overline{E}$ (T = 2) returns to the high state the output buffer and all inputs are disabled and all signals are unlatched. The device is now ready for the next cycle.

Late Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↘	H	V	X	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	↘	X	V	X	WRITE BEGINS, DATA IS LATCHED
2	L	H	X	X	X	WRITE IN PROGRESS INTERNALLY
3	↗	H	X	X	X	WRITE COMPLETED
4	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The late write cycle is a cross between the early write cycle and the read-modify-write cycle.

Recall that in the early write the output is guaranteed to remain high impedance, and in the read-modify-write the output is guaranteed valid at access time. The late write is between these two cases. With this cycle the output may become active, and may become valid data, or may remain active but undefined. Valid data is written into the RAM if data setup, data hold, write setup and write pulse widths are observed.

HM-6514

1024 x 4 CMOS RAM

Features

- Low Power Standby .... 125μW Max.
- Low Power Operation .... 35mW/MHz Max.
- Data Retention .... @ 2.0V Min.
- TTL Compatible Input/Output
- Common Data In/Out
- Three-State Outputs
- Standard JEDEC Pinout
- Fast Access Time .... 120/200nsec Max.
- Wide Operating Temperature Ranges:
  - HM-6514-5 .... 0°C to +70°C
  - HM-6514-9 .... -40°C to +85°C
  - HM-6514-2/-8 .... -55°C to +125°C
- 18 Pin Package for High Density
- On-Chip Address Register
- Gated Inputs—No Pull Up or Pull Down Resistors Required

Description

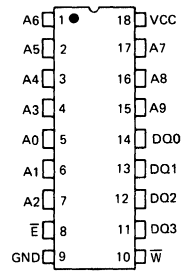
The HM-6514 is a 1024 x 4 static CMOS RAM fabricated using self aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

On-chip latches are provided for the addresses allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance state for use in expanded memory systems. Gated inputs allow low operating current and also eliminates the need for pull-up or pulldown resistors.

The HM-6514 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

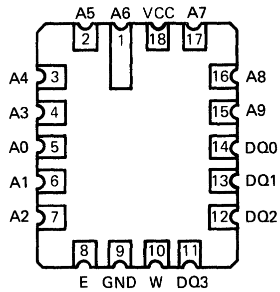
Pinouts

TOP VIEW



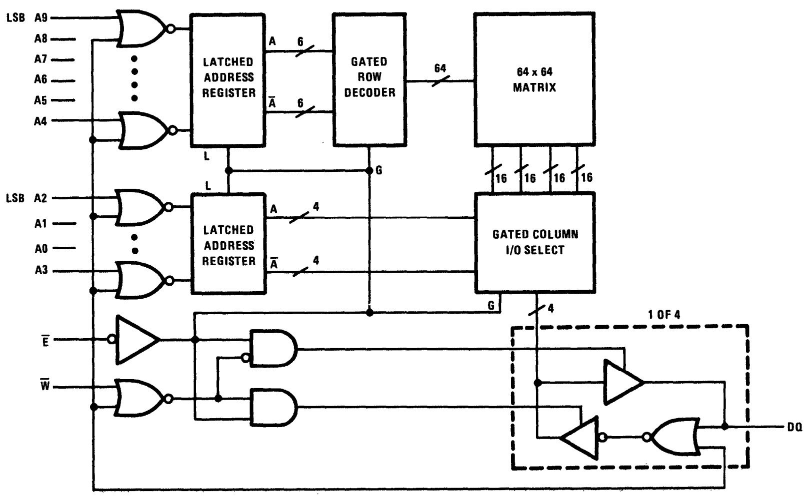
LCC

TOP VIEW



A — Address Input
E — Chip Enable
W — Write Enable
DQ — Data In/Out

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow standard IC Handling Procedures.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) ....-0.3V to +8.0V
Input or Output Voltage Applied.................. (GND -0.3V) to (VCC +0.3V)
Storage Temperature..............................-65°C to +150°C

Operating Range

Operating Supply Voltage
HM-6514S-2/-8 .... 4.5V to 5.5V
Operating Temperature
HM-6514S-2/-8 .... -55°C to +125°C

**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications ①

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50	µA	IO = 0 Ē = VCC −0.3V
	ICCOP	Operating Supply Current ②		7	mA	Ē = 1MHz, IO = 0 VI = GND
	ICCDR	Data Retention Supply Current		25	µA	VCC = 2.0V, IO = 0 Ē = VCC
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	-1.0	+1.0	µA	VI = VCC or GND
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	µA	VIO = VCC or GND
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		V	IO = -1.0mA
	CI	Input Capacitance ③		8.0	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance ③		10.0	pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		120	ns	④
	TAVQV	Address Access Time		120	ns	④
	TELQX	Chip Enable Output Enable Time	10		ns	③④
	TEHQZ	Chip Enable Output Disable Time		50	ns	③④
	TELEH	Chip Enable Pulse Negative Width	120		ns	④
	TEHEL	Chip Enable Pulse Positive Width	50		ns	④
	TAVEL	Address Setup Time	0		ns	④
	TELAX	Address Hold Time	40		ns	④
	TWLWH	Write Enable Pulse Width	120		ns	④
	TWLEH	Write Enable Pulse Setup Time	120		ns	④
	TELWH	Write Enable Pulse Hold Time	120		ns	④
	TDVWH	Data Setup Time	50		ns	④
	TWHDX	Data Hold Time	0		ns	④
	TWLDV	Write Data Delay Time	70		ns	④
	TWLEL	Early Output High-Z Time	0		ns	④
	TEHWH	Late Output High-Z Time	0		ns	④
	TELEL	Read or Write Cycle Time	170		ns	④

NOTES:
① All devices tested at worst case temperature and V_{CC}.
② Operating supply current (ICCOP) is proportional to operating frequency. Example: typical ICCOP = 5mA/MHz.
③ Tested at initial design and after major design changes.
④ Input rise and fall times: 5ns max. Input and output timing reference level: 1.5V. Output load: 1 TTL gate equivalent and C_L = 50 to 300pF. For C_L greater than 50pF, access time is derated 0.15ns/pF.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) ....-0.3V to +8.0V
Input or Output Voltage Applied.................. (GND -0.3V) to (VCC +0.3V)
Storage Temperature..............................-65°C to +150°C

Operating Range

Operating Supply Voltage
HM-6514S-9 .... 4.5V to 5.5V
Operating Temperature
HM-6514S-9 ....-40°C to +85°C

*CAUTION: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications ①

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		25	μA	IO = 0, E̅ = VCC −0.3V
	ICCOP	Operating Supply Current ②		7	mA	E̅ = 1MHz, IO = 0, VI = GND
	ICCDR	Data Retention Supply Current		15	μA	VCC = 2.0V, IO = 0, E̅ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	-1.0	+1.0	μA	VI = VCC or GND
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	μA	VIO = VCC or GND
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		V	IO = -1.0mA
	CI	Input Capacitance ③		8.0	pF	VI = VCC or GND, f = 1MHz
	CIO	Input/Output Capacitance ③		10.0	pF	VIO = VCC or GND, f = 1MHz
A.C.	TELQV	Chip Enable Access Time		120	ns	④
	TAVQV	Address Access Time		120	ns	④
	TELQX	Chip Enable Output Enable Time	10		ns	③④
	TEHQZ	Chip Enable Output Disable Time		50	ns	③④
	TELEH	Chip Enable Pulse Negative Width	120		ns	④
	TEHEL	Chip Enable Pulse Positive Width	50		ns	④
	TAVEL	Address Setup Time	0		ns	④
	TELAX	Address Hold Time	40		ns	④
	TWLWH	Write Enable Pulse Width	120		ns	④
	TWLEH	Write Enable Pulse Setup Time	120		ns	④
	TELWH	Write Enable Pulse Hold Time	120		ns	④
	TDVWH	Data Setup Time	50		ns	④
	TWHDX	Data Hold Time	0		ns	④
	TWLDV	Write Data Delay Time	70		ns	④
	TWLEL	Early Output High-Z Time	0		ns	④
	TEHWH	Late Output High-Z Time	0		ns	④
	TELEL	Read or Write Cycle Time	170		ns	④

NOTES:
① All devices tested at worst case temperature and V_{CC}.
② Operating supply current (ICCOP) is proportional to operating frequency. Example: typical ICCOP = 5mA/MHz.
③ Tested at initial design and after major design changes.
④ Input rise and fall times: 5ns max. Input and output timing reference level: 1.5V. Output load: 1 TTL gate equivalent and C_L = 50 to 300pF. For C_L greater than 50pF, access time is derated 0.15ns/pF.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) ....-0.3V to +8.0V
Input or Output Voltage Applied .... (GND -0.3V) to (VCC +0.3V)
Storage Temperature ....-65°C to +150°C

Operating Range

Operating Supply Voltage
HM-6514B-2/-8 .... 4.5V to 5.5V
Operating Temperature
HM-6514B-2/-8 .... -55°C to +125°C

**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications ①

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50	μA	IO = 0 $\overline{E}$ = VCC −0.3V
	ICCOP	Operating Supply Current ②		7	mA	$\overline{E}$ = 1MHz, IO = 0 VI = GND
	ICCDR	Data Retention Supply Current		25	μA	VCC = 2.0V, IO = 0 $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	-1.0	+1.0	μA	VI = VCC or GND
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	μA	VIO = VCC or GND
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		V	IO = -1.0mA
	CI	Input Capacitance ③		8.0	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance ③		10.0	pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		200	ns	④
	TAVQV	Address Access Time		220	ns	④
	TELQX	Chip Enable Output Enable Time	20		ns	③ ④
	TEHQZ	Chip Enable Output Disable Time		80	ns	③ ④
	TELEH	Chip Enable Pulse Negative Width	200		ns	④
	TEHEL	Chip Enable Pulse Positive Width	90		ns	④
	TAVEL	Address Setup Time	20		ns	④
	TELAX	Address Hold Time	50		ns	④
	TWLWH	Write Enable Pulse Width	200		ns	④
	TWLEH	Write Enable Pulse Setup Time	200		ns	④
	TELWH	Write Enable Pulse Hold Time	200		ns	④
	TDVWH	Data Setup Time	120		ns	④
	TWHDX	Data Hold Time	0		ns	④
	TWLDV	Write Data Delay Time	80		ns	④
	TWLEL	Early Output High-Z Time	0		ns	④
	TEHWH	Late Output High-Z Time	0		ns	④
	TELEL	Read or Write Cycle Time	290		ns	④

NOTES:
① All devices tested at worst case temperature and V_{CC}.
② Operating supply current (ICCOP) is proportional to operating frequency. Example: typical ICCOP = 5mA/MHz.
③ Tested at initial design and after major design changes.
④ Input rise and fall times: 5ns max. Input and output timing reference level: 1.5V. Output load: 1 TTL gate equivalent and C_L = 50 to 300pF. For C_L greater than 50pF, access time is derated 0 15ns/pF.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) ....-0.3V to +8.0V
Input or Output Voltage Applied.................. (GND -0.3V) to (VCC +0.3V)
Storage Temperature ....-65°C to +150°C

Operating Range

Operating Supply Voltage
HM-6514B-9 .... 4.5V to 5.5V
Operating Temperature
HM-6514B-9 .... -40°C to +85°C

**CAUTION:* *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications ①

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		25	μA	IO = 0, $\overline{E}$ = VCC −0.3V
	ICCOP	Operating Supply Current ②		7	mA	$\overline{E}$ = 1MHz, IO = 0, VI = GND
	ICCDR	Data Retention Supply Current		15	μA	VCC = 2.0V, IO = 0, $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	-1.0	+1.0	μA	VI = VCC or GND
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	μA	VIO = VCC or GND
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		V	IO = -1.0mA
	CI	Input Capacitance ③		8.0	pF	VI = VCC or GND, f = 1MHz
	CIO	Input/Output Capacitance ③		10.0	pF	VIO = VCC or GND, f = 1MHz
A.C.	TELQV	Chip Enable Access Time		200	ns	④
	TAVQV	Address Access Time		220	ns	④
	TELQX	Chip Enable Output Enable Time	20		ns	③④
	TEHQZ	Chip Enable Output Disable Time		80	ns	③④
	TELEH	Chip Enable Pulse Negative Width	200		ns	④
	TEHEL	Chip Enable Pulse Positive Width	90		ns	④
	TAVEL	Address Setup Time	20		ns	④
	TELAX	Address Hold Time	50		ns	④
	TWLWH	Write Enable Pulse Width	200		ns	④
	TWLEH	Write Enable Pulse Setup Time	200		ns	④
	TELWH	Write Enable Pulse Hold Time	200		ns	④
	TDVWH	Data Setup Time	120		ns	④
	TWHDX	Data Hold Time	0		ns	④
	TWLDV	Write Data Delay Time	80		ns	④
	TWLEL	Early Output High-Z Time	0		ns	④
	TEHWH	Late Output High-Z Time	0		ns	④
	TELEL	Read or Write Cycle Time	290		ns	④

NOTES:
① All devices tested at worst case temperature and V_{CC}.
② Operating supply current (ICCOP) is proportional to operating frequency. Example: typical ICCOP = 5mA/MHz.
③ Tested at initial design and after major design changes.
④ Input rise and fall times: 5ns max. Input and output timing reference level: 1.5V. Output load: 1 TTL gate equivalent and C_L = 50 to 300pF. For C_L greater than 50pF, access time is derated 0.15ns/pF.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) ....-0.3V to +8.0V
Input or Output Voltage Applied .... (GND -0.3V) to (VCC +0.3V)
Storage Temperature ....-65°C to +150°C

Operating Range

Operating Supply Voltage
HM-6514-2/-8 ....4.5V to 5.5V
Operating Temperature
HM-6514-2/-8 ....-55°C to +125°C

*CAUTION: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications ①

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50	μA	IO = 0, Ē = VCC −0.3V
	ICCOP	Operating Supply Current ②		7	mA	Ē = 1MHz, IO = 0, VI = GND
	ICCDR	Data Retention Supply Current		25	μA	VCC = 2.0V, IO = 0, Ē = VCC
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	-1.0	+1.0	μA	VI = VCC or GND
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	μA	VIO = VCC or GND
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		V	IO = -1.0mA
	CI	Input Capacitance ③		8.0	pF	VI = VCC or GND, f = 1MHz
	CIO	Input/Output Capacitance ③		10.0	pF	VIO = VCC or GND, f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300	ns	④
	TAVQV	Address Access Time		320	ns	④
	TELQX	Chip Enable Output Enable Time	20		ns	③ ④
	TEHQZ	Chip Enable Output Disable Time		100	ns	③ ④
	TELEH	Chip Enable Pulse Negative Width	300		ns	④
	TEHEL	Chip Enable Pulse Positive Width	120		ns	④
	TAVEL	Address Setup Time	20		ns	④
	TELAX	Address Hold Time	50		ns	④
	TWLWH	Write Enable Pulse Width	300		ns	④
	TWLEH	Write Enable Pulse Setup Time	300		ns	④
	TELWH	Write Enable Pulse Hold Time	300		ns	④
	TDVWH	Data Setup Time	200		ns	④
	TWHDZ	Data Hold Time	0		ns	④
	TWLDV	Write Data Delay Time	100		ns	④
	TWLEL	Early Output High-Z Time	0		ns	④
	TEHWH	Late Output High-Z Time	0		ns	④
	TELEL	Read or Write Cycle Time	420		ns	④

NOTES:
① All devices tested at worst case temperature and V_{CC}.
② Operating supply current (ICCOP) is proportional to operating frequency. Example: typical ICCOP = 5mA/MHz.
③ Tested at initial design and after major design changes.
④ Input rise and fall times: 5ns max. Input and output timing reference level: 1.5V. Output load: 1 TTL gate equivalent and C_L = 50 to 300pF. For C_L greater than 50pF, access time is derated 0.15ns/pF.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) ....-0.3V to +8.0V
Input or Output Voltage Applied.................. (GND -0.3V) to (VCC +0.3V)
Storage Temperature...............................-65°C to +150°C

Operating Range

Operating Supply Voltage
HM-6514-9 ....4.5V to 5.5V
Operating Temperature
HM-6514-9 .... -40°C to +85°C

**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications ①

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		25	μA	IO = 0, $\overline{E}$ = VCC −0.3V
	ICCOP	Operating Supply Current ②		7	mA	$\overline{E}$ = 1MHz, IO = 0, VI = GND
	ICCDR	Data Retention Supply Current		15	μA	VCC = 2.0V, IO = 0, $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	-1.0	+1.0	μA	VI = VCC or GND
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	μA	VIO = VCC or GND
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		V	IO = -1.0mA
	CI	Input Capacitance ③		8.0	pF	VI = VCC or GND, f = 1MHz
	CIO	Input/Output Capacitance ③		10.0	pF	VIO = VCC or GND, f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300	ns	④
	TAVQV	Address Access Time		320	ns	④
	TELQX	Chip Enable Output Enable Time	20		ns	③④
	TEHQZ	Chip Enable Output Disable Time		100	ns	③④
	TELEH	Chip Enable Pulse Negative Width	300		ns	④
	TEHEL	Chip Enable Pulse Positive Width	120		ns	④
	TAVEL	Address Setup Time	20		ns	④
	TELAX	Address Hold Time	50		ns	④
	TWLWH	Write Enable Pulse Width	300		ns	④
	TWLEH	Write Enable Pulse Setup Time	300		ns	④
	TELWH	Write Enable Pulse Hold Time	300		ns	④
	TDVWH	Data Setup Time	200		ns	④
	TWHDX	Data Hold Time	0		ns	④
	TWLDV	Write Data Delay Time	100		ns	④
	TWLEL	Early Output High-Z Time	0		ns	④
	TEHWH	Late Output High-Z Time	0		ns	④
	TELEL	Read or Write Cycle Time	420		ns	④

NOTES:
① All devices tested at worst case temperature and V_{CC}.
② Operating supply current (ICCOP) is proportional to operating frequency. Example: typical ICCOP = 5mA/MHz.
③ Tested at initial design and after major design changes.
④ Input rise and fall times: 5ns max. Input and output timing reference level: 1.5V. Output load: 1 TTL gate equivalent and C_L = 50 to 300pF. For C_L greater than 50pF, access time is derated 0.15ns/pF.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) ....-0.3V to +8.0V
Input or Output Voltage Applied.................. (GND -0.3V) to (VCC +0.3V)
Storage Temperature..............................-65°C to +150°C

Operating Range

Operating Supply Voltage
HM-6514C-9..4.5V to 5.5V
Operating Temperature
HM-6514C-9..-40°C to +85°C

**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications ①

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100	μA	IO = 0, Ē = VCC –0.3V
	ICCOP	Operating Supply Current ②		7	mA	Ē = 1MHz, IO = 0, VI = GND
	ICCDR	Data Retention Supply Current		50	μA	VCC = 2.0V, IO = 0, Ē = VCC
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	-1.0	+1.0	μA	VI = VCC or GND
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	μA	VIO = VCC or GND
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		V	IO = -1.0mA
	CI	Input Capacitance ③		8.0	pF	VI = VCC or GND, f = 1MHz
	CIO	Input/Output Capacitance ③		10.0	pF	VIO = VCC or GND, f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300	ns	④
	TAVQV	Address Access Time		320	ns	④
	TELQX	Chip Enable Output Enable Time	20		ns	③④
	TEHQZ	Chip Enable Output Disable Time		100	ns	③④
	TELEH	Chip Enable Pulse Negative Width	300		ns	④
	TEHEL	Chip Enable Pulse Positive Width	120		ns	④
	TAVEL	Address Setup Time	20		ns	④
	TELAX	Address Hold Time	50		ns	④
	TWLWH	Write Enable Pulse Width	300		ns	④
	TWLEH	Write Enable Pulse Setup Time	300		ns	④
	TELWH	Write Enable Pulse Hold Time	300		ns	④
	TDVWH	Data Setup Time	200		ns	④
	TWHDX	Data Hold Time	0		ns	④
	TWLDV	Write Data Delay Time	100		ns	④
	TWLEL	Early Output High-Z Time	0		ns	④
	TEHWH	Late Output High-Z Time	0		ns	④
	TELEL	Read or Write Cycle Time	420		ns	④

NOTES:
① All devices tested at worst case temperature and V_{CC}.
② Operating supply current (ICCOP) is proportional to operating frequency. Example: typical ICCOP = 5mA/MHz.
③ Tested at initial design and after major design changes.
④ Input rise and fall times: 5ns max. Input and output timing reference level: 1.5V. Output load: 1 TTL gate equivalent and C_L = 50 to 300pF. For C_L greater than 50pF, access time is derated 0.15ns/pF.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) ....-0.3V to +8.0V
Input or Output Voltage Applied .... (GND -0.3V) to (VCC +0.3V)
Storage Temperature ....-65°C to +150°C

Operating Range

Operating Supply Voltage
HM-6514-5 ....4.5V to 5.5V
Operating Temperature
HM-6514-5 ....0°C to +70°C

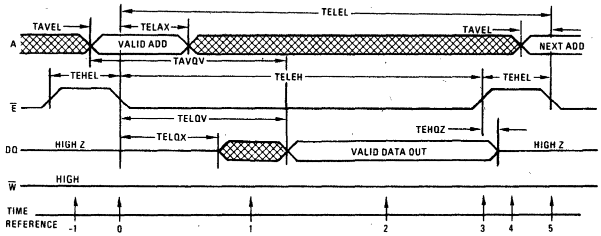
**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications ①

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		350	µA	Ē = VCC −0.3V IO = 0
	ICCOP	Operating Supply Current ②		7	mA	Ē = 1MHz, IO = 0 VI = GND
	ICCDR	Data Retention Supply Current		200	µA	VCC = 2.0V IO = 0 Ē=VCC
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	-10.0	+10.0	µA	VI = VCC or GND
	IIOZ	Input/Output Leakage Current	-10.0	+10.0	µA	VIO = VCC or GND
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		V	IO = -0.4mA
	CI	Input Capacitance③		8.0	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance③		10.0	pF	VI = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		350	ns	④
	TAVQV	Address Access Time		370	ns	④
	TELQX	Chip Enable Output Enable Time	20		ns	③④
	TEHQZ	Chip Enable Output Disable Time		100	ns	③④
	TELEH	Chip Enable Pulse Negative Width	350		ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		ns	④
	TAVEL	Address Setup Time	20		ns	④
	TELAX	Address Hold Time	50		ns	④
	TWLWH	Write Enable Pulse Width	350		ns	④
	TWLEH	Write Enable Pulse Setup Time	350		ns	④
	TELWH	Write Enable Pulse Hold Time	350		ns	④
	TDVWH	Data Setup Time	250		ns	④
	TWHDX	Data Hold Time	0		ns	④
	TWLDV	Write Data Delay Time	100		ns	④
	TWLEL	Early Output High-Z Time	0		ns	④
	TEHWH	Late Output High-Z Time	0		ns	④
	TELEL	Read or Write Cycle Time	500		ns	④

NOTES:
① All devices tested at worst case temperature and V_{CC}.
② Operating supply current (ICCOP) is proportional to operating frequency. Example: typical ICCOP = 5mA/MHz.
③ Tested at initial design and after major design changes.
④ Input rise and fall times: 5ns max. Input and output timing reference level: 1.5V. Output load: 1 TTL gate equivalent and C_L = 50 to 300pF. For C_L greater than 50pF, access time is derated 0.15ns/pF.

Read Cycle

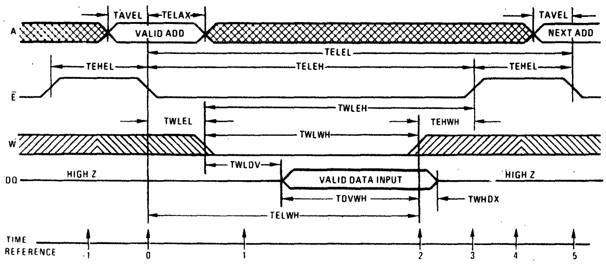


TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	DATA I/O DQ	FUNCTION
1	H	X	X	Z	MEMORY DISABLED
0	↘	H	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	X	X	OUTPUT ENABLED
2	L	H	X	V	OUTPUT VALID
3	↗	H	X	V	READ ACCOMPLISHED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address setup and hold time requirements must be met. After the required hold time the addresses may change state without affecting device operation. During time (T = 1) the outputs become enabled but data is not valid until time (T = 2). $\overline{W}$ must remain high throughout the read cycle. After the data has been read $\overline{E}$ may return high (T = 3). This will force the output buffers and all inputs to a disabled state at time (T = 4). The memory is now ready for the next cycle.

Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{W}$	A	DQ	FUNCTION
1	H	X	X	Z	MEMORY DISABLED
0	↘	X	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	X	Z	WRITE PERIOD BEGINS
2	L	↗	X	V	DATA IN IS WRITTEN
3	↗	H	X	Z	WRITE COMPLETED
4	H	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	X	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The write cycle is initiated by the falling edge of $\overline{E}$ (T = 0), which latches the address information in the on-chip registers. There are two basic types of write cycles, which differ in the control of the common data-in/data-out bus.

Case 1: $\overline{E}$ falls before $\overline{W}$ falls

The output buffers may become enabled (reading) if $\overline{E}$ falls before $\overline{W}$ falls. $\overline{W}$ is used to disable (three-state) the outputs so input data can be applied. TWLDV must be met to allow the $\overline{W}$ signal time to disable the outputs before applying input data. Also, at the end of the cycle the outputs may become active if $\overline{W}$ rises before $\overline{E}$. The RAM outputs and all inputs will -state) after $\overline{E}$ rises (TEHQZ). In this type of write cycle TWLEL and TEHWH may be ignored.

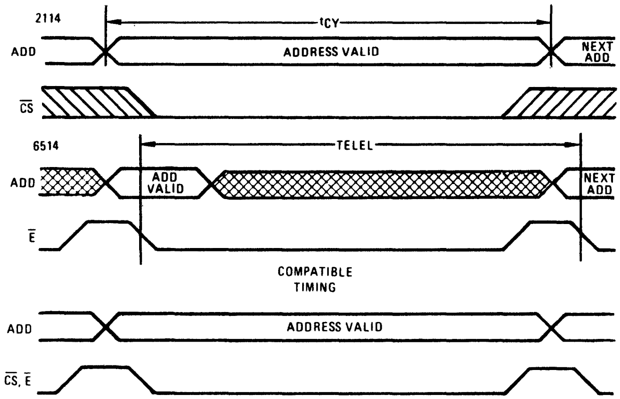
Case 2: $\overline{E}$ falls equal to or after $\overline{W}$ falls, and $\overline{E}$ rises before or equal to $\overline{W}$ rising

This $\overline{E}$ and $\overline{W}$ control timing will guarantee that the data outputs will stay disabled throughout the cycle, thus simplyifying the data input timing. TWLEL and TEHWH must be met but TWLDV becomes meaningless and can be ignored. In this cycle TDVWH and TWHDX become TDVEH and TEHDX. In other words, reference data setup and hold times to the $\overline{E}$ rising edge.

	IF	OBSERVE	IGNORE
Case 1	$\overline{E}$ falls before $\overline{W}$	TWLDV	TWLEL
Case 2	$\overline{E}$ falls after $\overline{W}$ & $\overline{E}$ rises before $\overline{W}$	TWLEL TEHWH	TWLDV TWHDX

If a series of consecutive write cycles are to be performed, $\overline{W}$ may be held low until all desired locations have been written (an extension of Case 2).

2114 Capability



2114 — Requires the Address to Remain Valid Throughout the Cycle.

6514 — Requires Valid Address for Only a Small Portion of the Cycle, but Requires $\overline{E}$ to Fall to Initiate Each Cycle.

HARRIS

HM-6516

2K x 8 CMOS RAM

Features

- **Low Power Standby .... 275μW Max.**
- **Low Power Operation .... 55mW/MHz Max.**
- **Fast Access .... 120/200ns Max.**
- **Industry Standard Pinout**
- **Single Supply .... 5 Volt VCC**
- **TTL Compatible**
- **Static Memory Cells**
- **High Output Drive**
- **On Chip Address Latches**
- **Easy Microprocessor Interfacing**
- **Wide Operating Temperature Ranges:**
  - **HM-6516-5 .... 0°C to +70°C**
  - **HM-6516-9 .... -40°C to +85°C**
  - **HM-6516-2/-8 .... -55°C to +125°C**

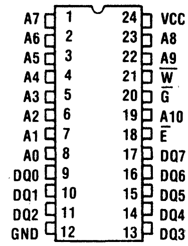
Description

The HM-6516 is a CMOS 2048 x 8 Static Random Access Memory. Extremely low power operation is achieved by the use of complementary MOS design techniques. This low power is further enhanced by the use of synchronous circuit techniques that keep the active (operating) power low, and also give fast access times. The pinout of the HM-6516 is the popular 24 pin, 8 bit wide JEDEC standard which allows easy memory board layouts, flexible enough to accomodate a variety of PROMs, RAMs, EPROMs, and ROMs.

The HM-6516 is ideally suited for use in microprocessor based systems. The byte wide organization simplifies the memory array design,and keeps operating power down to a minimum because only one device is enabled at a time. The address latches allow very simple interfacing to recent generation microprocessors which employ a multiplexed address/data bus. The convenient output enable control also simplifies multiplexed bus interfacing by allowing the data outputs to be controlled independent of the chip enable.

Pinouts

TOP VIEW

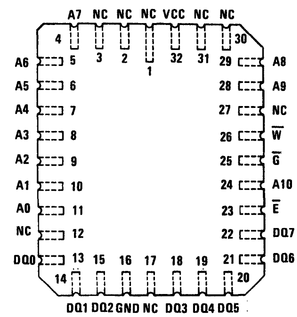


PIN NAMES

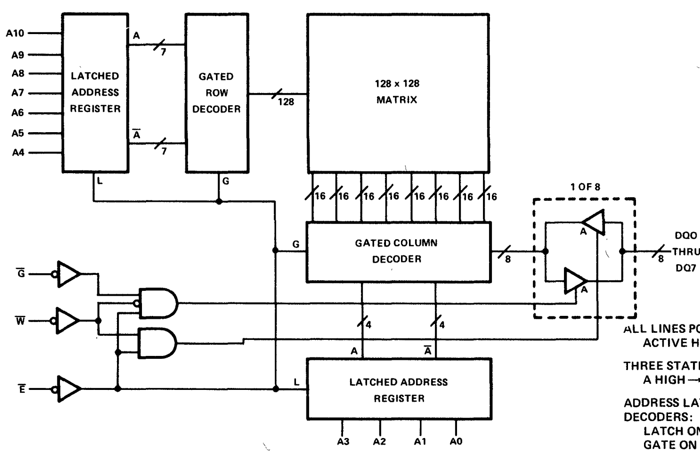
A	Address Input
DQ	Data Input/Output
Ē	Chip Enable
Ḡ	Output Enable
W̄	Write Enable
NC	No Connect

LCC

TOP VIEW



Functional Diagram



ALL LINES POSITIVE LOGIC - ACTIVE HIGH

THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE

ADDRESS LATCHES AND GATED DECODERS:
LATCH ON FALLING EDGE OF Ē
GATE ON FALLING EDGE OF Ē

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) ....-0.3V to +8.0V
Input or Output Voltage Applied .... (GND -0.3V) to (VCC +0.3V)
Storage Temperature ....-65°C to +150°C

Operating Range

Operating Supply Voltage
HM-6516B-8 .... 4.5V to 5.5V
HM-6516B-9 .... 4.5V to 5.5V
Operating Temperature
HM-6516B-8 .... -55°C to +125°C
HM-6516B-9 .... -40°C to +85°C

**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		10	mA	f=1MHz, IO=0, G̅=VCC VI = VCC or GND
	ICCDR	Data Retention Supply Current		25	μA	IO = 0, VCC = 2.0, VI = VCC or GND, E̅ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	−1.0	+1.0	μA	VI = VCC or GND
	IIOZ	Input/Output Leakage Current	−1.0	+1.0	μA	VIO = VCC or GND
	VIL	Input Low Voltage	−0.3	0.8	V	
	VIH	Input High Voltage	2.4	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 3.2mA
	VOH	Output High Voltage	2.4		V	IO = −1.0mA
	CI	Input Capacitance ③		8.0	pF	VI = VCC or GND, f = 1MHz
	CIO	Input/Output Capacitance ③		10.0	pF	VIO = VCC or GND, f = 1MHz
A.C. ⑤	TELQV	Chip Enable Access Time		120	ns	④
	TAVQV	Address Access Time		120	ns	④
	TELQX	Chip Enable Output Enable Time	10		ns	③
	TWLQZ	Write Enable Output Disable Time		50	ns	③
	TEHQZ	Chip Enable Output Disable Time		50	ns	③
	TGLQV	Output Enable Output Valid Time		80	ns	④
	TGLQX	Output Enable Output Enable Time	10		ns	③
	TGHQZ	Output Enable Output Disable Time		50	ns	③
	TELEH	Chip Enable Pulse Negative Width	120		ns	④
	TEHEL	Chip Enable Pulse Positive Width	50		ns	④
	TAVEL	Address Setup Time	0		ns	④
	TELAX	Address Hold Time	30		ns	④
	TWLWH	Write Enable Pulse Width	120		ns	④
	TWLEH	Write Enable Pulse Setup Time	120		ns	④
	TELWH	Write Enable Pulse Hold Time	120		ns	④
	TDVWH	Data Setup Time	50		ns	④
	TWHDX	Data Hold Time	10		ns	④
	TWLDV	Write Data Delay Time	50		ns	④
	TELEL	Read or Write Cycle Time	170		ns	④

NOTES:
① All devices tested at worst case temperature and V_{CC}.
② Typical derating: 5mA/MHz increase in ICCOP.
③ Tested at initial design and after major design changes.
④ Input pulse levels: 0V to 3V. Input rise and fall times: 5ns max. Input and output timing reference levels: 1.5V. Output load: 1 TTL gate equivalent and C_L = 50 to 300pF. For C_L greater than 50pF, access time is derated 0.15ns/pF.
⑤ Tested at V_{CC} = 4.5V and 5.5V.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) ....-0.3V to +8.0V
Input or Output Voltage Applied .... (GND -0.3V) to (VCC +0.3V)
Storage Temperature ....-65°C to +150°C

Operating Range

Operating Supply Voltage
HM-6516-8 .... 4.5V to 5.5V
HM-6516-9 .... 4.5V to 5.5V
Operating Temperature
HM-6516-8 ....-55°C to +125°C
HM-6516-9 ....-40°C to +85°C

*CAUTION: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications

	SYMBOL	PARAMETER	TEMP & VCC = OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100	µA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		10	mA	f=1MHz, IO=0, $\overline{G}$=VCC VI = VCC or GND
	ICCDR	Data Retention Supply Current		50	µA	IO = 0, VCC = 2.0, VI = VCC or GND, $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	−1.0	+1.0	µA	VI = VCC or GND
	IIOZ	Input/Output Leakage Current	−1.0	+1.0	µA	VIO = VCC or GND
	VIL	Input Low Voltage	−0.3	0.8	V	
	VIH	Input High Voltage	2.4	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 3.2mA
	VOH	Output High Voltage	2.4		V	IO = −1.0mA
	CI	Input Capacitance ③		8.0	pF	VI = VCC or GND, f = 1MHz
	CIO	Input/Output Capacitance ③		10.0	pF	VIO = VCC or GND, f = 1MHz
A.C. ⑤	TELQV	Chip Enable Access Time		200	ns	④
	TAVQV	Address Access Time		200	ns	④
	TELQX	Chip Enable Output Enable Time	10		ns	③
	TWLQZ	Write Enable Output Disable Time		80	ns	③
	TEHQZ	Chip Enable Output Disable Time		80	ns	③
	TGLQV	Output Enable Output Valid Time		80	ns	④
	TGLQX	Output Enable Output Enable Time	10		ns	③
	TGHQZ	Output Enable Output Disable Time		80	ns	③
	TELEH	Chip Enable Pulse Negative Width	200		ns	④
	TEHEL	Chip Enable Pulse Positive Width	80		ns	④
	TAVEL	Address Setup Time	0		ns	④
	TELAX	Address Hold Time	50		ns	④
	TWLWH	Write Enable Pulse Width	200		ns	④
	TWLEH	Write Enable Pulse Setup Time	200		ns	④
	TELWH	Write Enable Pulse Hold Time	200		ns	④
	TDVWH	Data Setup Time	80		ns	④
	TWHDX	Data Hold Time	10		ns	④
	TWLDV	Write Data Delay Time	80		ns	④
	TELEL	Read or Write Cycle Time	280		ns	④

NOTES:
① All devices tested at worst case temperature and V_{CC}.
② Typical derating: 5mA/MHz increase in ICCOP.
③ Tested at initial design and after major design changes.
④ Input pulse levels: 0V to 3V. Input rise and fall times: 5ns max. Input and output timing reference levels: 1.5V. Output load: 1 TTL gate equivalent and C_L = 50 to 300pF. For C_L greater than 50pF, access time is derated 0.15ns/pF.
⑤ Tested at V_{CC} = 4.5V and 5.5V.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) ....-0.3V to +8.0V
Input or Output Voltage Applied .... (GND -0.3V) to (VCC +0.3V)
Storage Temperature ....-65°C to +150°C

*CAUTION: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Operating Range

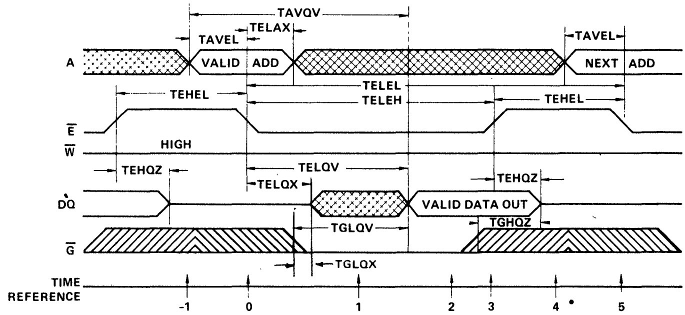
Operating Supply Voltage
HM-6516-5 .... 4.5V to 5.5V
Operating Temperature
HM-6516-5 .... 0°C to +70°C

Electrical Specifications

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		500	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		10	mA	f=1MHz,IO=0,$\overline{G}$=VCC VI = VCC or GND
	ICCDR	Data Retention Supply Current		250	μA	IO = 0, VCC = 2.0, VI = VCC or GND, $\overline{E}$ = VCC
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	−5.0	+5.0	μA	VI = VCC or GND
	IIOZ	Input/Output Leakage Current	−5.0	+5.0	μA	VIO = VCC or GND
	VIL	Input Low Voltage	−0.3	0.8	V	
	VIH	Input High Voltage	2.4	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 3.2mA
	VOH	Output High Voltage	2.4		V	IO = −1.0mA
	CI	Input Capacitance ③		8.0	pF	VI = VCC or GND, f = 1MHz
	CIO	Input/Output Capacitance ③		10.0	pF	VIO = VCC or GND, f = 1MHz
A.C. ⑤	TELQV	Chip Enable Access Time		200	ns	④
	TAVQV	Address Access Time		200	ns	④
	TELQX	Chip Enable Output Enable Time	10		ns	③
	TWLQZ	Write Enable Output Disable Time		80	ns	③
	TEHQZ	Chip Enable Output Disable Time		80	ns	③
	TGLQV	Output Enable Output Valid Time		80	ns	④
	TGLQX	Output Enable Output Enable Time	10		ns	③
	TGHQZ	Output Enable Output Disable Time		80	ns	③
	TELEH	Chip Enable Pulse Negative Width	200		ns	④
	TEHEL	Chip Enable Pulse Positive Width	80		ns	④
	TAVEL	Address Setup Time	0		ns	④
	TELAX	Address Hold Time	50		ns	④
	TWLWH	Write Enable Pulse Width	200		ns	④
	TWLEH	Write Enable Pulse Setup Time	200		ns	④
	TELWH	Write Enable Pulse Hold Time	200		ns	④
	TDVWH	Data Setup Time	80		ns	④
	TWHDX	Data Hold Time	10		ns	④
	TWLDV	Write Data Delay Time	80		ns	④
	TELEL	Read or Write Cycle Time	280		ns	④

NOTES:
① All devices tested at worst case temperature and V_{CC}.
② Typical derating: 5mA/MHz increase in ICCOP.
③ Tested at initial design and after major design changes.
④ Input pulse levels: 0V to 3V. Input rise and fall times: 5ns max. Input and output timing reference levels: 1.5V. Output load: 1 TTL gate equivalent and C_L = 50 to 300pF. For C_L greater than 50pF, access time is derated 0.15ns/pF.
⑤ Tested at V_{CC} = 4.5V and 5.5V.

Read Cycle

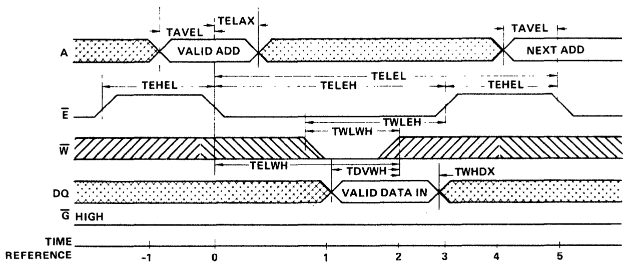


TRUTH TABLE

TIME REFERENCE	INPUTS E	W	G	A	DQ	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↘	H	X	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	L	X	X	OUTPUT ENABLED
2	L	H	L	X	V	OUTPUT VALID
3	↗	H	X	X	V	READ ACCOMPLISHED
4	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	X	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0), minimum address setup and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1), the outputs become enabled but data is not valid until time (T = 2), $\overline{W}$ must remain high throughout the read cycle. After the data has been read, $\overline{E}$ may return high (T = 3). This will force the output buffers into a high impedance mode at time (T = 4). $\overline{G}$ is used to disable the output buffers when in a logical "1" state (T = -1, 0, 3, 4, 5). After (T = 4) time, the memory is ready for the next cycle.

Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS E	W	G	A	DQ	FUNCTION
-1	H	X	H	X	X	MEMORY DISABLED
0	↘	X	H	V	X	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	H	X	X	WRITE PERIOD BEGINS
2	L	↗	H	X	V	DATA IN IS WRITTEN
3	↗	H	H	X	X	WRITE COMPLETED
4	H	X	H	X	X	PREPARE FOR NEXT CYCLE (SAME AS-1)
5	↘	X	H	V	X	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The write cycle is initiated on the falling edge of $\overline{E}$ (T = 0), which latches the address information in the on chip registers. If a write cycle is to be performed where the output is not to become active, $\overline{G}$ can be held high (inactive). TDVWH and TWHDX must be met for proper device operation regardless of $\overline{G}$. If $\overline{E}$ and $\overline{G}$ fall before $\overline{W}$ falls (read mode), a possible bus conflict may exist. If $\overline{E}$ rises before $\overline{W}$ rises, reference data setup and hold times to the $\overline{E}$ rising edge. The write operation is terminated by the first rising edge of $\overline{W}$ (T = 2) or $\overline{E}$(T = 3). After the minimum $\overline{E}$ high time (TEHEL), the next cycle may begin. If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may be held low unitl all desired locations have been written. In this case, data setup and hold times must be referenced to the rising edge of $\overline{E}$.

HARRIS

HM-65162

ADVANCE INFORMATION

2048 x 8 Asynchronous CMOS Static RAM

Features

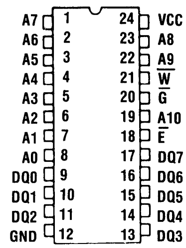
- **Fast Access Time .... 55/70/90ns Max.**
- **Low Standby Current..50μA Max.**
- **Low Operating Current... 70mA Max.**
- **Data Retention @ 2.0 Volts ....20μA Max.**
- **TTL Compatible Inputs and Outputs**
- **JEDEC Approved Pinout (2716, 6116 Type)**
- **No Clocks or Strobes Required**
- **Wide Temperature Range.. -55°C to +125°C**
- **Equal Cycle and Access Time**
- **Single 5 Volt Supply**
- **Gated Inputs—No Pull-Up or Pull-Down Resistors Required**

Description

The HM-65162 is a CMOS 2048 x 8 Static Random Access Memory manufactured using the Harris Advanced SAJI V process. The device utilizes asynchronous circuit design for fast cycle time and ease of use. The pinout is the JEDEC 24 pin, 8-bit wide standard which allows easy memory board layouts flexible to accommodate a variety of industry standard PROMs, RAMs, ROMs and EPROMs. The HM-65162 is ideally suited for use in microprocessor based systems with its 8-bit word length organization. The convenient output enable also simplifies the bus interface by allowing the data outputs to be controlled independent of the chip enable. Gated inputs lower operating current and also eliminate the need for pull-up or pull-down resistors.

Pinouts

TOP VIEW

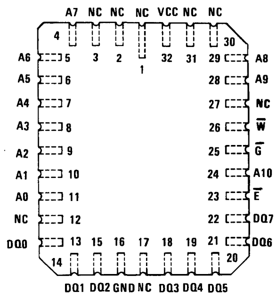


PIN NAMES

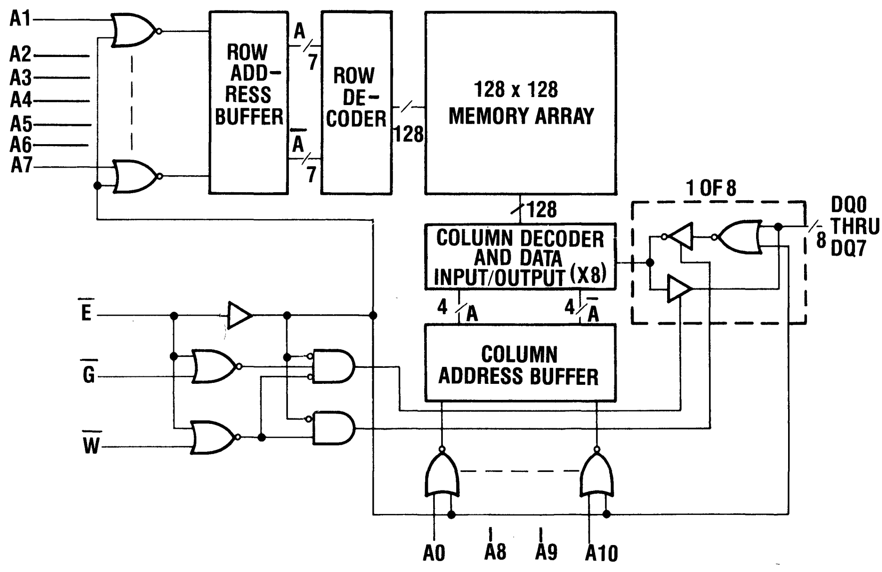
A	Address Input
DQ	Data Input/Output
Ē	Chip Enable
Ḡ	Output Enable
W̄	Write Enable
NC	No Connect

LCC

TOP VIEW



Functional Description



Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) ....-0.3V to +8.0V
Input or Output Voltage Applied.................. (GND -0.3V) to (VCC +0.3V)
Storage Temperature...............................-65°C to +150°C

Operating Range

Operating Supply Voltage
HM-65162S-9 .... 4.5V to 5.5V
Operating Temperature
HM-65162S-9 ....-40°C to +85°C

*CAUTION: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications   Advance Information

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB1	Standby Supply Current		100	μA	IO = 0, Ē = VCC−0.3V ⑥
	ICCSB	Standby Supply Current		8	mA	Ē = 2.2V, IO = 0 ⑥
	ICC	Enabled Supply Current		70	mA	Ē = 0.8V, IO = 0 ⑥
	ICCOP	Operating Supply Current ②		70	mA	Ē = 0.8V, IO = 0 ⑥ f = 1 MHz
	ICCDR	Data Retention Supply Current		40	μA	IO = 0, VCC = 2.0 Ē = VCC−0.3V
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	−1.0	+1.0	μA	VI = VCC or GND ⑥
	IIOZ	Input/Output Leakage Current	−1.0	+1.0	μA	VIO = VCC or GND ⑥
	VIL	Input Low Voltage	−0.3	0.8	V	
	VIH	Input High Voltage	2.2	VCC +0.3V	V	
	VOL	Output Low Voltage		0.4	V	IO = 4.0mA ⑤
	VOH	Output High Voltage	2.4		V	IO = −1.0mA ⑤
	CI	Input Capacitance ③		8	pF	VI = VCC = GND, f = 1 MHz
	CIO	Input/Output Capacitance ③		10	pF	VIO = VCC = GND, f = 1 MHz
A.C. READ CYCLE	TAVAV	Read Cycle Time	55		ns	④ ⑤ ⑥
	TAVQV	Address Access Time		55	ns	④ ⑤ ⑥
	TELQV	Chip Enable Access Time		55	ns	④ ⑤ ⑥
	TELQX	Chip Enable Output Enable Time	5		ns	③ ④ ⑤ ⑥
	TGLQV	Output Enable Access Time		35	ns	④ ⑤ ⑥
	TGLQX	Output Enable Output Enable Time	5		ns	③ ④ ⑤ ⑥
	TEHQZ	Chip Enable Output Disable Time		35	ns	③ ④ ⑤ ⑥
	TGHQZ	Output Enable Output Disable Time		30	ns	③ ④ ⑤ ⑥
	TAVQX	Output Hold from Address Change	5		ns	④ ⑤ ⑥
A.C. WRITE CYCLE	TAVAV	Write Cycle Time	55		ns	④ ⑤ ⑥
	TELWH	Chip Selection to End of Write	45		ns	④ ⑤ ⑥
	TAVWL	Address Setup Time	5		ns	④ ⑤ ⑥
	TWLWH	Write Enable Pulse Width	40		ns	④ ⑤ ⑥
	TWHAX	Write Enable Read Setup Time	10		ns	④ ⑤ ⑥
	TGHQZ	Output Enable Output Disable Time		30	ns	③ ④ ⑤ ⑥
	TWLQZ	Write Enable Output Disable Time		30	ns	③ ④ ⑤ ⑥
	TDVWH	Data Setup Time	25		ns	④ ⑤ ⑥
	TWHDX	Data Hold Time	10		ns	④ ⑤ ⑥
	TWHQX	Write Enable Output Enable Time	0		ns	④ ⑤ ⑥
	TWLEH	Write Enable Pulse Setup Time	45		ns	④ ⑤ ⑥
	TDVEH	Chip Enable Data Setup Time	25		ns	④ ⑤ ⑥
	TAVWH	Address Valid to End of Write	45		ns	④ ⑤ ⑥

NOTES.
① All devices tested at worst case temperature and supply voltage limits.
② Typical derating: 5mA/MHz increase in ICCOP. VI = VCC or GND.
③ Tested at initial design and after major process/design changes.
④ Input pulse levels 0V to 3V. Input rise and fall times 5ns max. Input and output timing reference levels 1.5V. Output load: 1 TTL gate equivalent and CL = 50 to 300pV. For CL greater than 50pF, access time is derated 0.15ns/pF.
⑤ Tested at VCC = 4.5V.
⑥ Tested at VCC = 5.5V.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) ....-0.3V to +8.0V
Input or Output Voltage Applied .... (GND -0.3V) to (VCC +0.3V)
Storage Temperature ....-65°C to +150°C

Operating Range

Operating Supply Voltage ....4.5V to 5.5V
Operating Temperature
HM-65162B-8 ....-55°C to +125°C
HM-65162B-9 ....-40°C to +85°C

***CAUTION:** *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications

		SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
D.C.		ICCSB1	Standby Supply Current		50	μA	IO = 0, $\overline{E}$ = VCC−0.3V ⑥
		ICCSB	Standby Supply Current		8	mA	$\overline{E}$ = 2.2V, IO = 0 ⑥
		ICC	Enabled Supply Current		70	mA	$\overline{E}$ = 0.8V, IO = 0 ⑥
		ICCOP	Operating Supply Current ②		70	mA	$\overline{E}$ = 0.8V, IO = 0 ⑥ f = 1 MHz
		ICCDR	Data Retention Supply Current		20	μA	IO = 0, VCC = 2.0 $\overline{E}$ = VCC−0.3V
		VCCDR	Data Retention Supply Voltage	2.0		V	
		II	Input Leakage Current	−1.0	+1.0	μA	VI = VCC or GND ⑥
		IIOZ	Input/Output Leakage Current	−1.0	+1.0	μA	VIO = VCC or GND ⑥
		VIL	Input Low Voltage	−0.3	0.8	V	
		VIH	Input High Voltage	2.2	VCC +0.3V	V	
		VOL	Output Low Voltage		0.4	V	IO = 4.0mA ⑤
		VOH	Output High Voltage	2.4		V	IO = −1.0mA ⑤
		CI	Input Capacitance ③		8	pF	VI = VCC = GND, f = 1 MHz
		CIO	Input/Output Capacitance ③		10	pF	VIO = VCC = GND, f = 1 MHz
A.C.	READ CYCLE	TAVAV	Read Cycle Time	70		ns	④ ⑤ ⑥
		TAVQV	Address Access Time		70	ns	④ ⑤ ⑥
		TELQV	Chip Enable Access Time		70	ns	④ ⑤ ⑥
		TELQX	Chip Enable Output Enable Time	5		ns	③ ④ ⑤ ⑥
		TGLQV	Output Enable Access Time		50	ns	④ ⑤ ⑥
		TGLQX	Output Enable Output Enable Time	5		ns	③ ④ ⑤ ⑥
		TEHQZ	Chip Enable Output Disable Time		35	ns	③ ④ ⑤ ⑥
		TGHQZ	Output Enable Output Disable Time		35	ns	③ ④ ⑤ ⑥
		TAVQX	Output Hold from Address Change	5		ns	④ ⑤ ⑥
	WRITE CYCLE	TAVAV	Write Cycle Time	70		ns	④ ⑤ ⑥
		TELWH	Chip Selection to End of Write	45		ns	④ ⑤ ⑥
		TAVWL	Address Setup Time	10		ns	④ ⑤ ⑥
		TWLWH	Write Enable Pulse Width	40		ns	④ ⑤ ⑥
		TWHAX	Write Enable Read Setup Time	10		ns	④ ⑤ ⑥
		TGHQZ	Output Enable Output Disable Time		35	ns	③ ④ ⑤ ⑥
		TWLQZ	Write Enable Output Disable Time		40	ns	③ ④ ⑤ ⑥
		TDVWH	Data Setup Time	30		ns	④ ⑤ ⑥
		TWHDX	Data Hold Time	10		ns	④ ⑤ ⑥
		TWHQX	Write Enable Output Enable Time	0		ns	③ ④ ⑤ ⑥
		TWLEH	Write Enable Pulse Setup Time	40		ns	④ ⑤ ⑥
		TDVEH	Chip Enable Data Setup Time	30		ns	④ ⑤ ⑥
		TAVWH	Address Valid to End of Write	50		ns	④ ⑤ ⑥

NOTES:
① All devices tested at worst case temperature and supply voltage limits.
② Typical derating: 5mA/MHz increase in ICCOP. VI = VCC or GND.
③ Tested at initial design and after major process/design changes.
④ Input pulse levels 0V to 3V. Input rise and fall times 5ns max. Input and output timing reference levels 1.5V. Output load: 1 TTL gate equivalent and CL = 50 to 300pF. For CL greater than 50pF, access time is derated 0.15ns/pF.
⑤ Tested at VCC = 4.5V.
⑥ Tested at VCC = 5.5V

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) .... -0.3V to +8.0V
Input or Output Voltage Applied .... (GND -0.3V) to (VCC +0.3V)
Storage Temperature .... -65°C to +150°C

Operating Range

Operating Supply Voltage .... 4.5V to 5.5V
Operating Temperature
HM-65162-8 .... -55°C to +125°C
HM-65162-9 .... -40°C to +85°C

**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB1	Standby Supply Current		100	μA	IO = 0, Ē = VCC−0.3V ⑥
	ICCSB	Standby Supply Current		8	mA	Ē = 2.2V, IO = 0 ⑥
	ICC	Enabled Supply Current		70	mA	Ē = 0.8V, IO = 0 ⑥
	ICCOP	Operating Supply Current ②		70	mA	Ē = 0.8V, IO = 0 ⑥ f = 1 MHz
	ICCDR	Data Retention Supply Current		40	μA	IO = 0, VCC = 2.0 Ē = VCC−0.3V
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	−1.0	+1.0	μA	VI = VCC or GND ⑥
	IIOZ	Input/Output Leakage Current	−1.0	+1.0	μA	VIO = VCC or GND ⑥
	VIL	Input Low Voltage	−0.3	0.8	V	
	VIH	Input High Voltage	2.2	VCC +0.3V	V	
	VOL	Output Low Voltage		0.4	V	IO = 4.0mA ⑤
	VOH	Output High Voltage	2.4		V	IO = −1.0mA ⑤
	CI	Input Capacitance ③		8	pF	VI = VCC = GND, f = 1 MHz
	CIO	Input/Output Capacitance ③		10	pF	VIO = VCC = GND, f = 1 MHz
A.C. READ CYCLE	TAVAV	Read Cycle Time	90		ns	④ ⑤ ⑥
	TAVQV	Address Access Time		90	ns	④ ⑤ ⑥
	TELQV	Chip Enable Access Time		90	ns	④ ⑤ ⑥
	TELQX	Chip Enable Output Enable Time	5		ns	③ ④ ⑤ ⑥
	TGLQV	Output Enable Access Time		65	ns	④ ⑤ ⑥
	TGLQX	Output Enable Output Enable Time	5		ns	③ ④ ⑤ ⑥
	TEHQZ	Chip Enable Output Disable Time		50	ns	③ ④ ⑤ ⑥
	TGHQZ	Output Enable Output Disable Time		40	ns	③ ④ ⑤ ⑥
	TAVQX	Output Hold from Address Change	5		ns	④ ⑤ ⑥
A.C. WRITE CYCLE	TAVAV	Write Cycle Time	90		ns	④ ⑤ ⑥
	TELWH	Chip Selection to End of Write	55		ns	④ ⑤ ⑥
	TAVWL	Address Setup Time	10		ns	④ ⑤ ⑥
	TWLWH	Write Enable Pulse Width	55		ns	④ ⑤ ⑥
	TWHAX	Write Enable Read Setup Time	10		ns	④ ⑤ ⑥
	TGHQZ	Output Enable Output Disable Time		40	ns	③ ④ ⑤ ⑥
	TWLQZ	Write Enable Output Disable Time		50	ns	③ ④ ⑤ ⑥
	TDVWH	Data Setup Time	30		ns	④ ⑤ ⑥
	TWHDX	Data Hold Time	15		ns	④ ⑤ ⑥
	TWHQX	Write Enable Output Enable Time	0		ns	③ ④ ⑤ ⑥
	TWLEH	Write Enable Pulse Setup Time	55		ns	④ ⑤ ⑥
	TDVEH	Chip Enable Data Setup Time	30		ns	④ ⑤ ⑥
	TAVWH	Address Valid to End of Write	65		ns	④ ⑤ ⑥

NOTES:
① All devices tested at worst case temperature and supply voltage limits.
② Typical derating: 5mA/MHz increase in ICCOP. VI = VCC or GND.
③ Tested at initial design and after major process/design changes.
④ Input pulse levels 0V to 3V. Input rise and fall times 5ns max Input and output timing reference levels 1.5V. Output load: 1 TTL gate equivalent and CL = 50 to 300pV. For CL greater than 50pF, access time is derated 0.15ns/pF.
⑤ Tested at VCC = 4.5V.
⑥ Tested at VCC = 5.5V.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) ....-0.3V to +8.0V
Input or Output Voltage Applied .... (GND -0.3V) to (VCC +0.3V)
Storage Temperature ....-65°C to +150°C

Operating Range

Operating Supply Voltage ....4.5V to 5.5V
Operating Temperature
HM-65162C-8 ....-55°C to +125°C
HM-65162C-9 ....-40°C to +85°C

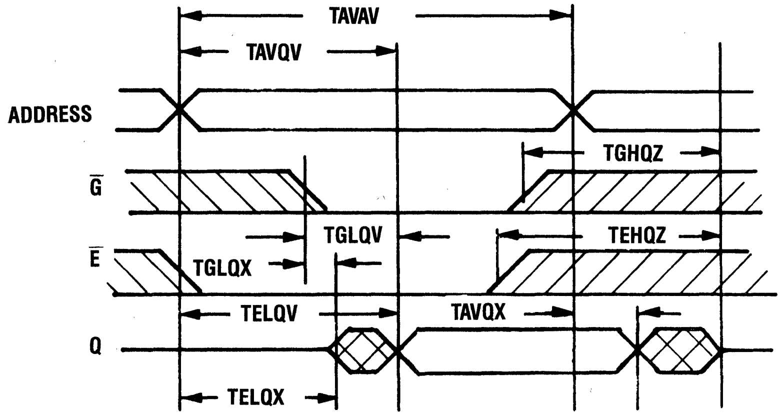
***CAUTION:** *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications

			TEMP. & VCC = OPERATING RANGE ①			
	SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB1	Standby Supply Current		900	µA	IO = 0, $\overline{E}$ = VCC−0.3V ⑥
	ICCSB	Standby Supply Current		8	mA	$\overline{E}$ = 2.2V, IO = 0 ⑥
	ICC	Enabled Supply Current		70	mA	$\overline{E}$ = 0.8V, IO = 0 ⑥
	ICCOP	Operating Supply Current ②		70	mA	$\overline{E}$ = 0.8V, IO = 0 ⑥ f = 1 MHz
	ICCDR	Data Retention Supply Current		300	µA	IO = 0, VCC = 2.0 $\overline{E}$ = VCC−0.3V
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	−5.0	+5.0	µA	VI = VCC or GND ⑥
	IIOZ	Input/Output Leakage Current	−5.0	+5.0	µA	VIO = VCC or GND ⑥
	VIL	Input Low Voltage	−0.3	0.8	V	
	VIH	Input High Voltage	2.2	VCC +0.3V	V	
	VOL	Output Low Voltage		0.4	V	IO = 4.0mA ⑤
	VOH	Output High Voltage	2.4		V	IO = −1.0mA ⑤
	CI	Input Capacitance ③		8	pF	VI = VCC = GND, f = 1 MHz
	CIO	Input/Output Capacitance ③		10	pF	VIO = VCC = GND, f = 1 MHz
A.C. READ CYCLE	TAVAV	Read Cycle Time	90		ns	④ ⑤ ⑥
	TAVQV	Address Access Time		90	ns	④ ⑤ ⑥
	TELQV	Chip Enable Access Time		90	ns	④ ⑤ ⑥
	TELQX	Chip Enable Output Enable Time	5		ns	③ ④ ⑤ ⑥
	TGLQV	Output Enable Access Time		65	ns	④ ⑤ ⑥
	TGLQX	Output Enable Output Enable Time	5		ns	③ ④ ⑤ ⑥
	TEHQZ	Chip Enable Output Disable Time		50	ns	③ ④ ⑤ ⑥
	TGHQZ	Output Enable Output Disable Time		40	ns	③ ④ ⑤ ⑥
	TAVQX	Output Hold from Address Change	5		ns	④ ⑤ ⑥
A.C. WRITE CYCLE	TAVAV	Write Cycle Time	90		ns	④ ⑤ ⑥
	TELWH	Chip Selection to End of Write	55		ns	④ ⑤ ⑥
	TAVWL	Address Setup Time	10		ns	④ ⑤ ⑥
	TWLWH	Write Enable Pulse Width	55		ns	④ ⑤ ⑥
	TWHAX	Write Enable Read Setup Time	10		ns	④ ⑤ ⑥
	TGHQZ	Output Enable Output Disable Time		40	ns	③ ④ ⑤ ⑥
	TWLQZ	Write Enable Output Disable Time		50	ns	③ ④ ⑤ ⑥
	TDVWH	Data Setup Time	30		ns	④ ⑤ ⑥
	TWHDX	Data Hold Time	15		ns	④ ⑤ ⑥
	TWHQX	Write Enable Output Enable Time	0		ns	③ ④ ⑤ ⑥
	TWLEH	Write Enable Pulse Setup Time	55		ns	④ ⑤ ⑥
	TDVEH	Chip Enable Data Setup Time	30		ns	④ ⑤ ⑥
	TAVWH	Address Valid to End of Write	65		ns	④ ⑤ ⑥

NOTES:
① All devices tested at worst case temperature and supply voltage limits.
② Typical derating: 5mA/MHz increase in ICCOP. VI = VCC or GND.
③ Tested at initial design and after major process/design changes.
④ Input pulse levels 0V to 3V. Input rise and fall times 5ns max. Input and output timing reference levels 1.5V. Output load: 1 TTL gate equivalent and CL = 50 to 300pV. For CL greater than 50pF, access time is derated 0.15ns/pF.
⑤ Tested at VCC = 4.5V.
⑥ Tested at VCC = 5.5V.

Read Cycle

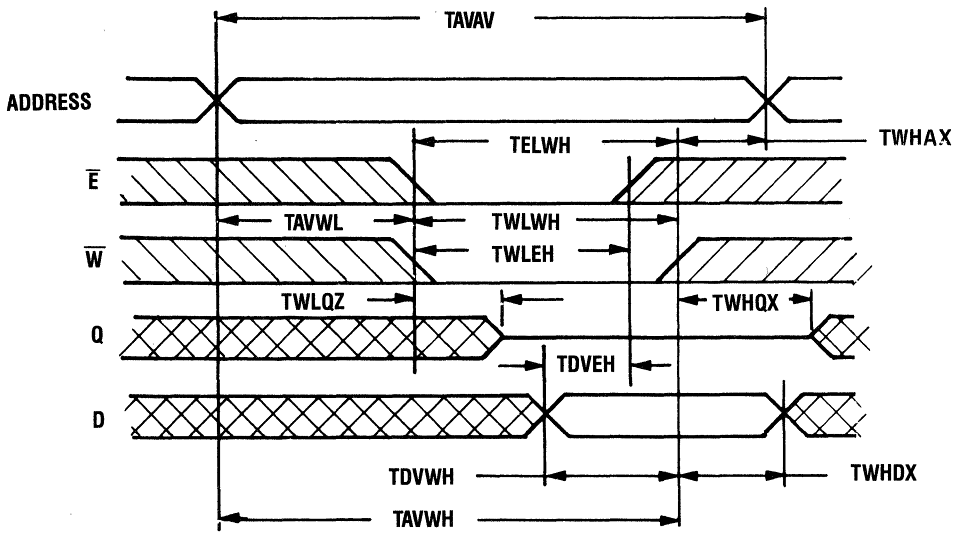


NOTE: $\overline{W}$ IS HIGH FOR A READ CYCLE

Addresses must remain stable for the duration of the read cycle. To read, $\overline{G}$ and $\overline{E}$ must be ≤ VIL and $\overline{W}$ ≥ VIH. The output buffers can be controlled independently by $\overline{G}$ while $\overline{E}$ is low. To execute consecutive read cycles, $\overline{E}$ may be tied low continuously until all desired locations are accessed. When $\overline{E}$ is low, addresses must be driven by stable logic levels and must not be in the high impedance state.

Write Cycles

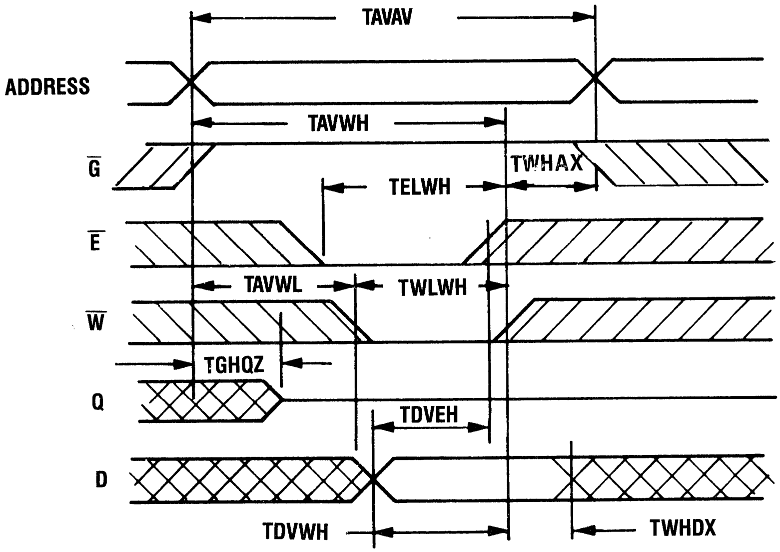
WRITE CYCLE I



NOTE: $\overline{G}$ IS LOW THROUGHOUT WRITE CYCLE

To write, addresses must be stable, $\overline{E}$ low and $\overline{W}$ falling low for a period no shorter than TWLWH. Data in is referenced with the rising edge of $\overline{W}$. (TDVWH and TWHDX). While addresses are changing, $\overline{W}$ must be high. When $\overline{W}$ falls low, the I/O pins are still in the output state for a period of TWLQZ and input data of the opposite phase to the outputs must not be applied. (Bus contention). If $\overline{E}$ transitions low simultaneously with the $\overline{W}$ line transitioning low or after the $\overline{W}$ transition, the output will remain in a high impedance state. $\overline{G}$ is held continuously low.

WRITE CYCLE II



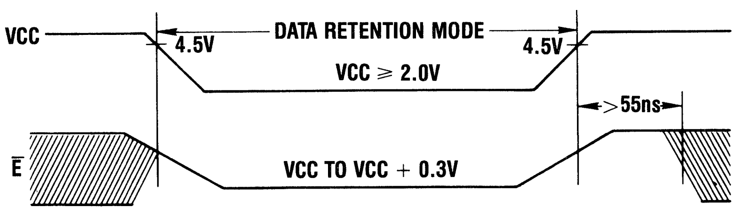
In this write cycle $\overline{G}$ has control of the output after a period, TGHQZ. $\overline{G}$ switching the output to a high impedance state allows data in to be applied without bus contention after TGHQZ. When $\overline{W}$ transitions high, the data in can change after TWHDX to complete the write cycle.

Low Voltage Data Retention

HARRIS CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip Enable ($\overline{E}$) must be held high during data retention; within VCC to VCC+0.3V.
2. On RAMs which have selects or output enables (e.g., $\overline{S}$, $\overline{G}$), one of the selects or output enables should be held in the deselected state to keep the RAM outputs high impedance, minimizing power dissipation.
3. Inputs which are to be held high (e.g., $\overline{E}$) must be kept between VCC+0.3V and 70% of VCC during the power up and power down transitions.
4. The RAM can begin operation > 55ns after VCC reaches the minimum operating voltage (4.5 volts).

DATA RETENTION TIMING



HM-65262

PRELIMINARY

16K x 1 Asynchronous CMOS Static RAM

Features

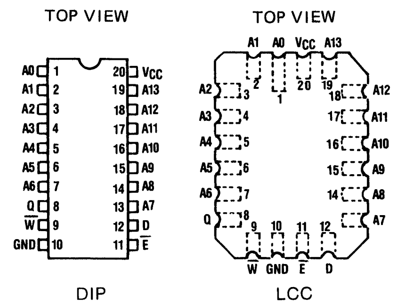
- Low Standby Current 50/100μA
- Low Operating Current 50mA
- Fast Access Time 55/70/85ns
- Low Voltage Data Retention at 2.0V
- CMOS/TTL Compatible Inputs and Outputs
- JEDEC Approved Pinout
- Equal Cycle and Access Times
- No Clocks or Strobes Required
- Single 5 Volt Supply
- Gated Inputs - No Pull-up or Pull-down Resistors Required
- Wide Temperature Range ..... -55°C to +125°C
- Easy Microprocessor Interfacing

Description

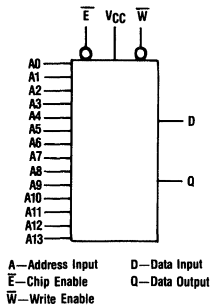
The HM-65262 is a CMOS 16384 x 1 bit Static Random Access Memory manufactured using the Harris advanced SAJI VI process. The device utilizes asynchronous circuit design for fast cycle times and ease of use. The HM-65262 is available in both the JEDEC standard 20-pin, 0.300 inch wide dual-in-line and 20 pad LCC packages, providing high board-level packing density. Gated inputs lower standby current, and also eliminate the need for pull-up or pull-down resistors.

The HM-65262, a full CMOS RAM, utilizes an array of six transistor (6T) memory cells for the most stable and lowest possible standby supply current over the full military temperature range. In addition to this, the high stability of the 6T RAM cell provides excellent protection against soft errors due to noise and alpha particles. This stability also improves the radiation tolerance of the RAM over that of four transistor (4T) devices.

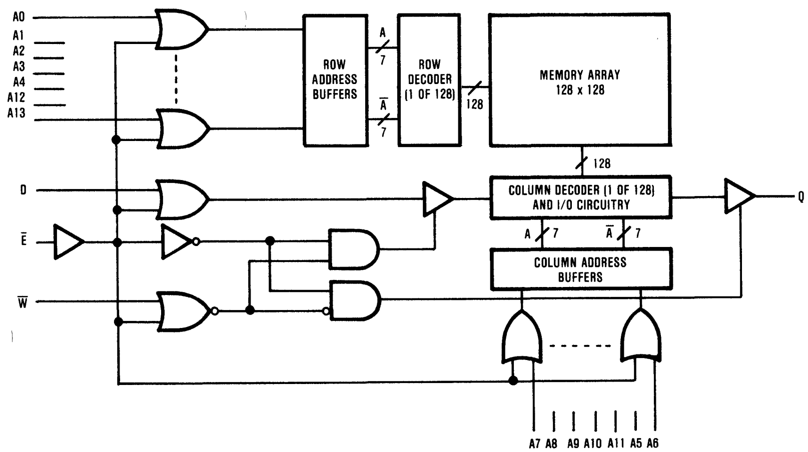
Pinouts



Logic Symbol



Functional Diagram



Absolute Maximum Ratings*

Supply Voltage (VCC-GND) .... -0.3 to 8.0V
Input or Output Voltage Applied.. GND -0.3V to VCC +0.3V
Storage Temperature ....-65°C to +150°C

Operating Ranges

Operating Supply Voltage.........................4.5V to 5.5V
Operating Temperature.....................-55°C to +125°C

*CAUTION: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications (Note 1)

	SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB1	Standby Supply Current (CMOS)	--	100	μA	IO = 0, $\overline{E}$ = VCC - 0.3V
	ICCSB	Standby Supply Current (TTL)	--	5	mA	IO = 0, $\overline{E}$ = 2.2V
	ICC	Enabled Supply Current	--	50	mA	IO = 0, $\overline{E}$ =0.8V
	ICCOP	Operating Supply Current (Note 2)	--	50	mA	IO = 0, $\overline{E}$ =0.8V,f = 1MHz
	ICCDR	Data Retention Supply Current	--	40	μA	VCC = 2.0V, $\overline{E}$ = VCC
	ICCDR1	Data Retention Supply Current	--	60	μA	VCC = 3.0V, $\overline{E}$ = VCC
	II	Input Leakage Current	-1.0	+1.0	μA	VI = GND or VCC
	IOZ	Output Leakage Current	-1.0	+1.0	μA	VIO = GND or VCC
	VCCDR	Data Retention Supply Voltage	2.0	--	V	
	VOL	Output Low Voltage	--	0.4	V	IO = 8.0mA
	VOH	Output High Voltage	2.4	--	V	IO = -4.0mA
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	2.2	VCC + 0.3	V	
	CI	Input Capacitance (Note 3)	--	8	pF	VI = VCC or GND, f = 1MHz
	CO	Output Capacitance (Note 3)	--	10	pF	VIO = VCC or GND, f = 1MHz
READ CYCLE	TAVAX	Read Cycle Time	70	--	ns	(Note 4)
	TAVQV	Address Access Time	--	70	ns	(Note 4)
	TELQV	Chip Enable Access Time	--	70	ns	(Note 4)
	TELQX	Chip Enable Output Enable Time	5	--	ns	(Note 3)
	TEHQX	Chip Disable Output Hold Time	5	--	ns	(Note 3)
	TAXQX	Address Invalid Output Hold Time	5	--	ns	(Note 3)
(5) A.C.	TEHQZ	Chip Disable Output Disable Time	--	40	ns	(Note 3)
WRITE CYCLE	TAVAX	Write Cycle Time	70	--	ns	(Note 4) ↓
	TELWH	Chip Enable to End of Write	55	--	ns	↓
	TWLWH	Write Enable Pulse Width	40	--	ns	↓
	TAVWL	Address Setup Time	0	--	ns	↓
	TWHAX	Address Hold Time	0	--	ns	↓
	TDVWH	Data Setup Time	30	--	ns	↓
	TWHDX	Data Hold Time	0	--	ns	↓
	TWLQZ	Write Enable Output Disable Time	--	40	ns	(Note 3)
	TWHQX	Write Disable Output Enable Time	0	--	ns	(Note 3)
	TAVWH	Address Valid to End of Write	55	--	ns	(Note 4) ↓
	TAVEL	Address Setup Time	0	--	ns	↓
	TEHAX	Address Hold Time	0	--	ns	↓
	TAVEH	Address Valid to End of Write	55	--	ns	↓
	TELEH	Enable Pulse Width	55	--	ns	↓
	TWLEH	Write to End of Write	40	--	ns	↓
	TDVEH	Data Setup Time	30	--	ns	↓
	TEHDX	Data Hold Time	0	--	ns	↓

NOTES:
1. All devices tested at worst case temperature and supply voltage limits.
2. Typical derating = 5mA/MHz increase in ICCOP, VI = VCC or GND.
3. Tested at initial design and major design changes.
4. Input pulse levels: 0V to 3.V.Input rise and fall times: 5ns max. Input and output timing reference levels: 1.5V. Output load: 1 TTL gate equivalent and CL = 50 to 300pF. For CL greater than 50pF, access time is derated 0.15ns/pF.
5. Tested at VCC = 4.5V and 5.5V.

Absolute Maximum Ratings*

Supply Voltage (VCC-GND) .... -0.3 to 8.0V
Input or Output Voltage Applied .. GND -0.3V to VCC +0.3V
Storage Temperature .... -65°C to +150°C

Recommended Operating Conditions

Operating Supply Voltage .... 4.5V to 5.5V
Operating Temperature .... -55°C to +125°C

**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications (Note 1)

	SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB1	Standby Supply Current (CMOS)	--	100	µA	IO = 0, $\overline{E}$ = VCC -0.3V
	ICCSB	Standby Supply Current (TTL)	--	5	mA	IO = 0, $\overline{E}$ = 2.2V
	ICC	Enabled Supply Current	--	50	mA	IO = 0, $\overline{E}$ = 0.8V
	ICCOP	Operating Supply Current (Note 2)	--	50	mA	IO = 0, $\overline{E}$ = 0.8V.f = 1MHz
	ICCDR	Data Retention Supply Current	--	40	µA	VCC = 2.0V, $\overline{E}$ = VCC
	ICCDR1	Data Retention Supply Current	--	60	µA	VCC = 3.0V, $\overline{E}$ = VCC
	II	Input Leakage Current	-1.0	+1.0	µA	VI = GND or VCC
	IOZ	Output Leakage Current	-1.0	+1.0	µA	VIO = GND or VCC
	VCCDR	Data Retention Supply Voltage	2.0	--	V	
	VOL	Output Low Voltage	--	0.4	V	IO = 8.0mA
	VOH	Output High Voltage	2.4	--	V	IO = -4.0mA
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	2.2	VCC +0.3	V	
	CI	Input Capacitance (Note 3)	--	8	pF	VI = VCC or GND, f = 1MHz
	CO	Output Capacitance (Note 3)	--	10	pF	VIO = VCC or GND, f = 1MHz
⑤ A.C. READ CYCLE	TAVAX	Read Cycle Time	85	--	ns	(Note 4)
	TAVQV	Address Access Time	--	85	ns	(Note 4)
	TELQV	Chip Enable Access Time	--	85	ns	(Note 4)
	TELQX	Chip Enable Output Enable Time	5	--	ns	(Note 3)
	TEHQX	Chip Disable Output Hold Time	5	--	ns	(Note 3)
	TAXQX	Address Invalid Output Hold Time	5	--	ns	(Note 3)
	TEHQZ	Chip Disable Output Disable Time	--	40	ns	(Note 3)
WRITE CYCLE	TAVAX	Write Cycle Time	85	--	ns	(Note 4)
	TELWH	Chip Enable to End of Write	65	--	ns	↓
	TWLWH	Write Enable Pulse Width	45	--	ns	↓
	TAVWL	Address Setup Time	0	--	ns	↓
	TWHAX	Address Hold Time	0	--	ns	↓
	TDVWH	Data Setup Time	35	--	ns	↓
	TWHDX	Data Hold Time	0	--	ns	↓
	TWLQZ	Write Enable Output Disable Time	--	40	ns	(Note 3)
	TWHQX	Write Disable Output Enable Time	0	--	ns	(Note 3)
	TAVWH	Address Valid to End of Write	65	--	ns	(Note 4)
	TAVEL	Address Setup Time	0	--	ns	↓
	TEHAX	Address Hold Time	0	--	ns	↓
	TAVEH	Address Valid to End of Write	65	--	ns	↓
	TELEH	Enable Pulse Width	65	--	ns	↓
	TWLEH	Write to End of Write	45	--	ns	↓
	TDVEH	Data Setup Time	35	--	ns	↓
	TEHDX	Data Hold Time	0	--	ns	↓

NOTES:
1. All devices tested at worst case temperature and supply voltage limits.
2. Typical derating = 5mA/MHz increase in ICCOP, VI = VCC or GND.
3. Tested at initial design and major design changes.
4. Input pulse levels: 0V to 3.V.Input rise and fall times: 5ns max. Input and output timing reference levels: 1.5V. Output load: 1 TTL gate equivalent and CL = 50 to 300pF. For CL greater than 50pF, access time is derated 0.15ns/pF.
5. Tested at VCC = 4.5V and 5.5V.

Absolute Maximum Ratings*

Supply Voltage (VCC-GND) ....-0.3 to 8.0V
Input or Output Voltage Applied ..GND -0.3Vto VCC +0.3V
Storage Temperature ....-65°C to +150°C

Recommended Operating Conditions

Operating Supply Voltage.........................4.5V to 5.5V
Operating Temperature.......................-40°C to +85°C

*CAUTION: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications (Note 1)

	SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB1	Standby Supply Current (CMOS)	--	50	µA	IO = 0, $\overline{E}$ = VCC -0.3V
	ICCSB	Standby Supply Current (TTL)	--	5	mA	IO = 0, $\overline{E}$ =2.2V
	ICC	Enabled Supply Current	--	50	mA	IO = 0, $\overline{E}$ =0.8V
	ICCOP	Operating Supply Current (Note 2)	--	50	mA	IO = 0, $\overline{E}$ =0.8V,f = 1MHz
	ICCDR	Data Retention Supply Current	--	20	µA	VCC = 2.0V, $\overline{E}$ = VCC
	ICCDR1	Data Retention Supply Current	--	30	µA	VCC = 3.0V, $\overline{E}$ = VCC
	II	Input Leakage Current	-1.0	+1.0	µA	VI = GND or VCC
	IOZ	Output Leakage Current	-1.0	+1.0	µA	VIO = GND or VCC
	VCCDR	Data Retention Supply Voltage	2.0	--	V	
	VOL	Output Low Voltage	--	0.4	V	IO = 8.0mA
	VOH	Output High Voltage	2.4	--	V	IO = -4.0mA
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	2.2	VCC +0.3	V	
	CI	Input Capacitance (Note 3)	--	8	pF	VI = VCC or GND, f = 1MHz
	CO	Output Capacitance (Note 3)	--	10	pF	VIO = VCC or GND, f = 1MHz
(5) A.C. READ CYCLE	TAVAX	Read Cycle Time	55	--	ns	(Note 4)
	TAVQV	Address Access Time	--	55	ns	(Note 4)
	TELQV	Chip Enable Access Time	--	55	ns	(Note 4)
	TELQX	Chip Enable Output Enable Time	5	--	ns	(Note 3)
	TEHQX	Chip Disable Output Hold Time	5	--	ns	(Note 3)
	TAXQX	Address Invalid Output Hold Time	5	--	ns	(Note 3)
	TEHQZ	Chip Disable Output Disable Time	--	30	ns	(Note 3)
(5) A.C. WRITE CYCLE	TAVAX	Write Cycle Time	55	--	ns	(Note 4)
	TELWH	Chip Enable to End of Write	45	--	ns	↓
	TWLWH	Write Enable Pulse Width	35	--	ns	↓
	TAVWL	Address Setup Time	0	--	ns	↓
	TWHAX	Address Hold Time	0	--	ns	↓
	TDVWH	Data Setup Time	25	--	ns	↓
	TWHDX	Data Hold Time	0	--	ns	↓
	TWLQZ	Write Enable Output Disable Time	--	30	ns	(Note 3)
	TWHQX	Write Disable Output Enable Time	0	--	ns	(Note 3)
	TAVWH	Address Valid to End of Write	45	--	ns	(Note 4)
	TAVEL	Address Setup Time	0	--	ns	↓
	TEHAX	Address Hold Time	0	--	ns	↓
	TAVEH	Address Valid to End of Write	45	--	ns	↓
	TELEH	Enable Pulse Width	45	--	ns	↓
	TWLEH	Write to End of Write	35	--	ns	↓
	TDVEH	Data Setup Time	25	--	ns	↓
	TEHDX	Data Hold Time	0	--	ns	↓

NOTES:
1. All devices tested at worst case temperature and supply voltage limits.
2. Typical derating = 5mA/MHz increase in ICCOP, VI = VCC or GND.
3. Tested at initial design and major design changes.
4. Input pulse levels: 0V to 3.V.Input rise and fall times: 5ns max. Input and output timing reference levels: 1.5V. Output load: 1 TTL gate equivalent and CL = 50 to 300pF. For CL greater than 50pF, access time is derated 0.15ns/pF.
5. Tested at VCC = 4.5V and 5.5V.

Absolute Maximum Ratings*

Supply Voltage (VCC-GND) .... -0.3 to 8.0V
Input or Output Voltage Applied .. GND -0.3V to VCC +0.3V
Storage Temperature .... -65°C to +150°C

Recommended Operating Conditions

Operating Supply Voltage .... 4.5V to 5.5V
Operating Temperature .... -40°C to +85°C

*CAUTION: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications (Note 1)

	SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB1	Standby Supply Current (CMOS)	--	50	μA	IO=0, $\bar{E}$=VCC-0.3V
	ICCSB	Standby Supply Current (TTL)	--	5	mA	IO=0, $\bar{E}$= 2.2V
	ICC	Enabled Supply Current	--	50	mA	IO=0, $\bar{E}$= 0.8V
	ICCOP	Operating Supply Current (Note 2)	--	50	mA	IO=0, $\bar{E}$= 0.8V, =1MHz
	ICCDR	Data Retention Supply Current	--	20	μA	VCC=2.0V, E=VCC
	ICCDR1	Data Retention Supply Current	--	30	μA	VCC=3.0V, $\bar{E}$=VCC
	II	Input Leakage Current	-1.0	+1.0	μA	VI=GND or VCC
	IOZ	Output Leakage Current	-1.0	+1.0	μA	VIO=GND or VCC
	VCCDR	Data Retention Supply Voltage	2.0	--	V	
	VOL	Output Low Voltage	--	0.4	V	IO=8.0mA
	VOH	Output High Voltage	2.4	--	V	IO=-4.0mA
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	2.2	VCC +0.3	V	
	CI	Input Capacitance (Note 3)	--	8	pF	VI=VCC or GND, f=1MHz
	CO	Output Capacitance (Note 3)	--	10	pF	VIO=VCC or GND, f=1MHz
⑤ A.C. READ CYCLE	TAVAX	Read Cycle Time	70	--	ns	(Note 4)
	TAVQV	Address Access Time	--	70	ns	(Note 4)
	TELQV	Chip Enable Access Time	--	70	ns	(Note 4)
	TELQX	Chip Enable Output Enable Time	5	--	ns	(Note 3)
	TEHQX	Chip Disable Output Hold Time	5	--	ns	(Note 3)
	TAXQX	Address Invalid Output Hold Time	5	--	ns	(Note 3)
	TEHQZ	Chip Disable Output Disable Time	--	30	ns	(Note 3)
WRITE CYCLE	TAVAX	Write Cycle Time	70	--	ns	(Note 4)
	TELWH	Chip Enable to End of Write	55	--	ns	↓
	TWLWH	Write Enable Pulse Width	40	--	ns	↓
	TAVWL	Address Setup Time	0	--	ns	↓
	TWHAX	Address Hold Time	0	--	ns	↓
	TDVWH	Data Setup Time	30	--	ns	↓
	TWHDX	Data Hold Time	0	--	ns	↓
	TWLQZ	Write Enable Output Disable Time	--	30	ns	(Note 3)
	TWHQX	Write Disable Output Enable Time	0	--	ns	(Note 3)
	TAVWH	Address Valid to End of Write	55	--	ns	(Note 4)
	TAVEL	Address Setup Time	0	--	ns	↓
	TEHAX	Address Hold Time	0	--	ns	↓
	TAVEH	Address Valid to End of Write	55	--	ns	↓
	TELEH	Enable Pulse Width	55	--	ns	↓
	TWLEH	Write to End of Write	40	--	ns	↓
	TDVEH	Data Setup Time	30	--	ns	↓
	TEHDX	Data Hold Time	0	--	ns	↓

NOTES:
1. All devices tested at worst case temperature and supply voltage limits.
2. Typical derating = 5mA/MHz increase in ICCOP, VI = VCC or GND.
3. Tested at initial design and major design changes.
4. Input pulse levels: 0V to 3.V. Input rise and fall times: 5ns max. Input and output timing reference levels: 1.5V. Output load: 1 TTL gate equivalent and CL = 50 to 300pF. For CL greater than 50pF, access time is derated 0.15ns/pF.
5. Tested at VCC = 4.5V and 5.5V.

Absolute Maximum Ratings*

Supply Voltage (VCC-GND) .... -0.3 to 8.0V
Input or Output Voltage Applied .. GND -0.3V to VCC +0.3V
Storage Temperature .... -65°C to +150°C

Recommended Operating Conditions

Operating Supply Voltage .... 4.5V to 5.5V
Operating Temperature .... -40°C to +85°C

*CAUTION: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications (Note 1)

	SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB1	Standby Supply Current (CMOS)	--	50	μA	IO=0, $\overline{E}$=VCC-0.3V
	ICCSB	Standby Supply Current (TTL)	--	5	mA	IO=0, $\overline{E}$= 2.2V
	ICC	Enabled Supply Current	--	50	mA	IO=0, $\overline{E}$=0.8V
	ICCOP	Operating Supply Current (Note 2)	--	50	mA	IO=0, $\overline{E}$=0.8V,f=1MHz
	ICCDR	Data Retention Supply Current	--	20	μA	VCC=2.0V, $\overline{E}$=VCC
	ICCDR1	Data Retention Supply Current	--	30	μA	VCC=3.0V, $\overline{E}$=VCC
	II	Input Leakage Current	-1.0	+1.0	μA	VI=GND or VCC
	IOZ	Output Leakage Current	-1.0	+1.0	μA	VIO=GND or VCC
	VCCDR	Data Retention Supply Voltage	2.0	-	V	
	VOL	Output Low Voltage	--	0.4	V	IO=8.0mA
	VOH	Output High Voltage	2.4	--	V	IO=-4.0mA
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	2.2	VCC+0.3	V	
	CI	Input Capacitance (Note 3)	--	8	pF	VI=VCC or GND, f=1MHz
	CO	Output Capacitance (Note 3)	--	10	pF	VIO=VCC or GND, f=1MHz
A.C. READ CYCLE	TAVAX	Read Cycle Time	85	--	ns	(Note 4)
	TAVQV	Address Access Time	--	85	ns	(Note 4)
	TELQV	Chip Enable Access Time	--	85	ns	(Note 4)
	TELQX	Chip Enable Output Enable Time	5	--	ns	(Note 3)
	TEHQX	Chip Disable Output Hold Time	5	--	ns	(Note 3)
	TAXQX	Address Invalid Output Hold Time	5	--	ns	(Note 3)
	TEHQZ	Chip Disable Output Disable Time	--	30	ns	(Note 3)
A.C. WRITE CYCLE	TAVAX	Write Cycle Time	85	--	ns	(Note 4)
	TELWH	Chip Enable to End of Write	65	--	ns	↓
	TWLWH	Write Enable Pulse Width	45	--	ns	↓
	TAVWL	Address Setup Time	0	--	ns	↓
	TWHAX	Address Hold Time	0	--	ns	↓
	TDVWH	Data Setup Time	35	--	ns	↓
	TWHDX	Data Hold Time	0	--	ns	↓
	TWLQZ	Write Enable Output Disable Time	--	30	ns	(Note 3)
	TWHQX	Write Disable Output Enable Time	0	--	ns	(Note 3)
	TAVWH	Address Valid to End of Write	65	--	ns	(Note 4)
	TAVEL	Address Setup Time	0	--	ns	↓
	TEHAX	Address Hold Time	0	--	ns	↓
	TAVEH	Address Valid to End of Write	65	--	ns	↓
	TELEH	Enable Pulse Width	65	--	ns	↓
	TWLEH	Write to End of Write	45	ns		↓
	TDVEH	Data Setup Time	35	--	ns	↓
	TEHDX	Data Hold Time	0	--	ns	↓

NOTES:
1. All devices tested at worst case temperature and supply voltage limits.
2. Typical derating = 5mA/MHz increase in ICCOP, VI = VCC or GND.
3. Tested at initial design and major design changes.
4. Input pulse levels: 0V to 3.V.Input rise and fall times: 5ns max. Input and output timing reference levels: 1.5V. Output load: 1 TTL gate equivalent and CL = 50 to 300pF. For CL greater than 50pF, access time is derated 0.15ns/pF.
5. Tested at VCC = 4.5V and 5.5V.

Absolute Maximum Ratings*

Supply Voltage (VCC-GND) .... -0.3 to 8.0V
Input or Output Voltage Applied .. GND -0.3V to VCC +0.3V
Storage Temperature .... -65°C to +150°C

Recommended Operating Conditions

Operating Supply Voltage .... 4.5V to 5.5V
Operating Temperature .... -40°C to +85°C

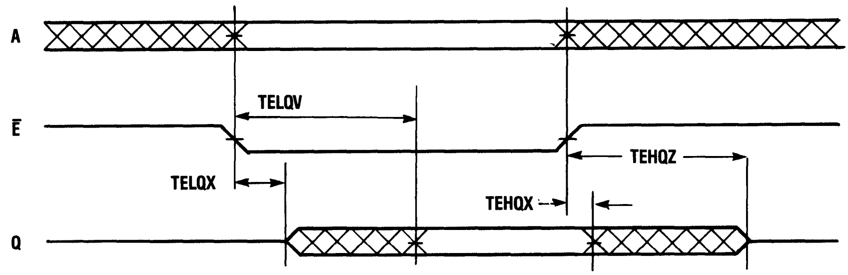
**CAUTION: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications (Note 1)

Group	SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB1	Standby Supply Current (CMOS)	--	900	μA	IO=0, $\overline{E}$=VCC-0.3V
	ICCSB	Standby Supply Current (TTL)	--	5	mA	IO=0, $\overline{E}$=2.2V
	ICC	Enabled Supply Current	--	50	mA	IO=0, $\overline{E}$=0.8V
	ICCOP	Operating Supply Current (Note 2)	--	50	mA	IO=0, $\overline{E}$=0.8V,f=1MHz
	ICCDR	Data Retention Supply Current	--	400	μA	VCC=2.0V, $\overline{E}$=VCC
	ICCDR1	Data Retention Supply Current	--	550	μA	VCC=3.0V, $\overline{E}$=VCC
	II	Input Leakage Current	-1.0	+1.0	μA	VI=GND or VCC
	IOZ	Output Leakage Current	-1.0	+1.0	μA	VIO=GND or VCC
	VCCDR	Data Retention Supply Voltage	2.0	--	V	
	VOL	Output Low Voltage	--	0.4	V	IO=8.0mA
	VOH	Output High Voltage	2.4	--	V	IO=-4.0mA
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	2.2	VCC +0.3	V	
	CI	Input Capacitance (Note 3)	--	8	pF	VI=VCC or GND, f=1MHz
	CO	Output Capacitance (Note 3)	--	10	pF	VIO=VCC or GND, f=1MHz
A.C. (5) READ CYCLE	TAVAX	Read Cycle Time	85	--	ns	(Note 4)
	TAVQV	Address Access Time	--	85	ns	(Note 4)
	TELQV	Chip Enable Access Time	--	85	ns	(Note 4)
	TELQX	Chip Enable Output Enable Time	5	--	ns	(Note 3)
	TEHQX	Chip Disable Output Hold Time	5	--	ns	(Note 3)
	TAXQX	Address Invalid Output Hold Time	5	--	ns	(Note 3)
	TEHQZ	Chip Disable Output Disable Time	--	30	ns	(Note 3)
A.C. (5) WRITE CYCLE	TAVAX	Write Cycle Time	85	--	ns	(Note 4)
	TELWH	Chip Enable to End of Write	65	--	ns	
	TWLWH	Write Enable Pulse Width	45	--	ns	
	TAVWL	Address Setup Time	0	--	ns	
	TWHAX	Address Hold Time	0	--	ns	
	TDVWH	Data Setup Time	35	--	ns	
	TWHDX	Data Hold Time	0	--	ns	↓
	TWLQZ	Write Enable Output Disable Time	--	30	ns	(Note 3)
	TWHQX	Write Disable Output Enable Time	0	--	ns	(Note 3)
	TAVWH	Address Valid to End of Write	65	--	ns	(Note 4)
	TAVEL	Address Setup Time	0	--	ns	
	TEHAX	Address Hold Time	0	--	ns	
	TAVEH	Address Valid to End of Write	65	--	ns	
	TELEH	Enable Pulse Width	65	--	ns	
	TWLEH	Write to End of Write	45	--	ns	
	TDVEH	Data Setup Time	35	--	ns	
	TEHDX	Data Hold Time	0	--	ns	↓

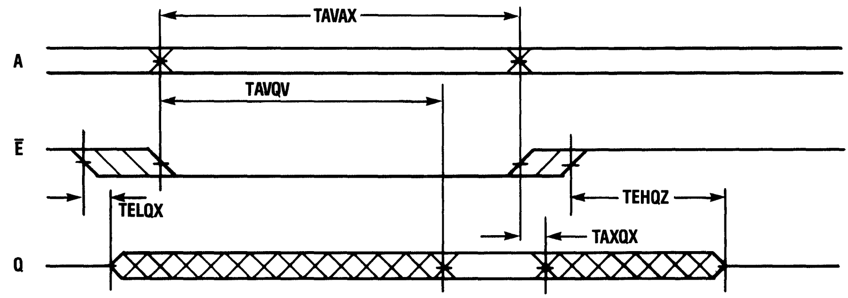
NOTES:
1. All devices tested at worst case temperature and supply voltage limits.
2. Typical derating = 5mA/MHz increase in ICCOP, VI = VCC or GND.
3. Tested at initial design and major design changes.
4. Input pulse levels: 0V to 3.V.Input rise and fall times: 5ns max. Input and output timing reference levels: 1.5V. Output load: 1 TTL gate equivalent and CL = 50 to 300pF. For CL greater than 50pF, access time is derated 0.15ns/pF.
5. Tested at VCC = 4.5V and 5.5V.

READ CYCLE 1: CONTROLLED BY $\overline{E}$



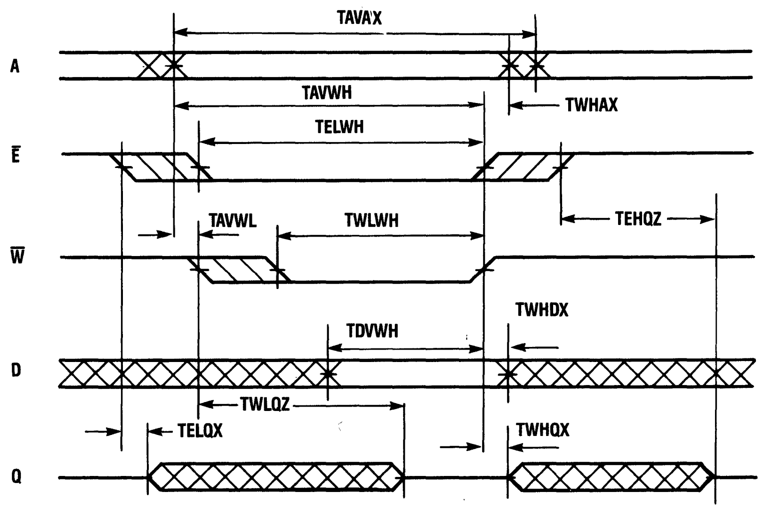
NOTE: $\overline{W}$ is held high for entire cycle and D is ignored. Address is stable by the time $\overline{E}$ goes low and remains valid until $\overline{E}$ goes high.

READ CYCLE 2: CONTROLLED BY ADDRESS



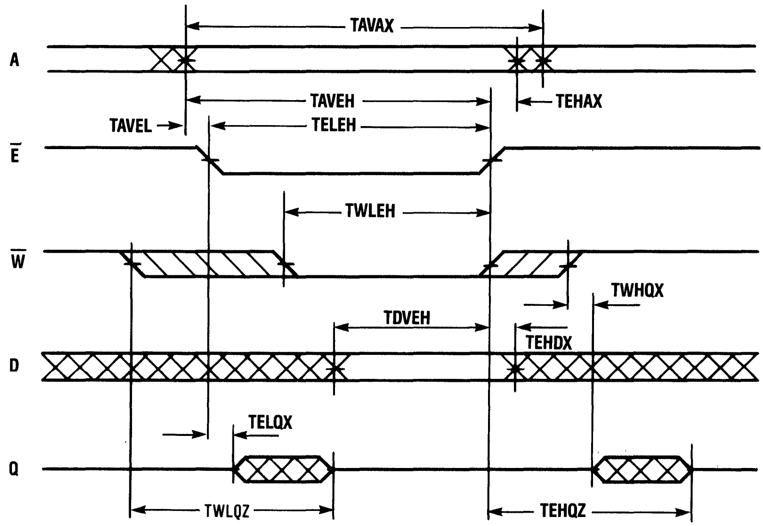
NOTE: $\overline{W}$ is high for the entire cycle and D is ignored. $\overline{E}$ is stable prior to A becoming valid and after A becomes invalid.

WRITE CYCLE 1 TIMING: CONTROLLED BY $\overline{W}$ (LATE WRITE)



NOTE: In this mode, $\overline{E}$ rises after $\overline{W}$. The address must remain stable whenever both $\overline{E}$ and $\overline{W}$ are low.

WRITE CYCLE 2 TIMING: CONTROLLED BY $\overline{E}$ (EARLY WRITE)



NOTE: In this mode, $\overline{W}$ rises after $\overline{E}$. If $\overline{W}$ falls before $\overline{E}$ by a time exceeding TWLQZ (Max) - TELQX (Min), and rises after $\overline{E}$ by a time exceeding TEHQZ (Max) - TWHQZ (Min), then $\overline{Q}$ will remain in the high impedance state throughout the cycle.

The address must remain stable whenever $\overline{E}$ and $\overline{W}$ are both low.

HARRIS

HM-65642

ADVANCE INFORMATION

8K x 8 Asynchronous CMOS Static RAM

HM-65642

Features

- **Full CMOS Design**
- **Six Transistor Memory Cell**
- **Low Standby Supply Current 250μA**
- **Low Operating Supply Current 80mA**
- **Fast Address Access Time 150ns**
- **Low Data Retention Supply Voltage 2.0V**
- **CMOS/TTL Compatible Inputs/Outputs**
- **JEDEC Approved Pinout**
- **Equal Cycle and Access Times**
- **No Clocks or Strobes Required**
- **Gated Inputs — No Pull-Up or Pull-Down Resistors Required**
- **Wide Temperature Range .... -55°C to +125°C**
- **Easy Microprocessor Interfacing**
- **Dual Chip Enable Control**

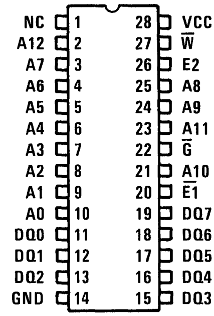
Description

The HM-65642 is a CMOS 8192 x 8 bit Static Random Access Memory. The pinout is the JEDEC 28 pin, 8 bit wide standard, which allows easy memory board layouts which accomodate a variety of industry standard ROM, PROM, EPROM, EEPROM and RAMs. The HM-65642 is ideally suited for use in microprocessor based systems. In particular, interfacing with the Harris 80C86 and 80C88 microprocessors is simplified by the convenient output enable (G̅) input.

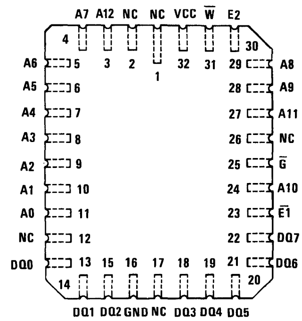
The HM-65642 is a full CMOS RAM which utilizes an array of six transistor (6T) memory cells for the most stable and lowest possible standby supply current over the full military temperature range. In addition to this, the high stability of the 6T RAM cell provides excellent protection against soft errors due to noise and alpha particles. This stability also improves the radiation tolerance of the RAM over that of four transistor or MIX-MOS (4T) devices.

Pinouts

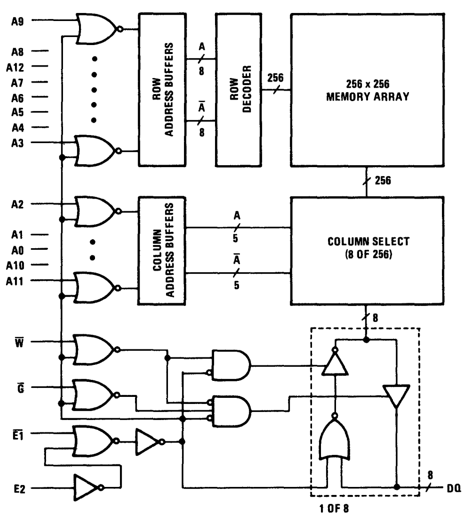
TOP VIEW



LCC
TOP VIEW



Functional Diagram



TRUTH TABLE

MODE	E̅1	E2	W̅	G̅
Standby (CMOS)	X	GND	X	X
Standby (TTL)	VIH	X	X	X
	X	VIL	X	X
Enable (High Z)	VIL	VIH	VIH	VIH
Write	VIL	VIH	VIL	X
Read	VIL	VIH	VIH	VIL

PIN DESCRIPTION

PIN	DESCRIPTION
A	Address Input
DQ	Data Input/Output
E̅1	Chip Enable
E2	Chip Enable
W̅	Write Enable
G̅	Output Enable

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings*

Supply Voltage (VCC-GND) ....-0.3 to 7.0V
Input or Output Voltage Applied..........-0.3 to VCC +0.3V
Storage Temperature..............................-65°C to +150°C

Recommended Operating Conditions

Supply Voltage (VCC) ....4.5V to 5.5V
Input Voltage High (VIH) .... 2.2 to VCC +0.3V
Input Voltage Low (VIL) ....-0.3V to +0.8V
Ambient Temperature HM-65642-8.......-55°C to +125°C
HM-65642-9.........-40°C to +85°C

**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

D.C. Electrical Specifications

PARAMETER	DESCRIPTION	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB1	Standby Supply Current (CMOS)		250	µA	E2 = GND, VCC = 5.5V
ICCSB2	Standby Supply Current (TTL)		10	mA	E2 = 0.8V or $\overline{E1}$ = 2.2V, VCC = 5.5V
ICCDR	Data Retention Supply Current		150	µA	E2 = GND, VCC = 2.0V
ICCEN	Enabled Supply Current		10	mA	E2 = 2.2V, $\overline{E1}$ = 0.8V, VCC = 5.5V, IIO = 0
ICCOP	Operating Supply Current (2)		20	mA	f = 1MHz, $\overline{E1}$ = 0.8V, E2 = 2.2V, VCC = 5.5V, IIO = 0
II	Input Leakage Current	-1	+1	µA	VIN = VCC or GND, VCC = 5.5V
IIOZ	Input/Output Leakage Current	-1	+1	µA	E2 = GND, VIO = VCC or GND, VCC = 5.5V
VCCDR	Data Retention Supply Voltage	2.0		V	E2 = GND
VOH	Output Voltage High	2.4		V	IOH =-1.0mA, VCC = 4.5V
VOL	Output Voltage Low		0.4	V	IOL = 4.0mA, VCC = 4.5V

Capacitance (Note 3)

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance	10	pF	f = 1MHz, VIN = VCC or GND
CIO	Input/Output Capacitance	12	pF	f = 1MHz, VIN = VCC or GND

NOTES:

1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns max; Input and output timing reference level: 1.5V; Ouput load: 1 TTL gate equivalent and CL = 50pF (Min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Typical derating: 5mA/MHz increase in ICCOP.
3. Tested at initial design and after major design changes - not 100% tested.

A.C. Electrical Specifications

PARAMETER		DESCRIPTION		MIN	MAX	UNITS	TEST CONDITIONS
READ CYCLE							
1 TAVAX	tRC	Read Cycle Time		150		ns	(Note 1, 4)
2 TAVQV	tAA	Address Access Time			150	ns	(Note 1, 4)
3 TE1LQV	tCE1	Chip Enable Access Time	$\overline{E1}$		150	ns	(Note 1, 4)
4 TE2HQV	tCE2		E2		150	ns	(Note 1, 4)
5 TGLQV	tOE	Output Enable Access Time			70	ns	(Note 1, 4)
6 TE1LQX	tLZ1	Chip Enable Valid to Output On	$\overline{E1}$	10		ns	(Note 2, 4)
7 TE2HQX	tLZ2		E2	10		ns	(Note 2, 4)
8 TGLQX	tOLZ	Output Enable Valid to Output On		5		ns	(Note 2, 4)
9 TE1HQZ	tHZ1	Chip Enable Not Valid to Output Off	$\overline{E1}$		50	ns	(Note 2, 4)
10 TE2LQZ	tHZ2		E2		60	ns	(Note 2, 4)
11 TGHQZ	tOHZ	Output Enable Not Valid to Output Off			50	ns	(Note 2, 4)
12 TAXQX	tOH	Output Hold From Address Change		10		ns	(Note 2, 4)
WRITE CYCLE							
13 TAVAX	tWC	Write Cycle Time		150		ns	(Note 1, 4)
14 TWLWH	tWP	Write Pulse Width		90		ns	(Note 1, 4)
15TE1LE1H	tCW	Chip Enable to End of Write	$\overline{E1}$	90		ns	(Note 1, 4)
16TE2HE2L	tCW		E2	90		ns	(Note 1, 4)
17 TAVWL	tAS	Address Setup Time	Late Write	0		ns	(Note 1, 4)
18 TAVE1L	tAS		Early Write, $\overline{E1}$	0		ns	(Note 1, 4)
19 TAVE2H	tAS		Early Write, E2	0		ns	(Note 1, 4)
20 TWHAX	tWR	Write Recovery Time	Late Write	10		ns	(Note 1, 4)
21 TE1HAX	tWR		Early Write, $\overline{E1}$	10		ns	(Note 1, 4)
22 TE2LAX	tWR		Early Write, E2	10		ns	(Note 1, 4)
23 TDVWH	tDW	Data Setup Time	Late Write	60		ns	(Note 1, 4)
24 TDVE1H	tDW		Early Write, $\overline{E1}$	60		ns	(Note 1, 4)
25 TDVE2L	tDW		Early Write, E2	60		ns	(Note 1, 4)
26 TWHDX	tDH	Data Hold Time	Late Write	5		ns	(Note 1, 4)
27 TE1HDX	tDH		Early Write, $\overline{E1}$	10		ns	(Note 1, 4)
28 TE2LDX	tDH		Early Write, E2	10		ns	(Note 1, 4)
29 TWLQZ	tWHZ	Write Enable Low to Output Off			50	ns	(Note 2, 4)
30 TWHQX	tOW	Write Enable High to Output On		5		ns	(Note 2, 4)

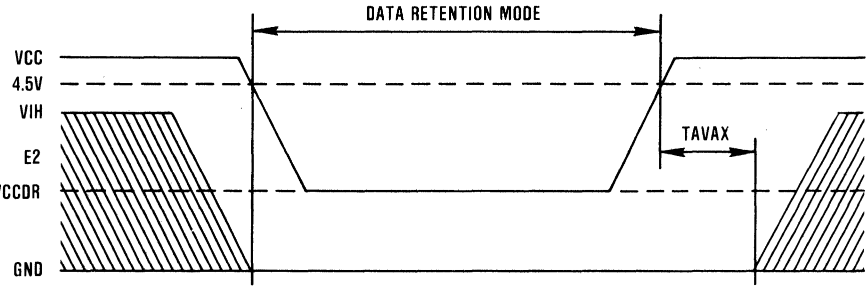
NOTES:

1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns max; Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent and CL = 50pF (min) — for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes — not 100% tested.
3. Typical derating: 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

Low Voltage Data Retention

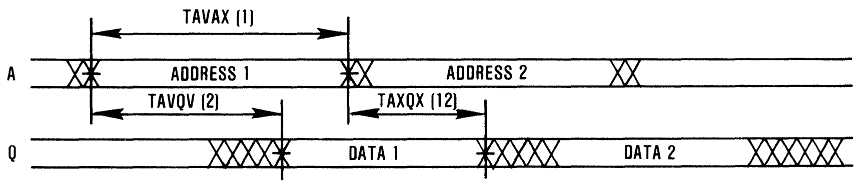
Harris CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over the operating temperature range. The following rules ensure data retention:

1. The RAM must be kept disabled during data retention. This is accomplished by holding the E2 pin between -0.3V and GND.
2. During power-up and power-down transitions, E2 must be held between -0.3V and 10% of VCC.
3. The RAM can begin operating one TAVAX after VCC reaches the minimum operating voltage of 4.5V

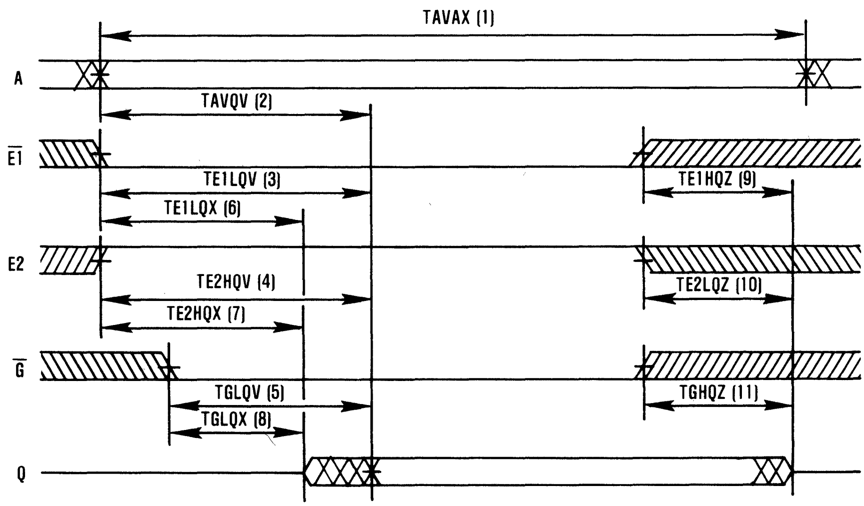


Read Cycles

READ CYCLE I: W̄, E2 HIGH; Ḡ, Ē1 LOW

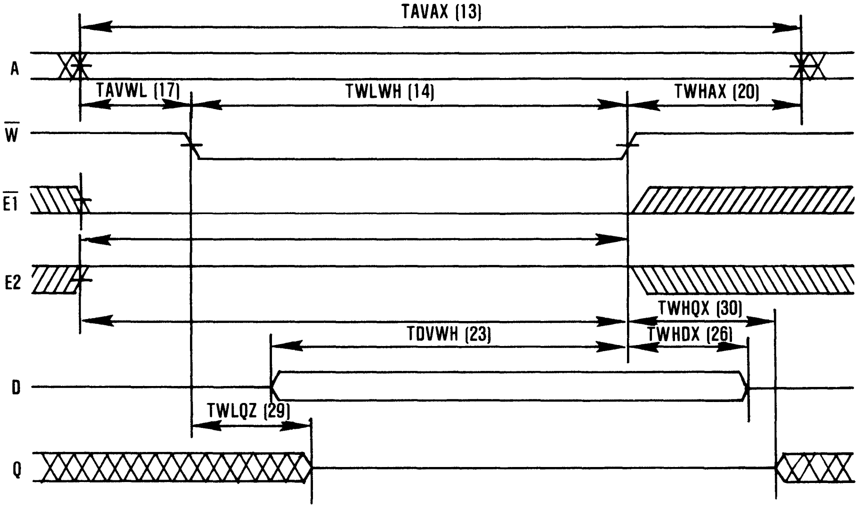


READ CYCLE II: W̄ HIGH

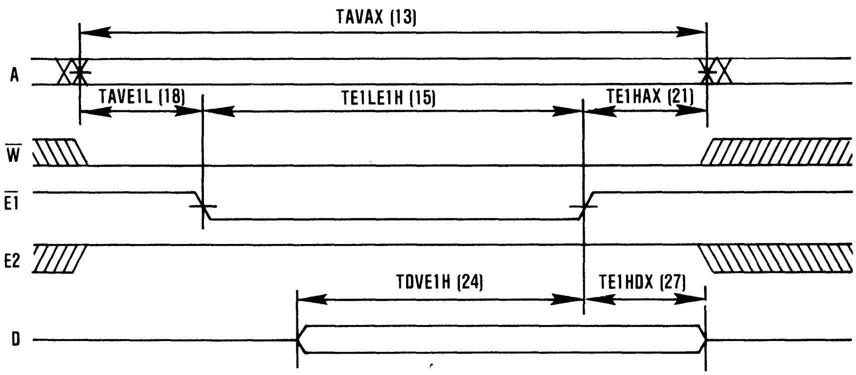


Write Cycles

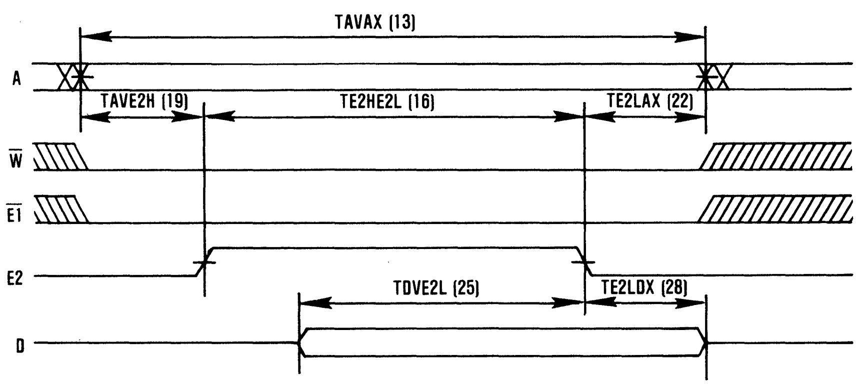
WRITE CYCLE I: LATE WRITE



WRITE CYCLE II: EARLY WRITE - CONTROLLED BY Ē1



WRITE CYCLE III: EARLY WRITE - CONTROLLED BY E2



HARRIS

HM-6564

8K x 8, 16K x 4 CMOS RAM

Features

- Low Power Standby .... 4mW Maximum
- Low Power Operation .... 280mW/MHz Maximum
- Data Retention .... 2.0V Minimum
- TTL Compatible In/Out
- Three State Outputs
- Fast Access Time .... 350ns Maximum
- Wide Operating Temperature Ranges
  - ▸ HM-6564-5 .... 0°C to +70°C
  - ▸ HM-6564-9 .... -40°C to +85°C
  - ▸ HM-6564-2/-8 .... -55°C to +125°C
- On Chip Address Registers
- Organizable 8K x 8 or 16K x 4
- 40 Pin DIP Pinout — 2.000" x 0.900"

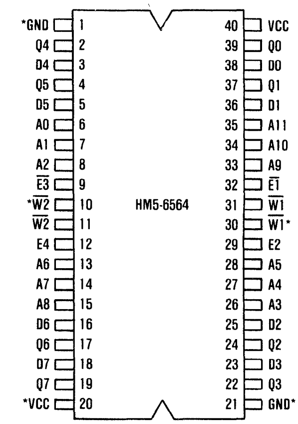
Description

The HM-6564 is a 64K bit CMOS RAM. It consists of 16 HM-6504 4K x 1 CMOS RAMs, in leadless carriers, mounted on a ceramic substrate. The HM-6564 is configured as an extra wide, standard length 40 pin DIP. The memory appears to the system as an array of 16 4K x 1 static RAMs. The array is organized as two 8K by 4 blocks of RAM sharing only the address bus. The data inputs, data outputs, chip enables and write enables are seperate for each block of RAM. This allows the user to organize the HM-6564 RAM as either an 8K by 8 or a 16K by 4 array.

This 64K memory provides a unique blend of low power CMOS semiconductor technology and advanced packaging techniques. The HM-6564 is intended for use in any application where a large amount of RAM is needed, and where power consumption and board space are prime concerns. The guaranteed low voltage data retention characteristics allow easy implementation of non-volatile read/write memory by using very small batteries mounted directly on the memory circuit board. Example applications include digital avionic instrumentation, remote data acquisition, and portable or hand held digital communications devices.

Pinout

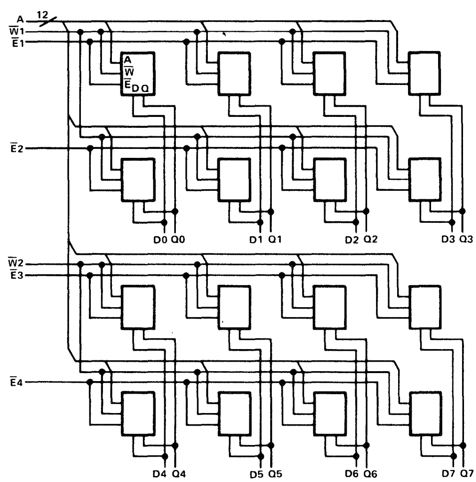
TOP VIEW



*NOTES:
Pins 20 and 40 (VCC) are internally connected. Similarly pins 1 and 21 (Ground) are connected. The user is advised to connect all four VCC pins and Ground pins to his board busses. This will improve power distribution across the array and will enhance decoupling.

Pin 10 is internally connected to pin 11, and pin 30 is connected to pin 31.

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Organization Guide

To Organize 8K x 8:

Connect: $\overline{E}1$ with $\overline{E}3$ (Pins 9 + 32)
$\overline{E}2$ with $\overline{E}4$ (Pins 12 + 29)
$\overline{W}1$ with $\overline{W}2$ (Pins 11 + 31)

To Organize 16K x 4:

Connect: Q0 with Q4 (Pins 2 + 39)
D0 with D4 (Pins 3 + 38)
Q1 with Q5 (Pins 4 + 37)
D1 with D5 (Pins 5 + 36)
D2 with D6 (Pins 16 + 25)
Q2 with Q6 (Pins 17 + 24)
D3 with D7 (Pins 18 + 23)
Q3 with Q7 (Pins 19 + 22)
Optional $\overline{W}1$ may be common with $\overline{W}2$ 11 (Pins 11 + 31)

Concerns for Proper Operation of Chip Enables:

The transition between blocks of RAM requires a change in the chip enable being used. When operating in the 8K x 8 mode, use the chip enables as if there were only two, $\overline{E}1$ and $\overline{E}2$. In the 16K x 4 mode, all chip enables must be treated separately. Transitions between chip enables must be treated with the same timing constraints that apply to any one chip enable. All chip enables must be high at least one chip enable high time (TEHEL) before any chip enable can fall. More than one chip enable low simultaneously, for devices whose outputs are tied common either internally or externally, is an illegal input condition and must be avoided.

Printed Circuit Board Mounting:

The leadless chip carrier packages used in the HM-6564 have conductive lids. These lids are electrically floating, not connected to VCC or GND. The designer should be aware of the possiblity that the carriers on the bottom side could short conductors below if pressed completely down against the surface of the circuit board. The pins on the package are designed with a standoff feature to help prevent the leadless carriers from touching the circuit board surface.

Board Size Tradeoffs

Printed circuit board real estate is a costly commodity. Actual board costs depend on layout tolerances, density, complexity, number of layers, choice of board material, and other factors.

The following table compares board space for 16 standard DIP 4K RAMs to the HM-6564 RAM array. Both fine line, close tolerance layout and standard "easy" layout board sizes are shown in the comparison.

64K ARRAY OR 16 4K RAMs ON A PC BOARD vs. THE HM-6563

PACKAGE	CIRCUIT SUBSTRATE	SIZE
18 Pin DIP	Standard Two Sided PCB	12 to 15 square inch
18 Pin DIP	Fine Line or Multilayer PCB	9 to 11 square inch
18 Pin Leadless Carrier	Multilayer Alumina Substrate	3 to 5 square inch
HM-6564	Two Sided Mounting Multilayer Alumina Substrate	2 square inch

The cost of semiconductor circuits decline with time. If actual costs were included, they would be out of date in a very short time. We urge you to contact your local Harris office of sales representative for accurate pricing allowing cost tradeoff analysis. In your cost analysis, also consider the advantages of a lighter, smaller overall package for your system. Consider how much more valuable your system will be when the memory array size is decreased to about 1/6 of normal size.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) .... -0.3V to +8.0V
Input or Output Voltage Applied .... (GND -0.3V) to (VCC +0.3V)
Storage Temperature .... -65°C to +150°C

Operating Range

Operating Supply Voltage
HM-6564-2/-8 .... 4.5V to 5.5V
Operating Temperature
HM-6564-2/-8 .... -55°C to +125°C

*CAUTION: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications ①

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		800	μA	IO = 0, VI = VCC or GND
	ICCOP1	Operating Supply Current (8K x 8) ②		56	mA	$\overline{E}$ = 1MHz, IO = 0, VI = VCC or GND
	ICCOP2	Operating Supply Current (16K x 4) ② ③		28	mA	$\overline{E}$ = 1MHz, IO = 0, VI = VCC or GND
	ICCDR	Data Retention Supply Current		400	μA	IO = 0, VCC = 2.0, VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		V	
	IIA	Address Input Leakage	-20	+20	μA	VI = VCC or GND
	IID1	Data Input Leakage (8K x 8)	-3	+3	μA	VI = VCC or GND
	IID2	Data Input Leakage (16K x 4) ③	-5	+5	μA	VI = VCC or GND
	IIE1	Enable Input Leakage (8K x 8)	-10	+10	μA	VI = VCC or GND
	IIE2	Enable Input Leakage (16K x 4) ③	-5	+5	μA	VI = VCC or GND
	IIW	Write Enable Input Leakage (Each)	-10	+10	μA	VI = VCC or GND
	IOZ1	Output Leakage (8K x 8)	-5	+5	μA	VO = VCC or GND
	IOZ2	Output Leakage (16Kx4) ③	-10	+10	μA	VO = VCC or GND
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	VCC-2.0	VCC+0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		V	IO = -1.0mA
	CIA	Address Input Capacitance ③		200	pF	f = 1MHz, VI = VCC or GND
	CID1	Data Input Capacitance (8K x 8) ③		50	pF	f = 1MHz, VI = VCC or GND
	CID2	Data Input Capacitance (16K x 4) ③		100	pF	f = 1MHz, VI = VCC or GND
	CIE1	Enable Input Capacitance (8K x 8) ③		160	pF	f = 1MHz, VI = VCC or GND
	CIE2	Enable Input Capacitance (16K x 4) ③		80	pF	f = 1MHz, VI = VCC or GND
	CIW	Write Enable Input Capacitance (Each) ③		100	pF	f = 1MHz, VI = VCC or GND
	CO1	Output Capacitance (8K x 8) ③		50	pF	f = 1MHz, VO = VCC or GND
	CO2	Output Capacitance (16K x 4) ③		100	pF	f = 1MHz, VO = VCC or GND

NOTES:
① All devices tested at worst case temperature and V_{CC}.
② Operating supply current (ICCOP) is proportional to operating frequency. ICCOP is specified at an operating frequency of 1MHz, indicating repetitive accessing at a 1μs rate. Operation at slower rates will decrease ICCOP proportionally.
③ Tested at initial design and after major design changes.
④ Input rise and fall times: 20ns max. Input and output timing reference level: 1.5V. Output load: C_L = 50 to 300pF. For C_L greater than 50pF, access time is derated 0.15ns/pF.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) ....-0.3V to +8.0V
Input or Output Voltage Applied .... (GND -0.3V) to (VCC +0.3V)
Storage Temperature ....-65°C to +150°C

Operating Range

Operating Supply Voltage
HM-6564-9 ....4.5V to 5.5V
Operating Temperature
HM-6564-9 ....-40°C to +85°C

*CAUTION: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications ①

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		800	μA	IO = 0 VI = VCC or GND
	ICCOP1	Operating Supply Current (8K x 8) ②		56	mA	Ē = 1MHz, IO = 0 VI = VCC or GND
	ICCOP2	Operating Supply Current (16K x 4) ②③		28	mA	Ē = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		400	μA	IO = 0, VCC = 2.0, VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		V	
	IIA	Address Input Leakage	-20	+20	μA	VI = VCC or GND
	IID1	Data Input Leakage (8K x 8)	-3	+3	μA	VI = VCC or GND
	IID2	Data Input Leakage ③ (16K x 4)	-5	+5	μA	VI = VCC or GND
	IIE1	Enable Input Leakage (8K x 8)	-10	+10	μA	V = VCC or GND
	IIE2	Enable Input Leakage ③ (16K x 4)	-5	+5	μA	VI = VCC or GND
	IIW	Write Enable Input Leakage (Each)	-10	+10	μA	VI = VCC or GND
	IOZ1	Output Leakage (8K x 8)	-5	+5	μA	VO = VCC or GND
	IOZ2	Output Leakage (16K x 4) ③	-10	+10	μA	VO = VCC or GND
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	VCC-2.0	VCC+0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		V	IO = -1.0mA
	CIA	Address Input Capacitance ③		200	pF	f = 1MHz, VI = VCC or GND
	CID1	Data Input Capacitance (8K x 8) ③		50	pF	f = 1MHz, VI = VCC or GND
	CID2	Data Input Capacitance (16K x 4) ③		100	pF	f = 1MHz, VI = VCC or GND
	CIE1	Enable Input Capacitance (8K x 8) ③		160	pF	f = 1MHz, VI = VCC or GND
	CIE2	Enable Input Capacitance (16K x 4) ③		80	pF	f = 1MHz, VI = VCC or GND
	CIW	Write Enable Input Capacitance (Each) ③		100	pF	f = 1MHz, VI = VCC or GND
	CO1	Output Capacitance (8K x 8) ③		50	pF	f = 1MHz, VO = VCC or GND
	CO2	Output Capacitance (16K x 4) ③		100	pF	f = 1MHz, VO = VCC or GND

NOTES:
① All devices tested at worst case temperature and V_{CC}.
② Operating supply current (ICCOP) is proportional to operating frequency. ICCOP is specified at an operating frequency of 1MHz, indicating repetitive accessing at a 1μs rate. Operation at slower rates will decrease ICCOP proportionally.
③ Tested at initial design and after major design changes.
④ Input rise and fall times: 20ns max. Input and output timing reference level: 1.5V. Output load: C_L = 50 to 300pF. For C_L greater than 50pF, access time is derated 0.15ns/pF.

Electrical Specifications ①

A.C.

SYMBOL	PARAMETER	TEMP & VCC = OPERATING RANGE MIN	MAX	UNITS	TEST CONDITIONS
TELQV	Chip Enable Access		350	ns	④
TAVQV	Address Access (TAVQV=TELQV+TAVEL)		400	ns	④
TELQX	Output Enable	20		ns	③ ④
TEHQZ	Output Disable		120	ns	③ ④
TELEL	Read or Write Cycle	480		ns	④
TELEH	Chip Enable Low	350		ns	④
TEHEL	Chip Enable High	130		ns	④
TAVEL	Address Setup	50		ns	④
TELAX	Address Hold	50		ns	④
TWLWH	Write Enable Low	150		ns	④
TWLEH	Write Enable Setup	250		ns	④
TWLEL	Early Write Setup (Write Mode)	10		ns	④
TELWH	Early Write Hold (Write Mode)	100		ns	④
TDVWL	Data Setup	10		ns	④
TDVEL	Early Write Data Setup	10		ns	④
TWLDX	Data Hold	100		ns	④
TELDX	Early Write Data Hold	100		ns	④

NOTES:
① All devices tested at worst case temperature and V_{CC}.
② Operating supply current (ICCOP) is proportional to operating frequency. ICCOP is specified at an operating frequency of 1MHz, indicating repetitive accessing at a 1μs rate. Operation at slower rates will decrease ICCOP proportionally.
③ Tested at initial design and after major design changes.
④ Input rise and fall times: 20ns max. Input and output timing reference level: 1.5V. Output load: C_L = 50 to 300pF. For C_L greater than 50pF, access time is derated 0.15ns/pF.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) ....-0.3V to +8.0V
Input or Output Voltage Applied.................. (GND -0.3V) to (VCC +0.3V)
Storage Temperature..............................-65°C to +150°C

Operating Range

Operating Supply Voltage
HM-6564-5 .... 4.5V to 5.5V
Operating Temperature
HM-6564-5 .... 0°C to +70°C

*CAUTION: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications ①

D.C.

SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current		5.6	mA	IO = 0, VI = VCC or GND
ICCOP1	Operating Supply Current (8K x 8) ②		60	mA	$\overline{E}$ =1MHz, IO = 0 VI = VCC or GND
ICCOP2	Operating Supply Current (16K x 4) ②③		30	mA	$\overline{E}$ =1MHz, IO = 0 VI = VCC or GND
ICCDR	Data Retention Supply Curr.		3.2	mA	VCC = 2.0, IO = 0 VI = VCC or GND
VCCDR	Data Retention Supply V.	2.0		V	
IIA	Address Input Leakage	-20	+20	µA	VI = VCC or GND
IID1	Data Input Leakage (8K x 8)	-3	+3	µA	VI = VCC or GND
IID2	Data Input Leakage ③ (16K x 4)	-5	+5	µA	VI = VCC or GND
IIE1	Enable Input Leakage (8K x 8)	-10	+10	µA	VI = VCC or GND
IIE2	Enable Input Leakage ③ (16K x 4)	-5	+5	µA	VI = VCC or GND
IIW	Write Enable Input Leakage (Each)	-10	+10	µA	VI = VCC or GND
IOZ1	Output Leakage (8K x 8)	-5	+5	µA	VO = VCC or GND
IOZ2	Output Leakage (16Kx4) ③	-10	+10	µA	VO = VCC or GND
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	VCC -2.0	VCC +0.3	V	
VOL	Output Low Voltage		0.4	V	IO = 1.6mA
VOH	Output High Voltage	2.4		V	IO = -0.4mA
CIA	Address Input Capacitance ③		200	pF	f = 1MHz, VI = VCC or GND
CID1	Data Input Capacitance (8K x 8) ③		50	pF	f = 1MHz, VI = VCC or GND
CID2	Data Input Capacitance (16K x 4) ③		100	pF	f = 1MHz, VI = VCC or GND
CIE1	Enable Input Capacitance (8K x 8) ③		160	pF	f = 1MHz, VI = VCC or GND
CIE2	Enable Input Capacitance (16K x 4) ③		80	pF	f = 1MHz, VI = VCC or GND
CIW	Write Input Capacitance (Each) ③		100	pF	f = 1MHz, VI = VCC or GND
CO1	Output Capacitance (8K x 8) ③		50	pF	f = 1MHz, VO= VCC or GND
CO2	Output Capacitance (16K x 4) ③		100	pF	f = 1MHz, VO = VCC or GND

NOTES: ① All devices tested at worst case temperature and V_{CC}.
② Operating supply current (ICCOP) is proportional to operating frequency. ICCOP is specified at an operating frequency of 1MHz, indicating repetitive accessing at a 1µs rate. Operation at slower rates will decrease ICCOP proportionally.
③ Tested at initial design and after major design changes.
④ Input rise and fall times: 20ns max. Input and output timing reference level: 1.5V. Output load: C_L = 50 to 300pF. For C_L greater than 50pF, access time is derated 0.15ns/pF.

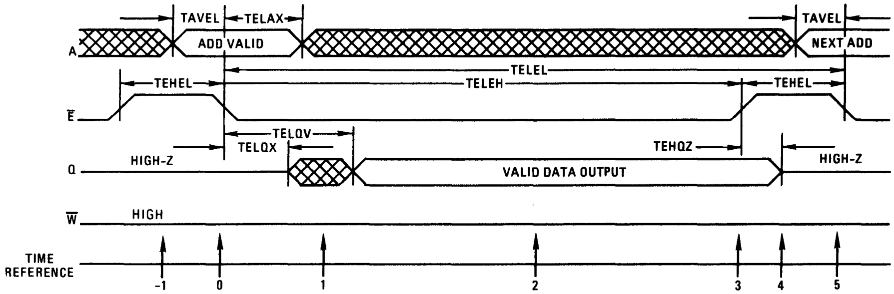
Electrical Specifications ①

A.C.

SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	MAX	UNITS	TEST CONDTIONS
TELQV	Chip Enable Access		450	ns	④
TAVQV	Address Access (TAVQV=TELQV+TAVEL)		500	ns	④
TELQX	Output Enable	20		ns	③ ④
TEHQZ	Output Disable		150	ns	③ ④
TELEL	Read or Write Cycle	600		ns	④
TELEH	Chip Enable Low	450		ns	④
TEHEL	Chip Enable High	150		ns	④
TAVEL	Address Setup	50		ns	④
TELAX	Address Hold	50		ns	④
TWLWH	Write Enable Low	150		ns	④
TWLEH	Write Enable Setup	250		ns	④
TWLEL	Early Write Setup (Write Mode)	10		ns	④
TELWH	Early Write Hold (Write Mode)	100		ns	④
TDVWL	Data Setup	10		ns	④
TDVEL	Early Write Data Setup	10		ns	④
TWLDX	Data Hold	100		ns	④
TELDX	Early Write Data Hold	100		ns	④

NOTES:
① All devices tested at worst case temperature and V_{CC}.
② Operating supply current (ICCOP) is proportional to operating frequency. ICCOP is specified at an operating frequency of 1MHz, indicating repetitive accessing at a 1µs rate. Operation at slower rates will decrease ICCOP proportionally.
③ Tested at initial design and after major design changes.
④ Input rise and fall times: 20ns max. Input and output timing reference level: 1.5V. Output load: C_L = 50 to 300pF. For C_L greater than 50pF, access time is derated 0.15ns/pF.

Read Cycle

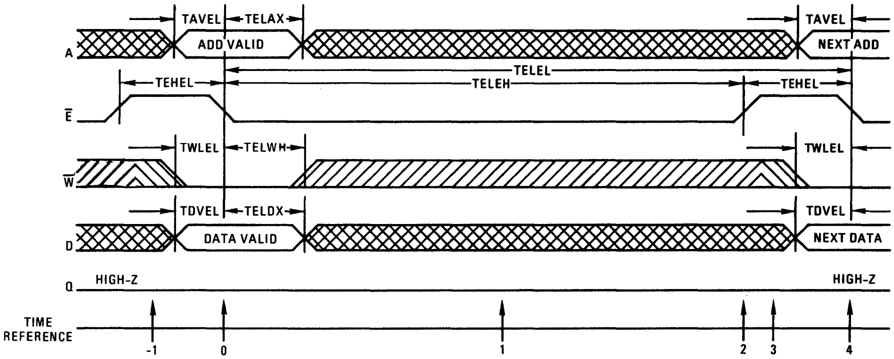


TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	A	OUTPUT Q	FUNCTION
-1	H	X	X	Z	Memory Disabled
0	↓	H	V	Z	Cycle Begins, Addresses are Latched
1	L	H	X	X	Output Enabled
2	L	H	X	V	Output Valid
3	↑	H	X	V	Read Accomplished
4	H	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↓	H	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The address information is latched in the on chip registers on the falling edge of Ē (T = 0). Minimum address set up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but data is not valid until during time (T = 2). W̄ must remain high until after time (T = 2). After the output data has been read, Ē may return high (T = 3). This will disable the output buffer and ready the RAM for the next memory cycle (T = 4).

Early Write Cycle

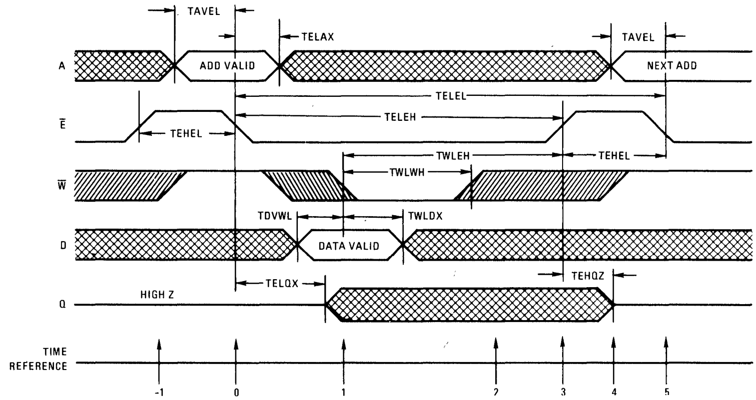


TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	Memory Disabled
0	↓	L	V	V	Z	Cycle Begins, Addresses are Latched
1	L	X	X	X	Z	Write in Progress Internally
2	↑	X	X	X	Z	Write Complete
3	H	X	X	X	Z	Prepare for Next Cycle (Same as -1)
4	↓	L	V	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The early write cycle is the only cycle where the output is guaranteed not to become active. On the falling edge of Ē (T = 0), the addresses, the write signal, and the data input are latched in on chip registers. The logic value of W at the time Ē falls determines the state of the output buffer for the cycle. Since W̄ is low when Ē falls, the output buffer is latched into the high impedance state and will remain in that state until Ē returns high (T = 2). For this cycle, the data input is latched by Ē going low; therefore data set up and hold times should be referenced to Ē. When Ē (T = 2) returns to the high state the output buffer disables and all signals are unlatched. The device is now ready for the next cycle.

Late Write Cycle



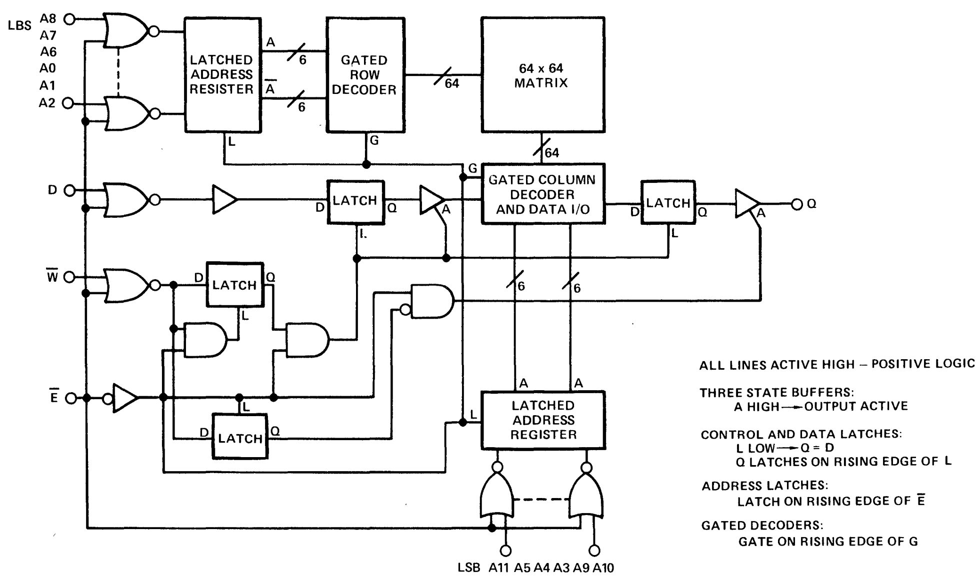
TRUTH TABLE

TIME REFERENCE	INPUTS Ē	W̄	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	Z	Memory Disabled
0	↓	H	V	X	Z	Cycle Begins, Addresses are Latched
1	L	↓	X	V	X	Write Begins, Data is Latched
2	L	H	X	X	X	Write in Progress Internally
3	↑	H	X	X	X	Write Completed
4	H	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↓	H	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The late write cycle is a cross between the early write cycle and the read-modify-write cycle. Recall that in the early write the output is guaranteed to remain high impedance, and in the read-modify-write the output is guaranteed valid at access time. The late write is between these two cases. With this cycle the output may become active, and may become valid data, or may remain active but undefined. Valid data is written into the RAM if data set up, data hold, write setup and write pulse widths are observed.

NOTES: In the above descriptions the numbers in parenthesis (T = n) refers to the respective timing diagrams. The numbers are located on the time reference line below each diagram. The timing diagrams shown are only examples and are not the only valid method of operation.

HM-6504 (One of Sixteen)



HARRIS HM-8808/08A

ADVANCE INFORMATION

8K x 8 Asynchronous CMOS Static RAM Module

Features

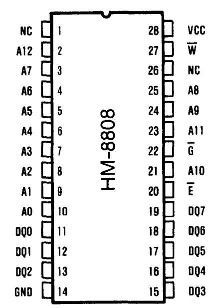
- Full CMOS Design
- 6 Transistor Memory Cell
- Low Standby Current 250/900μA
- Low Operating Current 70mA
- Fast Address Access Time 100/120/150ns
- Low Voltage Data Retention 2.0V
- CMOS/TTL Compatible Inputs/Outputs
- JEDEC Approved Pinout
- Equal Cycle and Access Time
- No Clocks or Strobes Required
- Single 5 Volt Supply
- Gated Inputs — No Pull-Up or Pull-Down Resistors Required
- Wide Temperature Range .... -55°C to +125°C
- Easy Microprocessor Interfacing
- Dual Chip Enable Control (HM-8808A)

Description

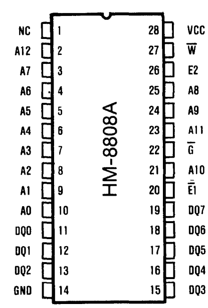
The HM-8808 and HM-8808A are 8K x 8 Asynchronous CMOS Static RAM Modules, based on multi-layered, co-fired, dual-in-line substrates. Mounted on each substrate are four HM-65162 2K x 8 CMOS SRAMS, a high speed CMOS decoder, and a ceramic decoupling capacitor, all packaged in leadless chip carriers. The capacitor is added to reduce noise and the need for external decoupling. The HM-65162 RAMs used in these modules are full CMOS devices, utilizing arrays of six transistor (6T) memory cells for the most stable and lowest possible standby supply current over the full military temperature range. In addition to this, the high stability of the 6T cell provides excellent protection against soft errors due to noise and alpha particles. This stability also improves the radiation tolerance of the RAM over that of four transistor devices. The HM-8808 and HM-8808A have gated inputs to simplify system design for optimum standby supply current. The pinouts of these modules conform to the JEDEC 28-pin 8-bit wide standard, which is compatible with a variety of industry standard memories. The HM-8808A is pin-compatible with many standard 8K x 8 RAMs, adding the advantage of high performance over the full military temperature range. Also, because of the second chip enable (E2), the HM-8808A simplifies the design of low-power battery back-up memory systems.

Pinouts

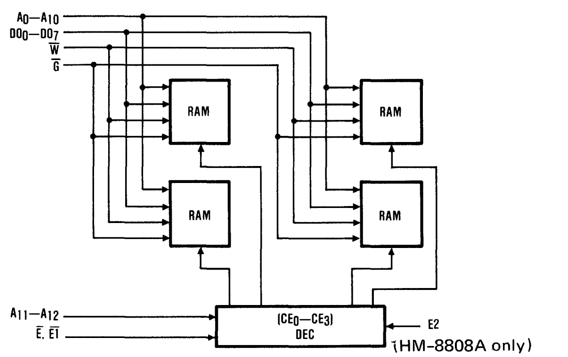
TOP VIEW



TOP VIEW



Functional Diagram



PIN DESCRIPTION

PIN	DESCRIPTION
A	Address Input
DQ	Data Input/Output
$\overline{E}$	Chip Enable (HM-8808)
$\overline{E1}$	Chip Enable (HM-8808A)
E2	Chip Enable (HM-8808A)
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable

SELECTION GUIDE

PART NUMBER	TELQV	ICCSB
HM-8808S/HM-8808AS	100ns	250μA
HM-8808B/HM-8808AB	120ns	250μA
HM-8808 /HM-8808A	150ns	900μA

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
Specifications are subject to change without notice.

Absolute Maximum Ratings*

Supply Voltage (VCC-GND) .... -0.3 to 8.0V
Input or Output Voltage Applied .... GND -0.3V to VCC +0.3V
Storage Temperature .... -65°C to +150°C

Recommended Operating Conditions

Operating Supply Voltage .... 4.5V to 5.5V
Op. Temp. HM-8808S/AS-8 .... -55°C to +125°C
HM-8808S/AS-9 .... -40°C to +85°C

**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications (Note 1)

	SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB1	Standby Supply Current (CMOS)	—	250	μA	IO=0, $\overline{E}$=VCC-0.3V (7), E2=0.3V (8)
	ICCSB	Standby Supply Current (TTL)	—	35	mA	IO=0, $\overline{E}$=VIH (7), E2=VIL (8)
	ICC	Enabled Supply Current	—	60	mA	IO=0, $\overline{E}$=VIL (7), E2=VIH (8)
	ICCOP	Operating Supply Current	—	70	mA	IO=0, f=1MHz, $\overline{E}$=VIL (7), E2=VIH (8) (2)
	ICCDR	Data Retention Supply Current	—	125	μA	VCC=2.0V, $\overline{E}$=VCC-0.3V (7), E2=0.3V (8)
	II	Input Leakage Current	-1.0	+1.0	μA	VI = GND or VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	μA	VIO = GND or VCC
	VCCDR	Data Retention Supply Voltage	2.0	—	V	VCC=2.0V, $\overline{E}$=VCC (7), E2=GND (8)
	VOL	Output Low Voltage	—	0.4	V	IO=4.0mA
	VOH	Output High Voltage	2.4	—	V	IO=-1.0mA
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	2.4	VCC+0.3	V	
	CI	Input Capacitance: $\overline{G}$, A	—	35	pF	VI=VCC or GND, f=1MHz (3)
	CIO	Input/Output Capacitance	—	43	pF	VIO=VCC or GND, f=1MHz (3)
	CE	Enable Input Capacitance	—	15	pF	VE=VCC or GND, f=1MHz (3)
	CW	Write Enable Capacitance	—	48	pF	VW=VCC or GND, f=1MHz (3)
READ CYCLE	TAVAX	Read Cycle Time	100	—	ns	
	TAVQV	Address Access Time	—	100	ns	
	TELQV	Chip Enable Access Time	—	100	ns	(5)
	TGLQV	Output Enable Access Time	—	50	ns	
	TELQX	Chip Enable Output Enable Time	20	—	ns	(3) (5)
	TGLQX	Output Enable Output Enable Time	5	—	ns	(3)
	TAXQX	Address Output Hold Time	5	—	ns	
	TEHQZ	Chip Disable Output Disable Time	0	60	ns	(3) (6)
(Note 4) A.C.	TGHQZ	Output Disable Time	0	40	ns	(3)
WRITE CYCLE	TAVAX	Write Cycle Time	100	—	ns	
	TELWH	Chip Enable to End of Write	70	—	ns	(5)
	TWLWH	Write Enable Pulse Width	40	—	ns	
	TELEH	Enable Pulse Width (Early Write)	TBD	—	ns	(3) (5) (6)
	TAVWL	Address Setup Time (Late Write)	15	—	ns	
	TAVEL	Address Setup Time (Early Write)	TBD	—	ns	(3) (5)
	TWHAX	Address Hold Time (Late Write)	10	—	ns	
	TEHAX	Address Hold Time (Early Write)	TBD	—	ns	(3)
	TDVWH	Data Setup Time (Late Write)	30	—	ns	
	TDVEH	Data Setup Time (Early Write)	30	—	ns	(6)
	TWHDX	Data Hold Time (Late Write)	10	—	ns	
	TEHDX	Data Hold Time (Early Write)	25	—	ns	(6)
	TWLEH	Write Enable Pulse Setup Time	40	—	ns	(6)
	TWLQZ	Write Enable Output Disable Time	—	40	ns	(3)
	TWHQX	Write Disable Output Enable Time	0	—	ns	(3)

NOTES:
1. All devices tested at worst case temperature and supply voltage limits.
2. Typical derating = 5mA/MHz increase in ICCOP, VI = VCC or GND.
3. Tested at initial design and after major design changes.
4. Input pulse levels: VIL = 0.0V, VIH = 3.0V
   Input rise and fall times: 5ns (max.)
   Input and output timing reference levels: 1.5V
   Output load: 1 TTL gate equivalent and 50pF (min, including scope and jig).
5. "EL" (enable input valid) equivalent to:
   EL on the HM-8808. EIL and E2H on the HM-8808A.
6. "EH" (enable input invalid) equivalent to:
   EH on the HM-8808. EIH or E2L on the HM-8808A.
7. Relevant to the HM-8808 only.
8. Relevant to the HM-8808A only.

Absolute Maximum Ratings*

Supply Voltage (VCC-GND) .... -0.3 to 8.0V
Input or Output Voltage Applied .... GND -0.3V to VCC +0.3V
Storage Temperature .... -65°C to +150°C

Recommended Operating Conditions

Operating Supply Voltage .... 4.5V to 5.5V
Op. Temp. HM-8808B/AB-8 .... -55°C to +125°C
HM-8808B/AB-9 .... -40°C to +85°C

**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications (Note 1)

	SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB1	Standby Supply Current (CMOS)	—	250	μA	IO=0, Ē=VCC-0.3V ⑦, E2=0.3V ⑧
	ICCSB	Standby Supply Current (TTL)	—	35	mA	IO=0, Ē=VIH ⑦, E2=VIL ⑧
	ICC	Enabled Supply Current	—	60	mA	IO=0, Ē=VIL ⑦, E2=VIH ⑧
	ICCOP	Operating Supply Current	—	70	mA	IO=0, f=1MHz, Ē=VIL ⑦, E2=VIH ⑧ ②
	ICCDR	Data Retention Supply Current	—	125	μA	VCC=2.0V, Ē=VCC-0.3V ⑦, E2=0.3V ⑧
	II	Input Leakage Current	-1.0	+1.0	μA	VI = GND or VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	μA	VIO = GND or VCC
	VCCDR	Data Retention Supply Voltage	2.0	—	V	VCC=2.0V, Ē=VCC ⑦, E2=GND ⑧
	VOL	Output Low Voltage	—	0.4	V	IO=4.0mA
	VOH	Output High Voltage	2.4	—	V	IO=-1.0mA
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	2.4	VCC+0.3	V	
	CI	Input Capacitance: G̅, A	—	35	pF	VI=VCC or GND, f=1MHz ③
	CIO	Input/Output Capacitance	—	43	pF	VIO=VCC or GND, f=1MHz ③
	CE	Enable Input Capacitance	—	15	pF	VE=VCC or GND, f=1MHz ③
	CW	Write Enable Capacitance	—	48	pF	VW=VCC or GND, f=1MHz ③
READ CYCLE	TAVAX	Read Cycle Time	120	—	ns	
	TAVQV	Address Access Time	—	120	ns	
	TELQV	Chip Enable Access Time	—	120	ns	⑤
	TGLQV	Output Enable Access Time	—	65	ns	
	TELQX	Chip Enable Output Enable Time	20	—	ns	③ ⑤
	TGLQX	Output Enable Output Enable Time	5	—	ns	③
	TAXQX	Address Output Hold Time	5	—	ns	
	TEHQZ	Chip Disable Output Disable Time	0	70	ns	③ ⑥
(Note 4) A.C.	TGHQZ	Output Disable Time	0	40	ns	③
WRITE CYCLE	TAVAX	Write Cycle Time	120	—	ns	
	TELWH	Chip Enable to End of Write	80	—	ns	⑤
	TWLWH	Write Enable Pulse Width	55	—	ns	
	TELEH	Enable Pulse Width (Early Write)	TBD	—	ns	③ ⑤ ⑥
	TAVWL	Address Setup Time (Late Write)	15	—	ns	
	TAVEL	Address Setup Time (Early Write)	TBD	—	ns	③ ⑤
	TWHAX	Address Hold Time (Late Write)	10	—	ns	
	TEHAX	Address Hold Time (Early Write)	TBD	—	ns	③
	TDVWH	Data Setup Time (Late Write)	30	—	ns	
	TDVEH	Data Setup Time (Early Write)	30	—	ns	⑥
	TWHDX	Data Hold Time (Late Write)	15	—	ns	
	TEHDX	Data Hold Time (Early Write)	25	—	ns	⑥
	TWLEH	Write Enable Pulse Setup Time	55	—	ns	⑥
	TWLQZ	Write Enable Output Disable Time	—	40	ns	③
	TWHQX	Write Disable Output Enable Time	0	—	ns	③

NOTES:
1. All devices tested at worst case temperature and supply voltage limits.
2. Typical derating = 5mA/MHz increase in ICCOP, VI = VCC or GND.
3. Tested at initial design and after major design changes.
4. Input pulse levels: VIL = 0.0V, VIH = 3.0V
   Input rise and fall times: 5ns (max.)
   Input and output timing reference levels: 1.5V
   Output load: 1 TTL gate equivalent and 50pF (min, including scope and jig).
5. "EL" (enable input valid) equivalent to:
   EL on the HM-8808. EIL and E2H on the HM-8808A.
6. "EH" (enable input invalid) equivalent to:
   EH on the HM-8808. EIH or E2L on the HM-8808A.
7. Relevant to the HM-8808 only.
8. Relevant to the HM-8808A only.

Absolute Maximum Ratings*

Supply Voltage (VCC-GND) .... -0.3 to 8.0V
Input or Output Voltage Applied ....GND -0.3V to VCC +0.3V
Storage Temperature .... -65°C to +150°C

Recommended Operating Conditions

Operating Supply Voltage .... 4.5V to 5.5V
Op. Temp. HM-8808/08A-8 .... -55°C to +125°C
HM-8808/08A-9 .... -40°C to +85°C

**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications (Note 1)

	SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB1	Standby Supply Current (CMOS)	—	900	µA	IO=0, $\overline{E}$=VCC-0.3V ⑦, E2=0.3V ⑧
	ICCSB	Standby Supply Current (TTL)	—	35	mA	IO=0, $\overline{E}$=VIH ⑦, E2=VIL ⑧
	ICC	Enabled Supply Current	—	60	mA	IO=0, $\overline{E}$=VIL ⑦, E2=VIH ⑧
	ICCOP	Operating Supply Current	—	70	mA	IO=0, f=1MHz, $\overline{E}$=VIL ⑦, E2=VIH ⑧ ②
	ICCDR	Data Retention Supply Current	—	400	µA	VCC=2.0V, $\overline{E}$=VCC-0.3V ⑦, E2=0.3V ⑧
	II	Input Leakage Current	-5.0	+5.0	µA	VI = GND or VCC
	IIOZ	Input/Output Leakage Current	-5.0	+5.0	µA	VIO = GND or VCC
	VCCDR	Data Retention Supply Voltage	2.0	—	V	VCC=2.0V, $\overline{E}$=VCC ⑦, E2=GND ⑧
	VOL	Output Low Voltage	—	0.4	V	IO=4.0mA
	VOH	Output High Voltage	2.4	—	V	IO=-1.0mA
	VIL	Input Low Voltage	-0.3	0.8	V	
	VIH	Input High Voltage	2.4	VCC+0.3	V	
	CI	Input Capacitance: $\overline{G}$, A	—	35	pF	VI=VCC or GND, f=1MHz ③
	CIO	Input/Output Capacitance	—	43	pF	VIO=VCC or GND, f=1MHz ③
	CE	Enable Input Capacitance	—	15	pF	VE=VCC or GND, f=1MHz ③
	CW	Write Enable Capacitance	—	48	pF	VW=VCC or GND, f=1MHz ③
READ CYCLE	TAVAX	Read Cycle Time	150	—	ns	
	TAVQV	Address Access Time	—	150	ns	
	TELQV	Chip Enable Access Time	—	150	ns	⑤
	TGLQV	Output Enable Access Time	—	65	ns	
	TELQX	Chip Enable Output Enable Time	25	—	ns	③ ⑤
	TGLQX	Output Enable Output Enable Time	5	—	ns	③
	TAXQX	Address Output Hold Time	5	—	ns	
	TEHQZ	Chip Disable Output Disable Time	0	80	ns	③ ⑥
(Note 4) A.C.	TGHQZ	Output Disable Time	0	50	ns	③
WRITE CYCLE	TAVAX	Write Cycle Time	150	—	ns	
	TELWH	Chip Enable to End of Write	90	—	ns	⑤
	TWLWH	Write Enable Pulse Width	65	—	ns	
	TELEH	Enable Pulse Width (Early Write)	TBD	—	ns	③ ⑤ ⑥
	TAVWL	Address Setup Time (Late Write)	20	—	ns	
	TAVEL	Address Setup Time (Early Write)	TBD	—	ns	③ ⑤
	TWHAX	Address Hold Time (Late Write)	20	—	ns	
	TEHAX	Address Hold Time (Early Write)	TBD	—	ns	③
	TDVWH	Data Setup Time (Late Write)	35	—	ns	
	TDVEH	Data Setup Time (Early Write)	35	—	ns	⑥
	TWHDX	Data Hold Time (Late Write)	20	—	ns	
	TEHDX	Data Hold Time (Early Write)	45	—	ns	⑥
	TWLEH	Write Enable Pulse Setup Time	65	—	ns	⑥
	TWLQZ	Write Enable Output Disable Time	—	50	ns	③
	TWHQX	Write Disable Output Enable Time	0	—	ns	③

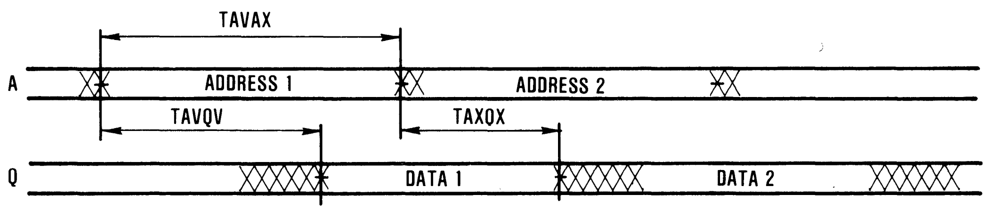
NOTES:
1. All devices tested at worst case temperature and supply voltage limits.
2. Typical derating = 5mA/MHz increase in ICCOP, VI = VCC or GND.
3. Tested at initial design and after major design changes.
4. Input pulse levels: VIL = 0.0V, VIH = 3.0V
   Input rise and fall times: 5ns (max.)
   Input and output timing reference levels: 1.5V
   Output load: 1 TTL gate equivalent and 50pF (min, including scope and jig).
5. "EL" (enable input valid) equivalent to:
   EL on the HM-8808. EIL and E2H on the HM-8808A.
6. "EH" (enable input invalid) equivalent to:
   EH on the HM-8808. EIH or E2L on the HM-8808A.
7. Relevant to the HM-8808 only.
8. Relevant to the HM-8808A only.

Truth Table

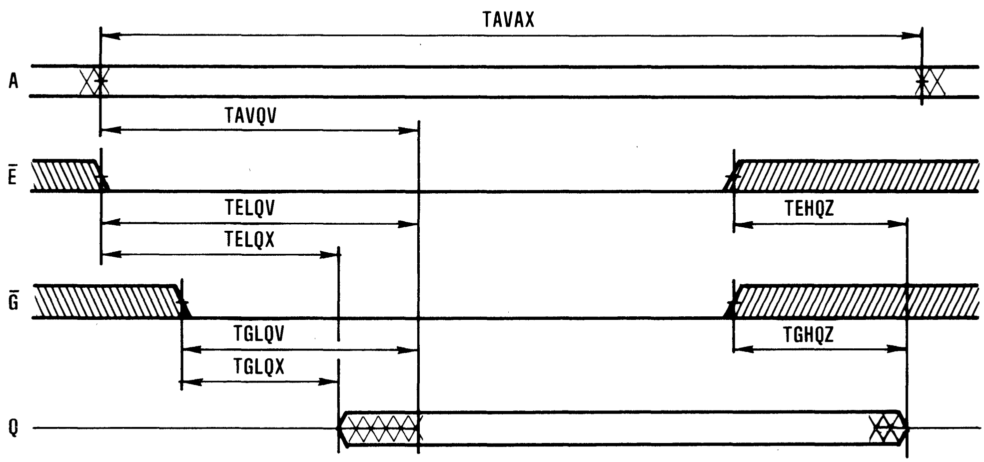
MODE	HM-8808 $\overline{E}$	HM-8808A $\overline{E1}$	HM-8808A E2	HM-8808/8808A $\overline{W}$	HM-8808/8808A $\overline{G}$
Standby (CMOS)	VCC	X	GND	X	X
Standby (TTL)	VIH	VIH	VIL	X	X
Enabled (High Z)	VIL	VIL	VIH	VIH	VIH
Write	VIL	VIL	VIH	VIL	X
Read	VIL	VIL	VIH	VIH	VIL

HM-8808 Timing Diagrams: Read Cycles

READ CYCLE I (Notes 1, 2)



READ CYCLE II (Note 1)

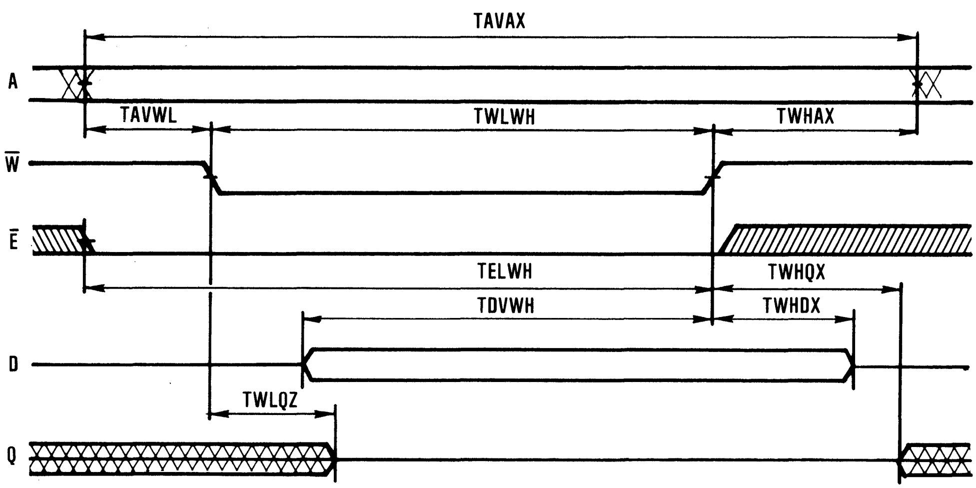


NOTES: 1. In a read cycle, $\overline{W}$ is held high.

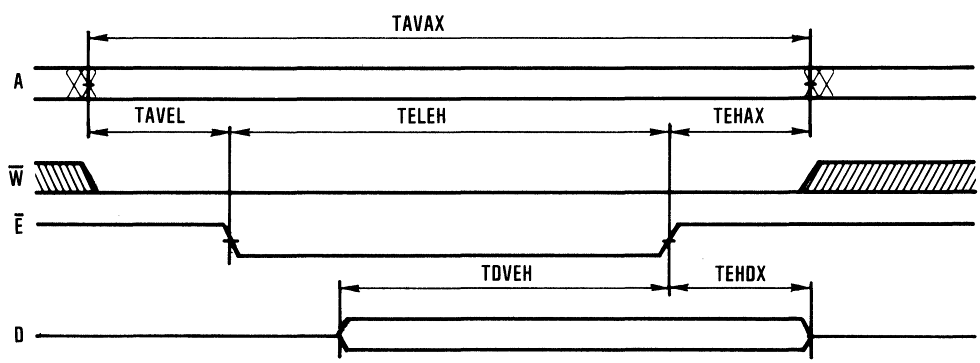
2. In read cycle I, the module is kept continuously enabled. $\overline{G}$, and $\overline{E}$ are held at VIL.

HM-8808 Timing Diagrams: Write Cycles

WRITE CYCLE I: (Notes 1, 3, 4)



WRITE CYCLE II: (Notes 2, 4)

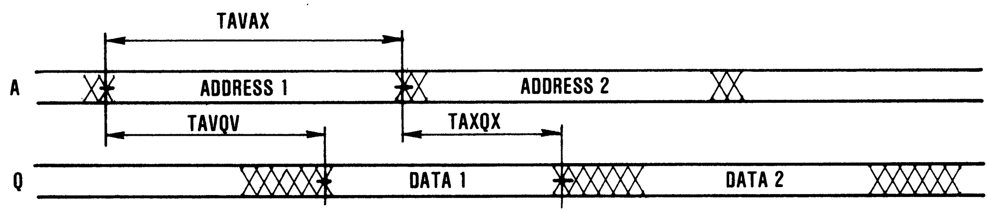


NOTES:

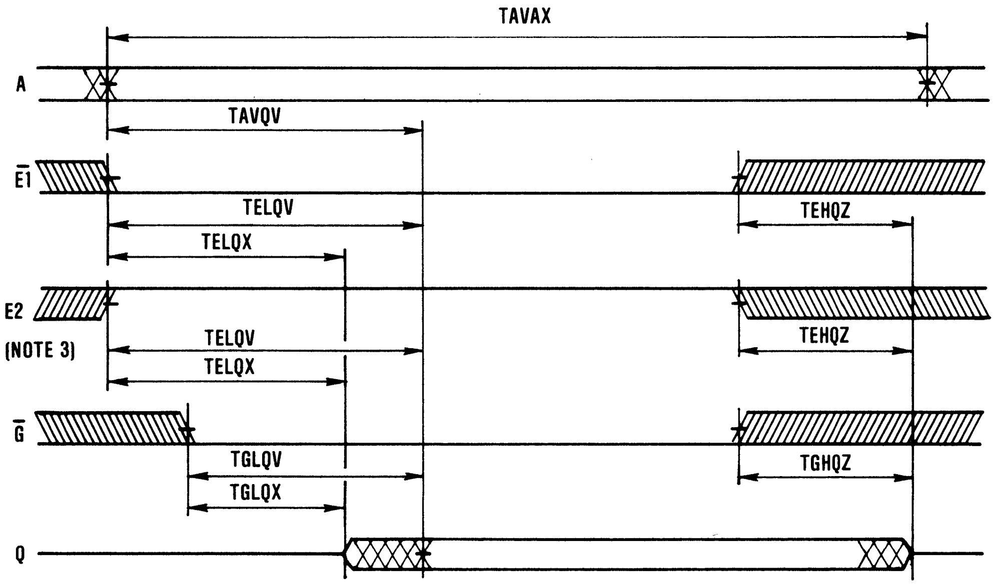
1. In Write Cycle I, the module is first enabled and then data is strobed into the RAM with a pulse on Write Enable ($\overline{W}$). Because $\overline{W}$ becomes valid after the part is enabled, this is sometimes referred to as a "Late Write" cycle.
2. In Write Cycle II, Address (A) and Write Enable ($\overline{W}$) are first set up, and then data is strobed into the RAM with a pulse on $\overline{E}$. Because $\overline{W}$ is valid before the module is enabled, this is sometimes referred to as an "Early Write" cycle.
3. Output Enable ($\overline{G}$) is normally held stable throughout the entire cycle. If $\overline{G}$ is held high, then the outputs (Q) remain in the high impedance state. If $\overline{G}$ is held low, then it may be necessary to lengthen the cycle to prevent bus contention. This would occur if TWLQZ and TDVWH overlapped.
4 Data Inputs (D) and Data Outputs (Q) are connected internally at the DQ pins.

HM-8808A Timing Diagrams: Read Cycles

READ CYCLE I (Note 1, 2)



READ CYCLE II (Note 1)

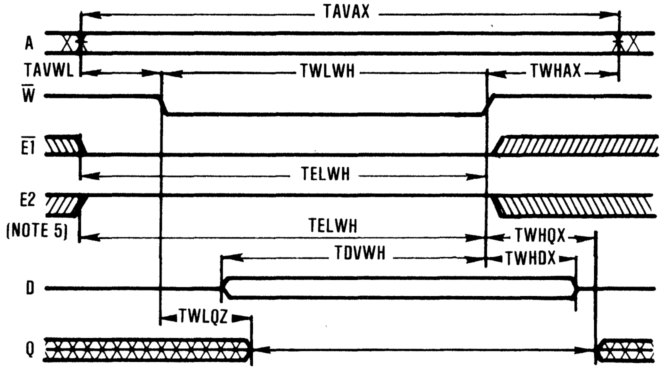


NOTES:

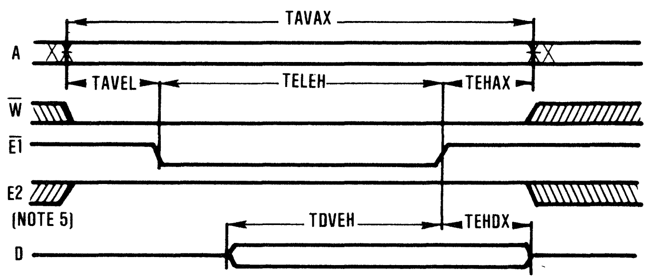
1. In a read cycle, $\overline{W}$ is held high.
2. In read cycle I, the module is kept continuously enabled: $\overline{G}$ and $\overline{E1}$ are held at VIL. E2 is held at VIH.
3. The AC timing of E2 is the same as that of $\overline{E1}$. Only the polarity is reversed. While $\overline{E1}$ is active low, E2 is active high. Therefore AC parameters that refer to the falling edge of enable, such as TELQV, can be applied to the rising edge of E2, and parameters that refer to the rising edge of enable, such as TEHQZ, can be applied to the falling edge of E2.

HM-8808A Timing Diagrams: Write Cycles

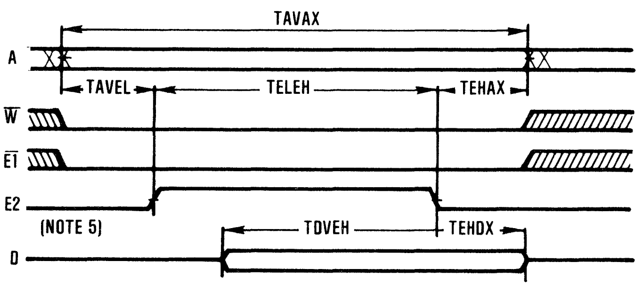
WRITE CYCLE I: Controlled by $\overline{W}$ (Notes 1, 3, 4)



WRITE CYCLE II: Controlled by $\overline{E1}$ (Notes 2, 4)



WRITE CYCLE III: Controlled by E2 (Notes 2, 4)



NOTES:

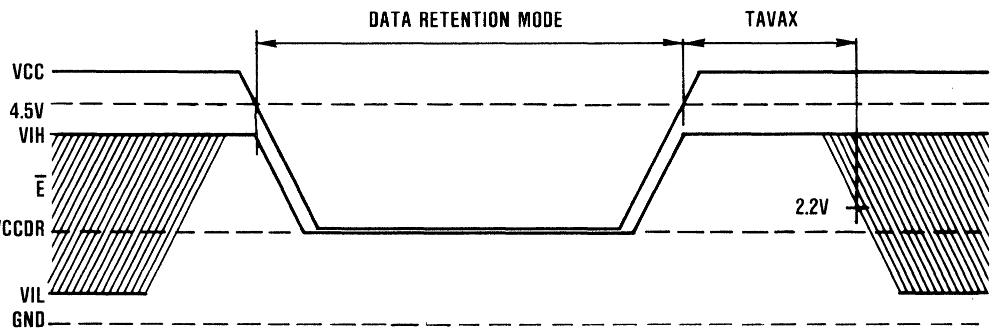
1. In Write Cycle I, the module is first enabled and then data is strobed into the RAM with a pulse on Write Enable ($\overline{W}$). Because $\overline{W}$ becomes valid after the part is enabled, this is sometimes referred to as a "Late Write" cycle.
2. In Write Cycle II and III, Address (A) and Write Enable ($\overline{W}$) are first set up, and then data is strobed into the RAM with a pulse on $\overline{E1}$ or E2. Because W is valid before the module is enabled, this is sometimes referred to as an "Early Write" cycle.
3. Output Enable ($\overline{G}$) is normally held stable throughout the entire cycle. If G is held high, then the outputs (Q) remain in the high impedance state. If $\overline{G}$ is held low, then it may be necessary to lengthen the cycle to prevent bus contention. This would occur if TWLQZ and TDVWH overlapped.
4. Data Inputs (D) and Data Outputs (Q) are connected internally at the DQ pins.
5. The AC timing of E2 is the same as that of $\overline{E1}$. Only the polarity is reversed. While $\overline{E1}$ is active low, E2 is active high. Therefore AC parameters that refer to the falling edge of enable, such as TELQV, can be applied to the rising edge of E2, and parameters that refer to the rising edge of enable, such as TEHQZ, can be applied to the falling edge of E2.

Low Voltage Data Retention

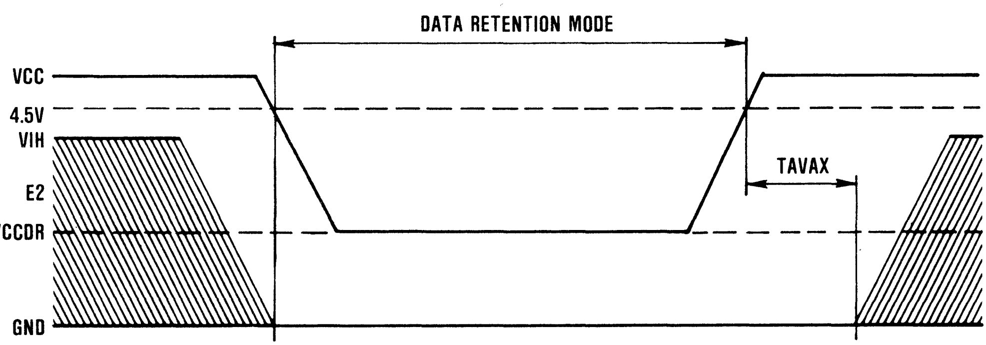
Harris CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. The module must be kept disabled during data retention. The Chip Enable ($\overline{E}$) on the HM-8808 must be held between VCC and VCC+0.3V. Chip Enable 2 (E2) on the HM-8808A must be held between -0.3V and GND.
2. During power-up and power-down transitions, $\overline{E}$ (HM-8808) must be held between 90% of VCC and VCC +0.3V; E2 (HM-8808A) must be held above -0.3V and below 10% of VCC.
3. The RAM module can begin operation one TAVAX after VCC reaches the minimum operating voltage (4.5V).

HM-8808 Data Retention Timing



HM-8808A Data Retention Timing



HARRIS

HM-8816H

PRELIMINARY

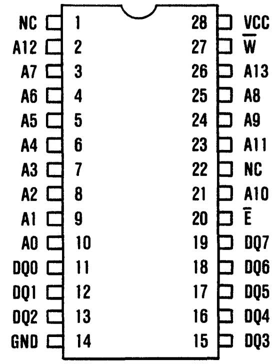
16K x 8 High Speed Asynchronous CMOS Static RAM Module

Features

- **Low Standby Supply Current 800μA**
- **Low Operating Supply Current 400mA**
- **Fast Access Time 70ns**
- **Low Data Retention Supply Voltage 2.0V**
- **Wide Operating Temperature Range .... -55°C to +125°C**
- **CMOS/TTL Compatible Inputs/Outputs**
- **JEDEC Approved Pinout**
- **Full CMOS — Six Transistor RAM Cells**
- **No Clocks or Strobes Required**
- **Single 5V Power Supply**
- **Standard DIP Size .... 0.6" x 1.5"**
- **Easy Microprocessor Interfacing**
- **Gated Inputs**

Pinout

TOP VIEW

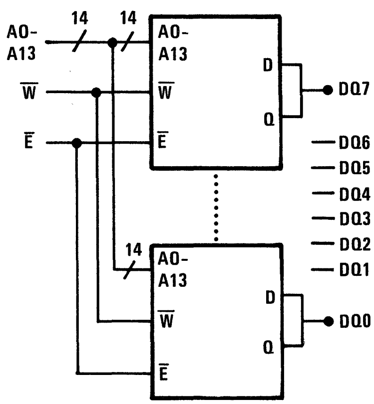


Description

The HM-8816H is a high speed, asynchronous CMOS static RAM module, based on a multi-layer, co-fired, dual-in-line ceramic substrate and eight HM-65262 16K x 1 asynchronous CMOS static RAMs packaged in leadless chip carriers. The HM-8816H uses on-substrate decoupling capacitors packaged in leadless chip carriers to reduce electrical noise and improve reliability. The pinout of the HM-8816H conforms to the JEDEC 8-bit wide, 28 pin RAM standard, which allows the system designer to design sockets that will accomodate a variety of industry standard RAMs and EPROMs. The HM-8816H also has gated inputs to simplify system design for optimum standby supply current.

The HM-65262 RAMs used in this module are full CMOS devices, utilizing arrays of six transistor (6T) memory cells for the most stable and lowest possible standby supply current over the full military temperature range. In addition to this, the high stability of the 6T cell provides excellent protection against soft errors due to electrical noise and alpha particles. This stability also improves the radiation tolerance of the RAMs over that of four transistor devices.

Functional Diagram



TRUTH TABLE

MODE	$\overline{E}$	$\overline{W}$
Standby (CMOS)	VCC	X
Standby (TTL)	VIH	X
Read	VIL	VIH
Write	VIL	VIL

PIN DESCRIPTIONS

PIN	FUNCTION
A0—A13	Address Inputs
DQ0—DQ7	Data Input/Outputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
VCC	Power (+5V)
GND	Ground

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed. Specifications are subject to change without notice.

Absolute Maximum Ratings*

SYMBOL	PARAMETER	MIN	MAX	UNITS
VCC	Supply Voltage (VCC - GND)	-0.3	+8.0	V
VIN	Applied Input or Output Voltage	-0.3	VCC +0.3	V
TA	Storage Temperature	-65	+150	°C

**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.*

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	MAX	UNITS
VCC	Supply Voltage (VCC - GND)		4.5	5.5	V
VIH	Input Voltage High		2.4	VCC +0.3	V
VIL	Input Voltage Low		-0.3	0.8	V
TA	Ambient Temperature	HM-8816H-8	-55	+125	°C
		HM-8816H-9	-40	+85	°C

D.C. Electrical Specifications (Note 1)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSBI	Standby Supply Curr. (CMOS)		800	μA	IO = 0, $\overline{E}$ = VCC - 0.3V
ICCSB	Standby Supply Current (TTL)		40	mA	IO = 0, $\overline{E}$ = VIH
ICC	Enabled Supply Current		400	mA	IO = 0, $\overline{E}$ = VIL, VIN = VIH or VIL
ICCOP	Operating Supply Current (2)		400	mA	IO=0, f=1MHz, $\overline{E}$=VIL, VIN=VCC or GND
ICCDR	Data Retention Supply Current		320	μA	VCC = 2.0V, $\overline{E}$ = VCC - 0.3V, IO = 0
II	Input Leakage Current	-1	+1	μA	VIN = VCC or GND
IIOZ	I/O Leakage Current	-1	+1	μA	VIO = VCC or GND
VCCDR	Data Retention Supply Voltage	2.0		V	$\overline{E}$ = VCC
VOL	Output Voltage Low		0.4	V	IOL = 8.0mA
VOH	Output Voltage High	2.4		V	IOH = -4.0mA

Capacitance (Note 3)

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance	70	pF	f = 1MHz, VIN = VCC or GND
CIO	Input/Output Capacitance	25	pF	f = 1MHz, VIO = VCC or GND

NOTES:
1. All devices tested at worst case temperature and supply voltage limits.
2. Typical derating: 40mA/MHz increase in ICCOP.
3. Tested at initial design and after major design changes.
4. Input pulse levels: VIL = 0.0V, VIH = 3.0V; Input rise and fall times: 5ns max; Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent and CL = 50pF min., including scope and jig - for CL greater than 50pF, access time is derated by 0.15ns/pF; Output load for output enable/disable times: 1 TTL gate equivalent and CL = 5pF min., including scope and jig.

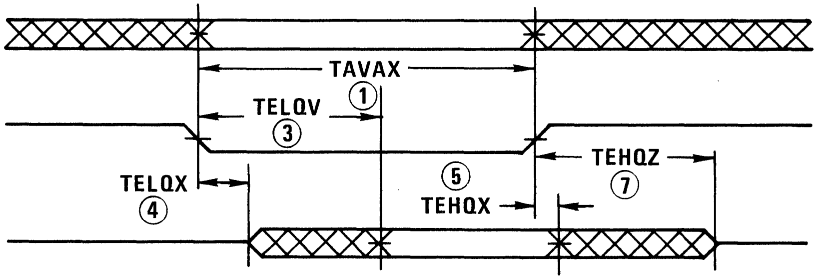
A.C. Electrical Specifications (Notes 1, 4)

					HM-8816HB		HM-8816H			
NO.	SYMBOL		PARAMETER		MIN	MAX	MIN	MAX	UNITS	NOTES
READ CYCLE										
1	TAVAX	tRC	Read Cycle Time		70		85		ns	
2	TAVQV	tAA	Address Access Time			70		85	ns	
3	TELQV	tCE	Chip Enable Access Time			70		85	ns	
4	TELQX	tLZ	Chip Enable Output Enable Time		5		5		ns	3
5	TEHQX		Chip Enable Output Hold Time		5		5		ns	3
6	TAXQX	tOH	Address Output Hold Time		5		5		ns	3
7	TEHQZ	tHZ	Chip Disable Output Disable Time		0	40	0	40	ns	3
WRITE CYCLE										
8	TAVAX	tWC	Write Cycle Time		70		85		ns	
9	TELWH	tCW	Chip Enable to End of Write	$\overline{W}$ Controlled	65		75		ns	
10	TELEH	tCW		$\overline{E}$ Controlled	65		75		ns	3
11	TWLWH	tWP	Write Pulse Width		55		60		ns	
12	TAVWL	tAS	Address Setup Time	$\overline{W}$ Controlled	0		0		ns	
13	TAVEL	tAS		$\overline{E}$ Controlled	0		0		ns	3
14	TWHAX	tWR	Write Recovery Time	$\overline{W}$ Controlled	10		10		ns	
15	TEHAX	tWR		$\overline{E}$ Controlled	10		10		ns	3
16	TDVWH	tDW	Data Setup Time	$\overline{W}$ Controlled	30		35		ns	
17	TDVEH	tDW		$\overline{E}$ Controlled	30		35		ns	3
18	TWHDX	tDH	Data Hold Time	$\overline{W}$ Controlled	5		5		ns	
19	TEHDX	tDH		$\overline{E}$ Controlled	10		10		ns	
20	TWLQZ	tWZ	Write Enable Low to Output Off			40		40	ns	3
21	TWHQX	tOW	Write Enable High to Output On		0		0		ns	3

NOTES: 1. All devices tested at worst case temperature and supply voltage limits.
2. Typical derating: 40mA/MHz increase in ICCOP.
3. Tested at initial design and after major design changes.
4. Input pulse levels: VIL = 0.0V, VIH = 3.0V; Input rise and fall times: 5ns max; Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent and CL = 50pF min., including scope and jig - for CL greater than 50pF, access time is derated by 0.15ns/pF; Output load for output enable/disable times: 1 TTL gate equivalent and CL = 5pF min., including scope and jig.

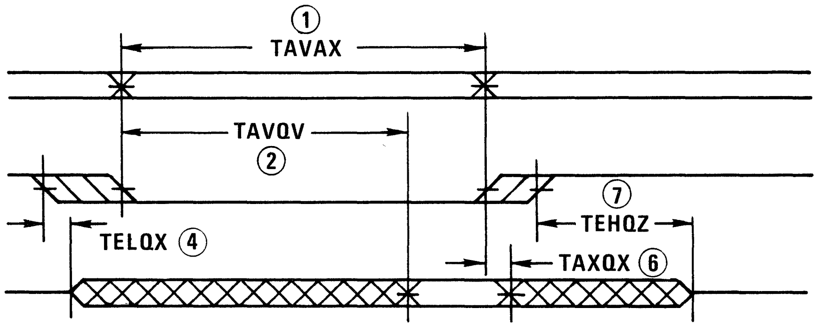
Timing Diagrams, Read Cycles

READ CYCLE 1: CONTROLLED BY $\overline{E}$



NOTE: $\overline{W}$ is held high for entire cycle and D is ignored. Address is stable by the time $\overline{E}$ goes low and remains valid until $\overline{E}$ goes high.

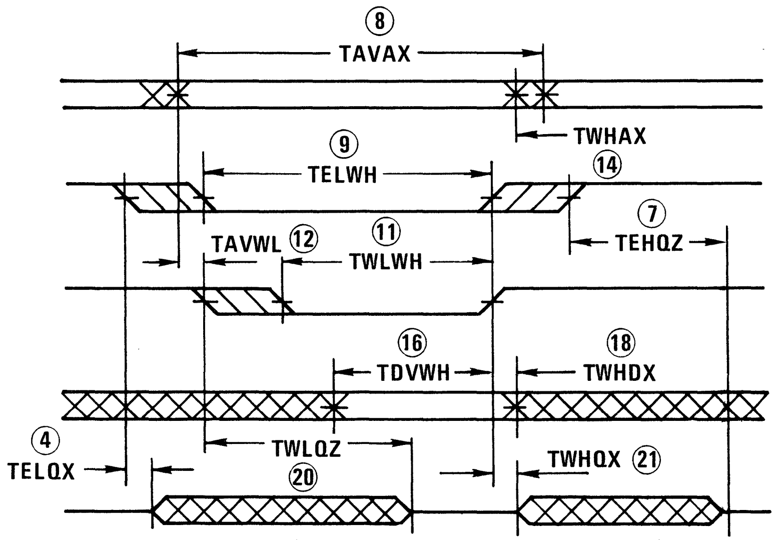
READ CYCLE 2: CONTROLLED BY ADDRESS



NOTE: $\overline{W}$ is high for the entire cycle and D is ignored. $\overline{E}$ is stable prior to A becoming valid and after A becomes invalid.

Timing Diagrams, Write Cycles

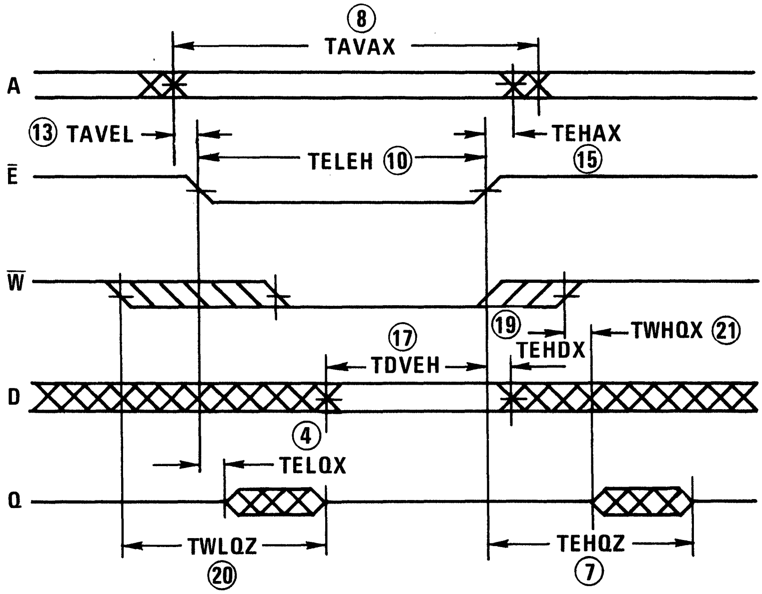
WRITE CYCLE 1 TIMING: CONTROLLED BY $\overline{W}$ (LATE WRITE)



NOTE: In this mode, $\overline{E}$ rises after $\overline{W}$. The address must remain stable whenever both $\overline{E}$ and $\overline{W}$ are low.

Timing Diagrams, Write Cycles

WRITE CYCLE 2 TIMING: CONTROLLED BY Ē (EARLY WRITE)



NOTE: In this mode, W̄ rises after Ē. If W̄ falls before Ē by a time exceeding TWLQZ (Max) - TELQX (Min), and rises after Ē by a time exceeding TEHQZ (Max) - TWHQZ (Min), then Q̄ will remain in the high impedance state throughout the cycle.

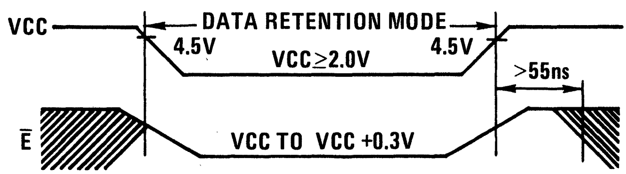
The address must remain stable whenever Ē and W̄ are both low.

Low Voltage Data Retention

Harris CMOS RAM are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. Chip Enable (Ē) must be held high during data retention; within VCC to VCC + 0.3V.
2. Ē must be kept between VCC +0.3 and 70% of VCC during the power up and power down transitions.
3. The RAM can begin operation 55ns after VCC reaches the minimum operation Voltage (4.5V).

DATA RETENTION TIMING



HM-92560

256K Synchronous CMOS RAM Module

Features

- **Low Standby Current 500μA**
- **Fast Address Access Time 170ns**
- **Data Retention .... 2.0V Min VCC**
- **Three State Outputs**
- **Organizable as 32K x 8 or 16K x 16 Array**
- **On Chip Address Registers**
- **48 Pin DIP Pinout — 2.66" x 1.30" x 0.29"**
- **Synchronous Operation Yields Low Operating Power 30mA/MHz**
- **Wide Temperature Range .... -55°C to +125°C**

Description

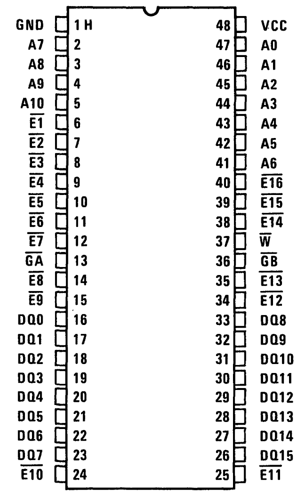
The HM-92560 is a high density 256K bit CMOS RAM module. Sixteen synchronous HM-6516 2K x 8 CMOS RAMs in leadless chip carriers are mounted on a multilayer ceramic substrate. The HM-92560 RAM module is organized as two 16K x 8 CMOS RAM arrays sharing a common address bus. Separate data input/output buses and chip enables allow the user to format the HM-92560 as either a 16K x 16 or 32K x 8 array. Ceramic capacitors are included on the substrate to reduce noise and to minimize the need for additional external decoupling.

The synchronous design of the HM-92560 provides low operating power along with address latches for ease of interface to multiplexed address/data bus microprocessors.

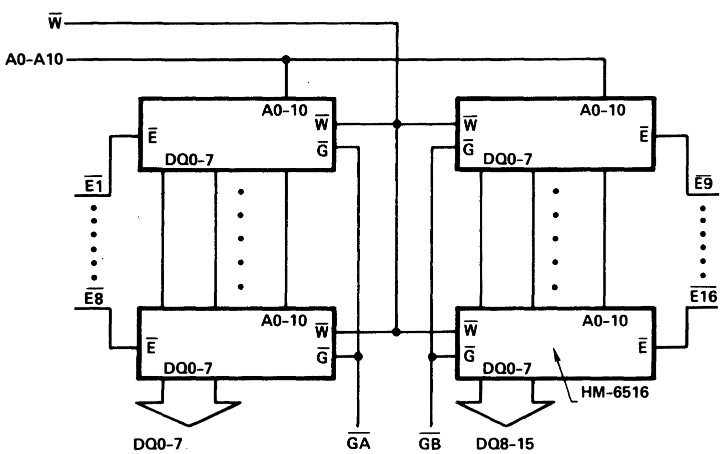
The HM-92560 is physically constructed as an extra wide 48 pin dual-in-line package with standard 0.1" centers between pins. This package technique combines the high packing density of CMOS and leadless chip carriers with the ease of use of DIP packaging.

Pinout

TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Organizational Guide

FOR 32K x 8 CONFIGURATION

CONNECT:
PIN 16 (DQ0) to PIN 33 (DQ8)
PIN 17 (DQ1) to PIN 32 (DQ9)
PIN 18 (DQ2) to PIN 31 (DQ10)
PIN 19 (DQ3) to PIN 30 (DQ11)
PIN 20 (DQ4) to PIN 29 (DQ12)
PIN 21 (DQ5) to PIN 28 (DQ13)
PIN 22 (DQ6) to PIN 27 (DQ14)
PIN 23 (DQ7) to PIN 26 (DQ15)

FOR 16K x 16 CONFIGURATION

CONNECT:
PIN 6 ($\overline{E1}$) to PIN 15 ($\overline{E9}$)
PIN 7 ($\overline{E2}$) to PIN 24 ($\overline{E10}$)
PIN 8 ($\overline{E3}$) to PIN 25 ($\overline{E11}$)
PIN 9 ($\overline{E4}$) to PIN 34 ($\overline{E12}$)
PIN 10 ($\overline{E5}$) to PIN 35 ($\overline{E13}$)
PIN 11 ($\overline{E6}$) to PIN 38 ($\overline{E14}$)
PIN 12 ($\overline{E7}$) to PIN 39 ($\overline{E15}$)
PIN 14 ($\overline{E8}$) to PIN 40 ($\overline{E16}$)
PIN 13 ($\overline{GA}$) to PIN 36 ($\overline{GB}$)

Concerns for Proper Operation of Chip Enables:

The transition between blocks of RAM requires a change in the chip enable being used. When operating in the 16K x 16 mode use the chip enables as if there were only eight, E1 thru E8. In the 32K x 8 mode, all chip enables must be treated separately. Transitions between chip enables must be treated with the same timing constraints that apply to any one chip enable. All chip enables must be high at least one chip enable high time (TEHEL) before any chip enable can fall. As the HM-92560 is a synchrounous memory every address transition must be accompanied by a chip enable transition (see timing diagrams). More than one chip enable low simultaneously, for devices whose outputs are tied common either internally or externally, is an illegal input condition and must be avoided.

Printed Circuit Board Mounting:

The leadless chip carrier packages used in the HM-92560 have conductive lids. These lids are electrically connected to GND. The designer should be aware of the possibility that the carriers on the bottom side could short conductors below if pressed completely down against the surface of the circuit board. The pins on the package are designed with a standoff feature to help prevent the leadless carriers from touching the circuit board surface.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) ....-0.3V to +8.0V
Input or Output Voltage Applied.................. (GND -0.3V) to (VCC +0.3V)
Storage Temperature..............................-65°C to +150°C

Operating Range

Operating Supply Voltage
HM5-92560-2/-8..4.5V to 5.5V
HM5-92560-9 ....4.5V to 5.5V
Operating Temperature
HM5-92560-2/-8...............................-55°C to +125°C
HM5-92560-9 ....-40°C to +85°C

*CAUTION: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications

	SYMBOL	PARAMETER	TEMP. & VCC * OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		500	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ② 16K x 16		30	mA	Ē = 1MHz, IO = 0 VI = VCC or GND, G̅ = VCC
	ICCOP	Operating Supply Current ② 32K x 8		15	mA	Ē = 1MHz, IO = 0 VI = VCC or GND, G̅ = VCC
	ICCDR	Data Retention Supply Current		350	μA	IO = 0, VCC = 2.0, VI = VCC or GND, Ē = VCC
	VCCDR	Data Retention Supply Voltage	2.0		V	
	II	Input Leakage Current	-5	+5	μA	VI = VCC or GND
	IIOZ	Input/Output Leakage Current	-5	+5	μA	VIO = VCC or GND
	VIL	Input Low Voltage	-0.3	.8	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	V	
	VOL	Output Low Voltage		0.4	V	IO = 3.2mA
	VOH	Output High Voltage	2.4		V	IO = -1.0mA
	CIA	Address Input ③ Capacitance		200	pF	VI = VCC or GND f = 1MHz
	CIE1	Enable Input ③ Capacitance (16K x 16)		100	pF	VI = VCC or GND f = 1MHz
	CIE2	Enable Input ③ Capacitance (32K x 8)		50	pF	VI = VCC or GND f = 1MHz
	CIG 1	Output Enable Input ③ Capacitance (16K x 16)		150	pF	VI = VCC or GND f = 1MHz
	CIG 2	Output Enable Input ③ Capacitance (32K x 8)		100	pF	VI = VCC or GND f = 1MHz
	CIO1	Input/Output ③ Capacitance (16K x 16)		150	pF	VI/O = VCC or GND f = 1MHz
	CIO2	Input/Output ③ Capacitance (32 x 8)		250	pF	VI/O = VCC or GND f = 1MHz
	CIW	Write Input ③ Capacitance		200	pF	VI = VCC or GND f = 1MHz
	CVcc	Decoupling Capacitance	0.5		μf	f = 1MHz

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) ....-0.3V to +8.0V
Input or Output Voltage Applied .... (GND -0.3V) to (VCC +0.3V)
Storage Temperature ....$-65^{o}C$ to $+150^{o}C$

Operating Range

Operating Supply Voltage
HM5-92560-2/-8 .... 4.5V to 5.5V
HM5-92560-9 .... 4.5V to 5.5V
Operating Temperature
HM5-92560-2/-8 ....$-55^{o}C$ to $+125^{o}C$
HM5-92560-9 ....$-40^{o}C$ to $+85^{o}C$

**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications

	SYMBOL	PARAMETER	TEMP. & VCC * OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
A.C.	TELQV	Chip Enable Access Time		150	ns	④
	TAVQV	Address Access Time		170	ns	④
	TELQX	Chip Enable Output Enable Time	10		ns	③④
	TEHQZ	Chip Enable Output Disable Time		70	ns	③④
	TGLQX	Output Enable Output Enable Time	10		ns	③④
	TGLQV	Output Enable Output Valid Time		70	ns	④
	TGHQZ	Output Enable Output Disable Time		70	ns	③④
	TELEH	Chip Enable Pulse Negative Width	150		ns	④
	TEHEL	Chip Enable Pulse Positive Width	80		ns	④
	TAVEL	Address Setup Time	20		ns	④
	TELAX	Address Hold Time	50		ns	④
	TWLWH	Write Enable Pulse Width	150		ns	④
	TWLEH	Write Enable Pulse Setup Time	150		ns	④
	TELWH	Write Enable Pulse Hold Time	150		ns	④
	TDVWH	Data Setup Time	80		ns	④
	TWHDX	Data Hold Time	20		ns	④
	TWLDV	Write Data Delay Time	70		ns	④
	TELEL	Read or Write Cycle Time	230		ns	④

NOTES:
① All devices tested at worst case temperature and V_{CC}.
② Operating supply current (ICCOP) is proportional to operating frequency.
③ Tested at initial design and after major design changes.
④ Input pulse levels: 0V to 3V. Input rise and fall times: 10ns max. Input and output timing reference levels: 1.5V. Output load: C_L = 50 to 300pF. For C_L greater than 50pF, access time is derated 0.15ns/pF.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) ....-0.3V to +8.0V
Input or Output Voltage Applied.................. (GND -0.3V) to (VCC +0.3V)
Storage Temperature..............................-65°C to +150°C

Operating Range

Operating Supply Voltage
HM5-92560-5 .... 4.5V to 5.5V
Operating Temperature
HM5-92560-5 .... 0°C to +70°C

**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications

D.C.

SYMBOL	PARAMETER	TEMP. & VCC * OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current		3.5	mA	IO = 0 VI = VCC or GND
ICCOP	Operating Supply Current ② 16K x 16		35	mA	$\overline{E}$ = 1MHz, IO = 0 VI = VCC or GND, $\overline{G}$ = VCC
ICCOP	Operating Supply Current ② 32K x 8		20	mA	$\overline{E}$ = 1MHz, IO = 0 VI = VCC or GND, $\overline{G}$ = VCC
ICCDR	Data Retention Supply Current		2.5	mA	IO = 0, VCC = 2.0, VI = VCC or GND, $\overline{E}$ = VCC
VCCDR	Data Retention Supply Voltage	2.0		V	
II	Input Leakage Current	-10	+10	μA	VI = VCC or GND
IIOZ	Input/Output Leakage Current	-10	+10	μA	VIO = VCC or GND
VIL	Input Low Voltage	-0.3	.8	V	
VIH	Input High Voltage	VCC -2.0	VCC +0.3	V	
VOL	Output Low Voltage		0.4	V	IO = 3.2mA
VOH	Output High Voltage	2.4		V	IO = -1.0mA
CIA	Address Input ③ Capacitance		200	pF	VI = VCC or GND f = 1MHz
CIE1	Enable Input ③ Capacitance (16K x 16)		100	pF	VI = VCC or GND f = 1MHz
CIE2	Enable Input ③ Capacitance (32K x 8)		50	pF	VI = VCC or GND f = 1MHz
CIG 1	Output Enable Input ③ Capacitance (16K x 16)		150	pF	VI =VCC or GND f = 1MHz
CIG 2	Output Enable Input ③ Capacitance (32K x 8)		100	pF	VI = VCC or GND f = 1MHz
CIO1	Input/Output ③ Capacitance (16K x 16)		150	pF	VI/O = VCC or GND f = 1MHz
CIO2	Input/Output ③ Capacitance (32 x 8)		250	pF	VI/O = VCC or GND f = 1MHz
CIW	Write Input ③ Capacitance		200	pF	VI = VCC or GND f = 1MHz
CVcc	Decoupling Capacitance	0.5		μf	f = 1MHz

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) ....-0.3V to +8.0V
Input or Output Voltage Applied.................. (GND -0.3V) to (VCC +0.3V)
Storage Temperature..............................-65°C to +150°C

Operating Range

Operating Supply Voltage
HM5-92560-5 .... 4.5V to 5.5V
Operating Temperature
HM5-92560-5 .... 0°C to +70°C

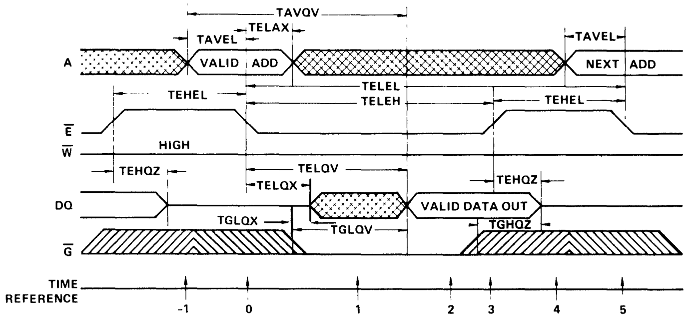
**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications

	SYMBOL	PARAMETER	TEMP. & VCC * OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
A.C.	TELQV	Chip Enable Access Time		250	ns	④
	TAVQV	Address Access Time		270	ns	④
	TELQX	Chip Enable Output Enable Time	10		ns	③ ④
	TEHQZ	Chip Enable Output Disable Time		80	ns	③ ④
	TGLQX	Output Enable Output Enable Time	10		ns	③ ④
	TGLQV	Output Enable Output Valid Time		70	ns	④
	TGHQZ	Output Enable Output Disable Time		80	ns	③ ④
	TELEH	Chip Enable Pulse Negative Width	250		ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		ns	④
	TAVEL	Address Setup Time	20		ns	④
	TELAX	Address Hold Time	50		ns	④
	TWLWH	Write Enable Pulse Width	250		ns	④
	TWLEH	Write Enable Pulse Setup Time	250		ns	④
	TELWH	Write Enable Pulse Hold Time	250		ns	④
	TDVWH	Data Setup Time	100		ns	④
	TWHDX	Data Hold Time	20		ns	④
	TWLDV	Write Data Delay Time	150		ns	④
	TELEL	Read or Write Cycle Time	350		ns	④

NOTES: ① All devices tested at worst case temperature and V_{CC}.
② Operating supply current (ICCOP) is proportional to operating frequency.
③ Tested at initial design and after major design changes.
④ Input pulse levels: 0V to 3V. Input rise and fall times: 10ns max. Input and output timing reference levels: 1.5V. Output load: C_L = 50 to 300pF. For C_L greater than 50pF, access time is derated 0.15ns/pF.

Read Cycle

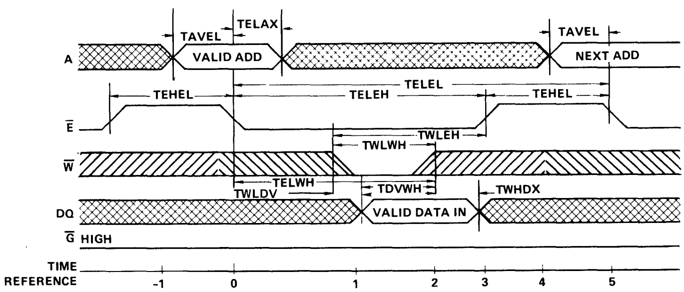


TRUTH TABLE

TIME REFERENCE	$\overline{E}$	$\overline{W}$	$\overline{G}$	A	DQ	FUNCTION
-1	H	X	X	X	Z	MEMORY DISABLED
0	↘	H	X	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	L	X	X	OUTPUT ENABLED
2	L	H	L	X	V	OUTPUT VALID
3	↗	H	X	X	V	READ ACCOMPLISHED
4	H	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↘	H	X	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$ (T = 0), minimum address setup and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1), the outputs become enabled but data is not valid until time (T = 2), $\overline{W}$ must remain high throughout the read cycle. After the data has been read, $\overline{E}$ may return high (T = 3). This will force the output buffers into a high impedance mode at time (T = 4). $\overline{G}$ is used to disable the output buffers when in a logical "1" state (T = -1, 0, 3, 4, 5). After (T = 4) time, the memory is ready for the next cycle.

Write Cycle



TRUTH TABLE

TIME REFERENCE	$\overline{E}$	$\overline{W}$	$\overline{G}$	A	DQ	FUNCTION
-1	H	X	H	X	X	MEMORY DISABLED
0	↘	X	H	V	X	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	H	X	X	WRITE PERIOD BEGINS
2	L	↗	H	X	V	DATA IN IS WRITTEN
3	↗	H	H	X	X	WRITE COMPLETED
4	H	X	H	X	X	PREPARE FOR NEXT CYCLE (SAME AS-1)
5	↘	X	H	V	X	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The write cycle is initiated on the falling edge of $\overline{E}$ (T = 0), which latches the address information in the on chip registers. If a write cycle is to be performed where the output is not to become active, $\overline{G}$ can be held high (inactive). TDVWH and TWHDX must be met for proper device operation regardless of $\overline{G}$. If $\overline{E}$ and $\overline{G}$ fall before $\overline{W}$ falls (read mode), a possible bus conflict may exist. If $\overline{E}$ rises before $\overline{W}$ rises, reference data setup and hold times to the $\overline{E}$ rising edge. The write operation is terminated by the first rising edge of $\overline{W}$ (T = 2) or $\overline{E}$(T = 3). After the minimum $\overline{E}$ high time (TEHEL), the next cycle may begin. If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may be held low unitl all desired locations have been written. In this case, data setup and hold times must be referenced to the rising edge of $\overline{E}$.

HARRIS

HM-92570

256K Buffered Synchronous CMOS RAM Module

Features

- LOW STANDBY CURRENT 600µA/3.5mA
- FAST ACCESS TIME 250ns
- DATA RETENTION . . . . 2.0V min
- THREE STATE OUTPUTS
- ORGANIZABLE AS 32K x 8 or 16K x 16 ARRAY
- BUFFERED ADDRESS AND CONTROL LINES
- ON CHIP ADDRESS REGISTERS
- 48 PIN DIP PINOUT – 2.66" x 1.30" x 0.29"
- WIDE TEMPERATURE RANGE . . . . -55°C to +125°C

Description

The HM-92570 is a fully buffered 256K bit CMOS RAM Module consisting of sixteen HM-6516 2Kx8 CMOS RAMs, two 82C82 CMOS octal latching bus drivers, and two HCT-138 CMOS 3:8 decoders in leadless chip carriers mounted on a multilayer ceramic substrate. The HM-92570 RAM Module is organized as two 16Kx8 CMOS RAM arrays sharing a common address bus. Separate data input/output buses allow the user to format the HM-92570 as either a 16Kx16 or 32Kx8 array.

On-board buffers and decoders reduce external package count requirements. Write enable, output enable and chip enable control signals are buffered along with address inputs. Ceramic capacitors sealed in leadless carriers are included on the substrate to reduce power supply noise and to reduce the need for external decoupling.

The synchronous design of the HM-92570 provides low operating power along with address latches for ease of interface to multiplexed address/data bus microprocessors.

The HM-92570 is physically constructed as an extra wide 48 pin dual-in-line package with standard 0.1" centers between pins. This package technique combines the high packing density of CMOS and leadless chip carriers with the ease of use of DIP packaging.

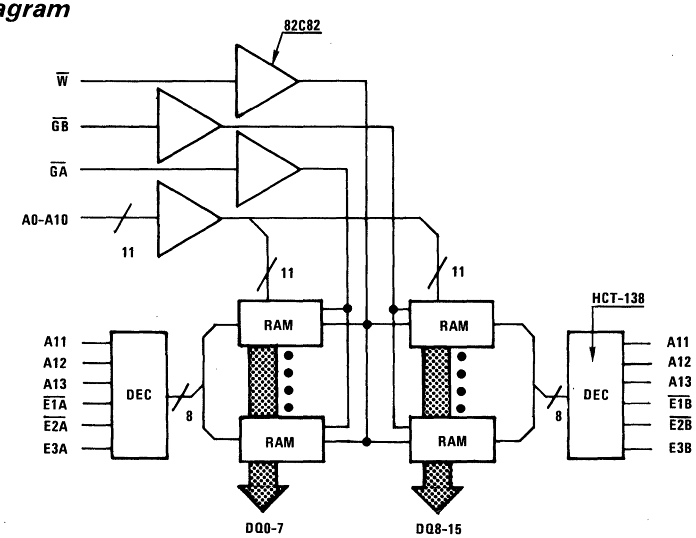
Pinout

GND	1	48	VCC
A7	2	47	A0
A8	3	46	A1
A9	4	45	A2
A10	5	44	A3
A11	6	43	A4
A12	7	42	A5
A13	8	41	A6
$\overline{E1A}$	9	40	$\overline{E1B}$
$\overline{E2A}$	10	39	$\overline{E2B}$
E3A	11	38	E3B
NC	12	37	$\overline{W}$
$\overline{GA}$	13	36	$\overline{GB}$
NC	14	35	NC
NC	15	34	NC
DQ0	16	33	DQ8
DQ1	17	32	DQ9
DQ2	18	31	DQ10
DQ3	19	30	DQ11
DQ4	20	29	DQ12
DQ5	21	28	DQ13
DQ6	22	27	DQ14
DQ7	23	26	DQ15
VCC	24	25	GND

PIN NAMES

A	–	Address Input
DQ	–	Data Input/Output
$\overline{GX}$	–	Output Enable
$\overline{EXX}$	–	Chip Enable
$\overline{W}$	–	Write Enable
NC	–	No Connection

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Organizational Guide

FOR 32K x 8 CONFIGURATION

CONNECT:
PIN 16 (DQ0) to PIN 33 (DQ8)
PIN 17 (DQ1) to PIN 32 (DQ9)
PIN 18 (DQ2) to PIN 31 (DQ10)
PIN 19 (DQ3) to PIN 30 (DQ11)
PIN 20 (DQ4) to PIN 29 (DQ12)
PIN 21 (DQ5) to PIN 28 (DQ13)
PIN 22 (DQ6) to PIN 27 (DQ14)
PIN 23 (DQ7) to PIN 26 (DQ15)

FOR 16K x 16 CONFIGURATION

CONNECT:
PIN 9 ($\overline{E1A}$) to PIN 40 ($\overline{E1B}$)
PIN 10 ($\overline{E2A}$) to PIN 39 ($\overline{E2B}$)
PIN 11 (E3A) to PIN 38 (E3B)
PIN 13 (GA) to PIN 36 (GB)

Concerns for Proper Operation of Chip Enables:

The transition between blocks of RAM requires a change in the chip enable being used. When operating in the 16K x 16 mode use the chip enables as if there were only three, E1 thru E3. In the 32K x 8 mode all chip enables must be treated separately. Transitions between chip enables must be treated with the same timing constraints that apply to any one chip enable. All chip enables must be high at least one chip enable high time (TEHEL) before any chip enable can fall.

As the HM-92570 is a synchrounous memory, every address transition must be accompanied by a chip enable transition (see timing diagrams). More than one chip enable low simultaneously, for devices whose outputs are tied common either internally or externally, is an illegal input condition and must be avoided. To properly decode the chip enables, addresses A11, A12, and A13 must be valid for the duration of TAVAV.

Printed Circuit Board Mounting:

The leadless chip carrier packages used in the HM-92570 have conductive lids. These lids are electrically connected to GND. The designer should be aware of the possibility that the carriers on the bottom side could short conductors below if pressed completely down against the surface of the circuit board. The pins on the package are designed with a standoff feature to help prevent the leadless carriers from touching the circuit board surface.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) ....-0.3V to +8.0V
Input or Output Voltage Applied.................. (GND -0.3V) to (VCC +0.3V)
Storage Temperature..............................-65°C to +150°C

Operating Range

Operating Supply Voltage
HM5-92570-2/-8.. 4.5V to 5.5V
HM5-92570-9 .... 4.5V to 5.5V
Operating Temperature
HM5-92570-2/-8.................................-55°C to +125°C
HM5-92570-9 ....-40°C to +85°C

**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications

D.C.

SYMBOL	PARAMETER	TEMP. & VCC OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current		600	μA	IO = 0 VI = VCC or GND
ICCOP	Operating Supply Current ② 16K x 16		30	mA	Ē = 1MHz, IO = 0 VI = VCC or GND, Ḡ = VCC
ICCOP	Operating Supply Current ② 32K x 8		15	mA	Ē = 1MHz, IO = 0 VI = VCC or GND, Ḡ = VCC
ICCDR	Data Retention Supply Current		450	μA	IO = 0, VCC = 2.0, VI = VCC or GND, Ē = VCC
VCCDR	Data Retention Supply Voltage	2.0		V	
II	Input Leakage Current	-1.0	+1.0	μA	VI = VCC or GND
IIOZ	Input/Output Leakage Current	-5.0	+5.0	μA	VIO = VCC or GND
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	3.5	VCC +0.3	V	
VOL	Output Low Voltage		0.4	V	IO = 3.2mA
VOH	Output High Voltage	2.4		V	IO = -1.0mA
CIA	Address Input ③ Capacitance		50	pF	VI = VCC or GND f = 1MHz
CIE1	Decoder Enable Input ③ Capacitance (16K x 16)		50	pF	VI = VCC or GND f = 1MHz
CIE2	Decoder Enable Input ③ Capacitance (32K x 8)		25	pF	VI = VCC or GND f = 1MHz
CIG 1	Output Enable Input ③ Capacitance (16K x 16)		50	pF	VI = VCC or GND f = 1MHz
CIG 2	Output Enable Input ③ Capacitance (32K x 8)		25	pF	VI = VCC or GND f = 1MHz
CIO1	Input/Output ③ Capacitance (16K x 16)		150	pF	VI/O = VCC or GND f = 1MHz
CIO2	Input/Output ③ Capacitance (32K x 8)		250	pF	VI/O = VCC or GND f = 1MHz
CIW	Write Input ③ Capacitance		25	pF	VI = VCC or GND f = 1MHz
CVcc	Decoupling Capacitance	0.5		μF	f = 1MHz

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) ....-0.3V to +8.0V
Input or Output Voltage Applied .... (GND -0.3V) to (VCC +0.3V)
Storage Temperature ....-65°C to +150°C

Operating Range

Operating Supply Voltage
HM5-92570-2/-8 .... 4.5V to 5.5V
HM5-92570-9 .... 4.5V to 5.5V
Operating Temperature
HM5-92570-2/-8 .... -55°C to +125°C
HM5-92570-9 .... -40°C to +85°C

**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications

	SYMBOL	PARAMETER	TEMP. & VCC OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
A.C.	TELQV	Chip Enable Access Time		250	ns	④
	TAVQV	Address Access Time		270	ns	④
	TELQX	Chip Enable Output Enable Time	10		ns	③④
	TEHQZ	Chip Enable Output Disable Time		150	ns	③④
	TGLQX	Output Enable Output Enable Time	10		ns	③④
	TGLQV	Output Enable Output Valid Time		120	ns	④
	TGHQZ	Output Enable Output Disable Time		150	ns	③④
	TELEH	Chip Enable Pulse Negative Width	250		ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		ns	④
	TAVEL	Address Setup Time	20		ns	④ ⑤
	TELAX	Address Hold Time	120		ns	④
	TWLWH	Write Enable Pulse Width	140		ns	④
	TWLEH	Write Enable Pulse Setup Time	140		ns	④
	TELWH	Write Enable Pulse Hold Time	250		ns	④
	TDVWH	Data Setup Time	20		ns	④
	TWHDX	Data Hold Time	70		ns	④
	TWLDV	Write Data Delay Time	120		ns	④
	TELEL	Read or Write Cycle Time	350		ns	④
	TAVAV	Enable Decoder Address Valid Time	270		ns	Applies Only to A11, A12, A13

NOTES:
① All devices tested at worst case temperature and V_{CC}.
② Operating supply current (ICCOP) is proportional to operating frequency.
③ Tested at initial design and after major design changes.
④ Input pulse levels: 0V to 3.5V. Input rise and fall times: 10ns max. Input and output timing reference levels: 1.5V. Output load: C_L = 50 to 300pF. For C_L greater than 50pF, access time is derated 0.15ns/pF.
⑤ Includes A11, A12, A13.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) ....-0.3V to +8.0V
Input or Output Voltage Applied .... (GND -0.3V) to (VCC +0.3V)
Storage Temperature ....-65°C to +150°C

Operating Range

Operating Supply Voltage
HM5-92570-5 .... 4.5V to 5.5V
Operating Temperature
HM5-92570-5 .... 0°C to +70°C

**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications

D.C.

SYMBOL	PARAMETER	TEMP. & VCC OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current		3.5	mA	IO = 0 VI = VCC or GND
ICCOP	Operating Supply Current ② 16K x 16		35	mA	$\bar{E}$ = 1MHz, IO = 0 VI = VCC or GND, $\bar{G}$ = VCC
ICCOP	Operating Supply Current ② 32K x 8		20	mA	$\bar{E}$ = 1MHz, IO = 0 VI = VCC or GND, $\bar{G}$ = VCC
ICCDR	Data Retention Supply Current		2.5	mA	IO = 0, VCC = 2.0, VI = VCC or GND, $\bar{E}$ = VCC
VCCDR	Data Retention Supply Voltage	2.0		V	
II	Input Leakage Current	-10.0	+10.0	μA	VI = VCC or GND
IIOZ	Input/Output Leakage Current	-10.0	+10.0	μA	VIO = VCC or GND
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	3.5	VCC +0.3	V	
VOL	Output Low Voltage		0.4	V	IO = 3.2mA
VOH	Output High Voltage	2.4		V	IO = -1.0mA
CIA	Address Input ③ Capacitance		50	pF	VI = VCC or GND f = 1MHz
CIE1	Decoder Enable Input ③ Capacitance (16K x 16)		50	pF	VI = VCC or GND f = 1MHz
CIE2	Decoder Enable Input ③ Capacitance (32K x 8)		25	pF	VI = VCC or GND f = 1MHz
CIG 1	Output Enable Input ③ Capacitance (16K x 16)		50	pF	VI = VCC or GND f = 1MHz
CIG 2	Output Enable Input ③ Capacitance (32K x 8)		25	pF	VI = VCC or GND f = 1MHz
CIO1	Input/Output ③ Capacitance (16K x 16)		150	pF	VI/O = VCC or GND f = 1MHz
CIO2	Input/Output ③ Capacitance (32K x 8)		250	pF	VI/O = VCC or GND f = 1MHz
CIW	Write Input ③ Capacitance		25	pF	VI = VCC or GND f = 1MHz
CVcc	Decoupling Capacitance	0.5		μF	f = 1MHz

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) ....-0.3V to +8.0V
Input or Output Voltage Applied .... (GND -0.3V) to (VCC +0.3V)
Storage Temperature ....-65°C to +150°C

Operating Range

Operating Supply Voltage
HM5-92570-5 .... 4.5V to 5.5V
Operating Temperature
HM5-92570-5 .... 0°C to +70°C

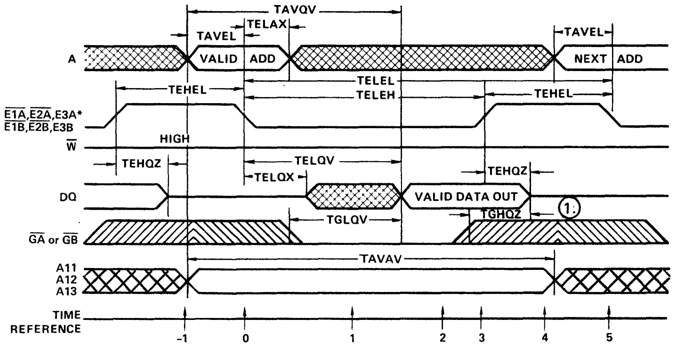
**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications

	SYMBOL	PARAMETER	TEMP. & VCC OPERATING RANGE ① MIN	MAX	UNITS	TEST CONDITIONS
A.C.	TELQV	Chip Enable Access Time		300	ns	④
	TAVQV	Address Access Time		320	ns	④
	TELQX	Chip Enable Output Enable Time	10		ns	③④
	TEHQZ	Chip Enable Output Disable Time		200	ns	③④
	TGLQX	Output Enable Output Enable Time	10		ns	③④
	TGLQV	Output Enable Output Valid Time		120	ns	④
	TGHQZ	Output Enable Output Disable Time		200	ns	③④
	TELEH	Chip Enable Pulse Negative Width	300		ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		ns	④
	TAVEL	Address Setup Time	20		ns	④ ⑤
	TELAX	Address Hold Time	130		ns	④
	TWLWH	Write Enable Pulse Width	150		ns	④
	TWLEH	Write Enable Pulse Setup Time	150		ns	④
	TELWH	Write Enable Pulse Hold Time	300		ns	④
	TDVWH	Data Setup Time	30		ns	④
	TWHDX	Data Hold Time	80		ns	④
	TWLDV	Write Data Delay Time	120		ns	④
	TELEL	Read or Write Cycle Time	450		ns	④
	TAVAV	Enable Decoder Address Valid Time	320		ns	Applies Only to A11, A12, A13

NOTES:
① All devices tested at worst case temperature and V_{CC}.
② Operating supply current (ICCOP) is proportional to operating frequency.
③ Tested at initial design and after major design changes.
④ Input pulse levels: 0V to 3.5V. Input rise and fall times: 10ns max. Input and output timing reference levels: 1.5V. Output load: C_L = 50 to 300pF. For C_L greater than 50pF, access time is derated 0.15ns/pF.
⑤ Includes A11, A12, A13.

Read Cycles

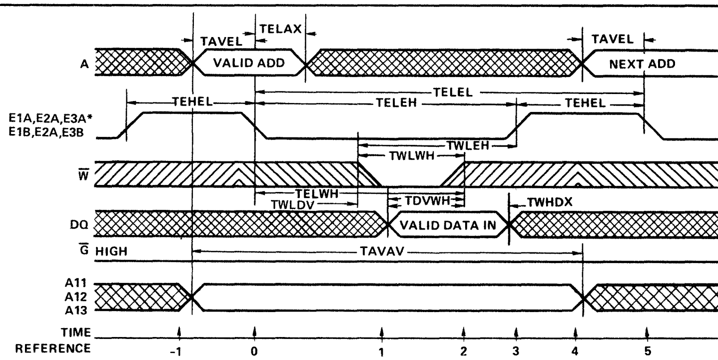


TRUTH TABLE

TIME REFERENCE	$\overline{E}$	$\overline{W}$	$\overline{G}$	A	A11 A12 A13	DATA I/O DQ	FUNCTION
-1	H	X	X	X	X	Z	MEMORY DISABLED
0	↓	H	X	V	V	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	H	L	X	V	X	OUTPUT ENABLED
2	L	H	L	X	V	V	OUTPUT VALID
3	↑	H	X	X	V	V	READ ACCOMPLISHED
4	H	X	X	X	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↓	H	X	V	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The address information is latched in the on chip registers on the falling edge of $\overline{E}$(T = 0), minimum address setup and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1), the outputs become enabled but data is not valid until time (T = 2), $\overline{W}$ must remain high throughout the read cycle. After the data has been read, E may return high (T = 3). This will force the output buffers into a high impedance mode at time (T = 4). $\overline{G}$ is used to disable the output buffers when in a logical "1" state (T = -1, 0, 3, 4, 5). After T = 4) time, the memory is ready for the next cycle. *E3A and E3B are opposite polarity of $\overline{E1A}$.

Write Cycles



TRUTH TABLE

TIME REFERENCE	$\overline{E}$	$\overline{W}$	$\overline{G}$	A	A11 A12 A13	DATA I/O DQ	FUNCTION
-1	H	X	H	X	X	X	MEMORY DISABLED
0	↓	X	H	V	V	X	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	L	H	X	V	X	WRITE PERIOD BEGINS
2	L	↑	H	X	V	V	DATA IN IS WRITTEN
3	↑	H	H	X	V	X	WRITE COMPLETED
4	H	X	H	X	X	X	PREPARE FOR NEXT CYCLE (SAME AS -1)
5	↓	X	H	V	V	X	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

The write cycle is initiated on the falling edge of E(T = 0), which latches the address information in the on chip registers. If a write cycle is to be performed where the output is not to become active, $\overline{G}$ can be held high (inactive). TDVWH and TWHDX must be met for proper device operation regardless of $\overline{G}$. If $\overline{E}$ and $\overline{G}$ fall before $\overline{W}$ falls (read mode), a possible bus conflict may exist. If $\overline{E}$ rises before $\overline{W}$ rises, reference data setup and hold times to the $\overline{E}$ rising edge. The write operation is terminated by the first rising edge of $\overline{W}$ (T = 2) or $\overline{E}$(T = 3). After the minimum $\overline{E}$ high time (TEHEL), the next cycle may begin. If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may be held low until all desired locations have been written. In this case, data setup and hold times must be referenced to the rising edge of $\overline{E}$. *E3A and E3B are opposite polarity of $\overline{E1A}$.

HM-6641

512 x 8 CMOS PROM

Features

- **Low Power Standby .... 500μW Max.**
- **Low Power Operation .... 50mW/MHz Max.**
- **Fast Access Time .... 250ns Max.**
- **Field Programmable**
- **Polysilicon Fuse Links**
- **TTL Compatible In/Out**
- **Popular Pinout Like Bipolar 7641**
- **Three State Outputs**
- **Address Latches Included on Chip**
- **Easy Microprocessor Interfacing**
- **Wide Operating Temperature Ranges:**
  - **HM-6641-9 .... -40°C to +85°C**
  - **HM-6641-2/-8 .... -55°C to +125°C**

Description

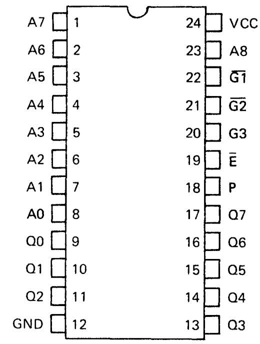
The HM-6641 is a 512 x 8 CMOS polysilicon fusible link Programmable Read Only Memory in the popular 24 pin, byte wide pinout. Synchronous circuit design techniques combine with CMOS processing to give this device high speed performance with very low power dissipation.

On chip address latches are provided, allowing easy interfacing with recent generation microprocessors that use multiplexed address/data bus structures, such as the 8085. The output enable controls, both active low and active high, further simplify microprocessor system interfacing by allowing output data bus control independent of the chip enable control. The data output latches allow the use of the HM-6641 in high speed pipelined architecture systems, and also in synchronous logic replacement functions.

Applications for the HM-6641 CMOS PROM include low power handheld microprocessor based instrumentation and communications systems, remote data acquisition and processing systems, processor control store, and synchronous logic replacement.

Pinouts

TOP VIEW

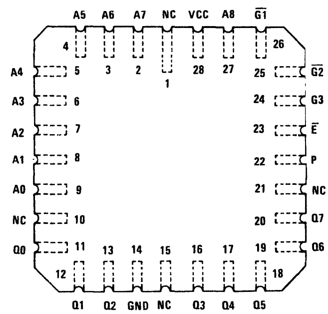


PIN NAMES

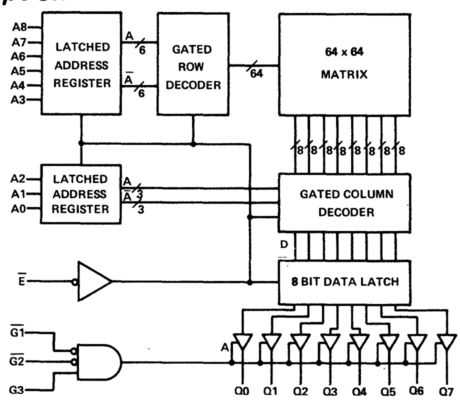
A Address Input	G̅ Output Enable
Q Data Output	P Program Enable
E̅ Chip Enable	(P = GND except during Programming)
NC No Connect	

LCC

TOP VIEW



Functional Description



ALL LINES POSITIVE LOGIC - ACTIVE HIGH

THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE

DATA LATCHES:
L HIGH → Q = D
Q LATCHES ON RISING EDGE OF E̅

ADDRESS LATCHES AND GATED DECODERS:
LATCH ON FALLING EDGE OF E̅
GATE ON FALLING EDGE OF E̅

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow standard IC Handling Procedures.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) .... +8.0V
Input or Output Voltage Applied .... (GND -0.3V) to (VCC +0.3V)
Storage Temperature .... -65°C to +150°C

Operating Range

Operating Supply Voltage
HM-6641-2/-8 .... 4.5V to 5.5V
HM-6641-9 .... 4.5V to 5.5V
Operating Temperature
HM-6641-2/-8 .... -55°C to +125°C
HM-6641-9 .... -40°C to +85°C

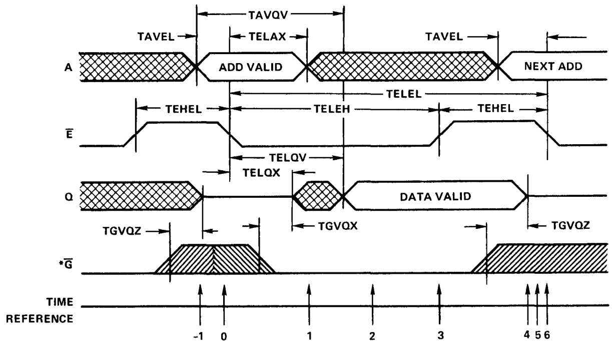
*CAUTION: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Electrical Specifications ①

SYMBOL	PARAMETER	TEMP & VCC = OPERATING RANGE MIN	MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current		100	μA	IO = 0 ⑥ VI = GND OR VCC
ICCOP	Operating Supply Current ②		15	mA	f = 1MHz, IO = 0 ⑥ VI = VCC or GND
II	Input Leakage Current	-1.0	+1.0	μA	GND≤VI≤VCC ⑥
IOZ	Output Leakage Current	-1.0	+1.0	μA	GND≤VO≤VCC ⑥
VIL	Input Low Voltage	-0.3	0.8	V	⑤
VIH	Input High Voltage	VCC-2.0	VCC+0.3	V	⑤
VOL	Output Low Voltage		0.4	V	IOL = 3.2mA ⑤
VOH	Output High Voltage	2.4		V	IOH = -1.0mA ⑤
CI	Input Capacitance ③		10.0	pF	VI = VCC or GND f = 1MHz
CO	Output Capacitance ③		12.0	pF	VO = VCC OR GND f = 1MHz
TELQV	Chip Enable Access Time		250	ns	④ ⑤ ⑥
TAVQV	(TAVQV = TELQV + TAVEL) Address Access Time		270	ns	④ ⑤ ⑥
TELQX	Chip Enable Time	20	150	ns	③ ④
TGVQX	Output Enable Time	20	150	ns	③ ④
TGXQZ	Output Disable Time	20	150	ns	③ ④
TELEH	Chip Enable Pulse Negative Width	250		ns	④ ⑤ ⑥
TELEL	Read Cycle Time	400		ns	④ ⑤ ⑥
TEHEL	Chip Enable Pulse Positive Width	150		ns	④ ⑤ ⑥
TAVEL	Address Set-up Time	20		ns	④ ⑤ ⑥
TELAX	Address Hold Time	60		ns	④ ⑤ ⑥

NOTES:
① All devices tested at worst case temperature and VCC limits.
② Typical derating: 15mA/MHz increase in ICCOP. VI = VCC or GND.
③ Tested at initial design and after major design changes.
④ Input pulse levels: 0.0V to 3.0V, Input and Output timing reference levels: 1.5V, Input rise and fall times: ≤5ns, Output load: 1 TTL gate equivalent and CL = 50 to 300pF. For CL > 50pF, access times are derated by 0.15 ns per pF. Output load for output enable/disable times = 1TTL Gate equivalent and CL = 50 to 300pF. (including scope and jig).
⑤ VCC = 4.5V.
⑥ VCC = 5.5V.

Read Cycle



*G HAS SAME TIMING AS $\overline{G}$ EXCEPT SIGNAL IS INVERTED

TRUTH TABLE

TIME REFERENCE	INPUTS E	G	A	OUTPUTS O	FUNCTION
-1	H	H	X	Z	MEMORY DISABLED
0	↓	H	V	Z	CYCLE BEGINS-ADDRESSES ARE LATCHED
1	L	L	X	X	OUTPUT ENABLED
2	L	L	X	V	OUTPUT VALID
3	↑	L	X	V	OUTPUT LATCHED
4	H	H	X	Z	READ ACCOMPLISHED AND OUTPUT DISABLED
5	H	H	X	Z	PREPARE FOR NEXT CYCLE (SAME AS -1)
6	↓	H	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

In the HM-6641 read cycle, the address information is latched into the on chip registers on the falling edge of $\overline{E}$(T = 0). Minimum address setup and hold time requirements must be met. After the required hold time,the addresses may change state without affecting device operation. To read data $\overline{G1}$ and $\overline{G2}$ must be low, and G3 must be high. After access time, $\overline{E}$ may be taken high to latch the data outputs and begin TEHEL. Taking either or both $\overline{G1}$ or $\overline{G2}$ high or G3 low will force the output buffers to a high impedance state. The output data may be re-enabled at any time taking $\overline{G1}$ and $\overline{G2}$ low and G3 high. On the falling edge of $\overline{E}$ the data will be unlatched. P should be grounded except when in the programming mode.

Programming

INTRODUCTION

The HM-6641 is a 512 word, by 8 bit field programmable read only memory utilizing polycrystalline silicon fusible links as programmable memory elements. Selected memory locations are permanently changed from their manufactured state, of all low (VOL) to a logical high (VOH), by the controlled application of programming potentials and pulses. Careful adherence to the following programming specifications will result in high programming yield. Both high VCC (6.0 volts) and low VCC (4.0 volts) verify cycles are specified to assure the integrity of the programmed fuse. This programming specification, although complete, does not preclude rapid programming. The worst case programming time required is 37.4 seconds, and typical programming time can be approximately 4 seconds per device.

The chip ($\overline{E}$) and output enable ($\overline{G}$) are used during the programming procedure. On PROM's which have more than one output enable control $\overline{G1}$ is to be used. The other output enables must be held in the active, or enabled, state throughout the entire programming sequence. The programmer designer is advised that all pins of the programmer's socket should be at ground potential when the PROM is inserted into the socket. VCC must be applied to the PROM before any input or output pin is allowed to rise*.

OVERALL PROGRAMMING PROCEDURE

1. The address of the first bit to be programmed is presented, and latched by the chip enable ($\overline{E}$) falling edge. The output is disabled by taking the output enable ($\overline{G}$) high.
2. VCC is raised to the programming voltage level, 12.5V.
3. The data output pin corresponding to the bit to be programmed is pulled low. All other bits in the word are pulled up to VCC (at the programming level).
4. A 500 μs pulse is applied to the programming control pin (P).
5. The data output pin is returned to VCC, and the VCC pin is returned to 6.0 volts.

6. The address of the bit is again presented, and latched by a second chip enable falling edge.

7. The data outputs are enabled, and read, to verify that the bit was successfully programmed.
   a). If verified, two post programming pulses are applied (the bit is programmed twice more). Then the next bit to be programmed is addressed and programmed.
   b). If not verified, the program/verify sequence is repeated up to 8 times total, at the programming voltage level, 12.5 volts.
   c). If data is not verified, the programming voltage is increased to +14.0 volts. The program/verify sequence is then repeated up to 8 additional times.

8. After all bits to be programmed have been verified at 6.0 volts, the VCC is lowered to 4.0 volts and all bits are verified.
   a). If all bits verify, the device is properly programmed.
   b). If any bit fails to verify, the device is rejected.

PROGRAMMING SYSTEM REQUIREMENTS

1. The power supply for the device to be programmed must be able to be set to four voltages; 4.0V, 6.0V, 12.5V, 14.0V. This supply must be able to supply 500mA average, and 1A dynamic, currents to the PROM during programming. The power supply rise fall times when switching between voltages must be no quicker than 1μs.

2. The address drivers must be able to maintain input voltage levels ≥70% VCC for VIH, and ≤20% VCC for VIL. The programming system designer has a choice between buffers that will track VCC up and down (e.g. open collector buffers with pull up resistors) or buffers used for VIH only at 4.0V and 6.0V and returned to VIL when the system is at programing voltages.*

3. The control input buffers have the same 70% and 20% VCC requirements as the address buffers. Notice that chip enable ($\overline{E}$) does not require a pull up to programming voltage levels, but that the output enable ($\overline{G}$) must have a pull up to track VCC up and down. The program control (P) must switch from ground to programming VCC level.*

4. The data input buffers must be able to sink up to 3mA from the PROM's output pins without rising more than 0.7 volts above ground, be able to hold the other outputs high with a current source capability of 0.5mA to 2.0mA, and not interfere with the reading and verifying of the data output of the PROM. Notice that a bit to be programmed is changed from a low state (VOL) to high (VOH) by pulling low on the output pin. A suggested implementation is open collector TTL buffers (or inverters) with 4.7KΩ pull up resistors to VCC.*

*Note: Never allow any input or output pin to rise more than 0.3 volts above VCC, or fall more than 0.3 volts below ground.

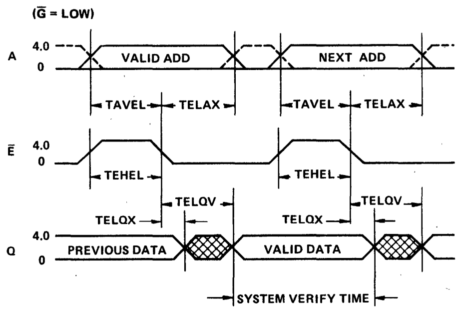
Programming System Specifications

PARAMETER	NAME	MIN	TARGET	MAX	UNITS
VCCN	Normal VCC	5.75	6.0	6.25	volts
VCC PGM	Programming Voltage	12.0	12.0	12.5	volts
VCC LV	Low Voltage Verify VCC	3.75	4.0	4.25	volts
ICC	System ICC Capability	500			mA
ICC Peak	Transient ICC Capability	1.0			A
	For PROM Input Pins:				
VOL	Output Low Voltage (to PROM)	-0.3	GND	20% VCC	volts
VOH	Output High Voltage (to PROM)	70% VCC	VCC	VCC +0.3	volts
IOL	Output Sink Current (at VOL)	.01			mA
IOH	Output Source Current (At VOH)	.01			mA
	For PROM Data Output Pins:				
VOL	Output Low Voltage (to PROM)	-0.3	GND	0.7	volts
VOH	Output High Voltage (to PROM)	70% VCC	VCC	VCC +0.3	volts
IOL	Output Sink Current (at VOL)	3.0			mA
IOH	Output Source Current (at VOH)	0.5	1.0	2.0	mA

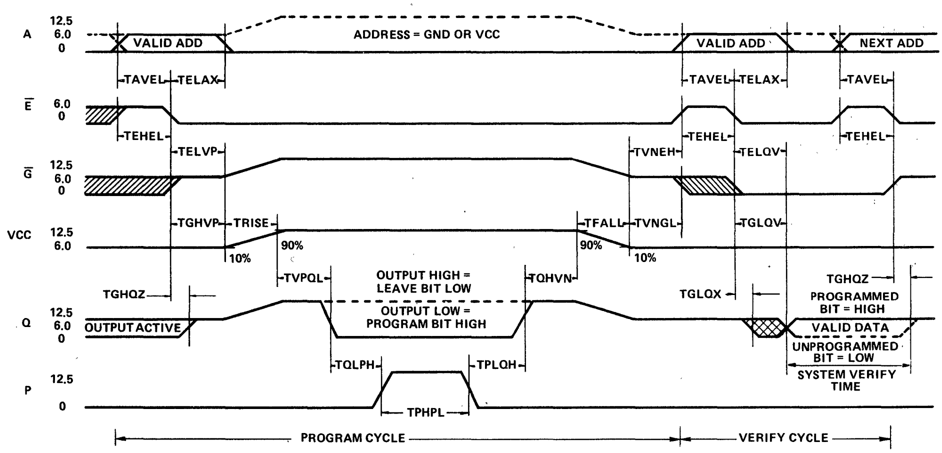
Programming System Timing

SYMBOLS	PARAMETER	MIN	MAX	UNITS
TAVEL	Address Set-up Time	500		ns
TELAX	Address Hold Time	500		ns
TEHEL	Chip Enable High Time	500		ns
TELVP	Chip Enable Low to VCC Rising Delay	500		ns
TGHVP	Output Enable High to VCC Rising Delay	500		ns
TGHQZ	Output Disable Time		150	ns
TRISE	VCC Rise Time (to PGM Voltage)	1.0		μs
TVPQL	VCC High (PGM) to Output Low Delay	500		ns
TQLPH	Programming Data Setup Time	500		ns
TPHPL	Programming Pulse Width	450	550	μs
TPLQH	Programming Data Hold Time	500		ns
TQHVN	Output High to VCC Normal Delay	500		ns
TFALL	VCC Fall Time (to Normal VCC)	1.0		μs
TVNEH	VCC Normal to Chip Enable High Delay	500		ns
TVNGL	VCC Normal to Output Enable Low Delay	500		ns
TELQV	Chip Enable Access Time		500	ns
TGLQV	Output Enable Access Time		500	ns
TGLQX	Output Enable Time		150	ns

Low Voltage Verify Cycle



Program and Verify Cycle



HARRIS

HM-6616

2K x 8 CMOS PROM

Features

- Low Standby and Operating Power
  - ICCSB - 100µA
  - ICCOP - 15mA/MHz
- Fast Access Time 90/120nsec
- Industry Standard Pinout
- Single 5.0 Volt Supply
- TTL Compatible Inputs
- High Output Drive .... 12 LSTTL Loads
- Synchronous Operation
- On-Chip Address Latches
- Seperate Output Enable
- Wide Operating Temperature Ranges:
  - HM-6616-9 .... -40°C to +85°C
  - HM-6616-2/-8 .... -55°C to +125°C

Description

The HM-6616 is a 16,384 bit fuse link CMOS PROM in a 2K word by 8 bit/word format with "Three State" outputs. This PROM is available in the standard 0.600 inch wide 24-Pin DIP, the 0.300 inch wide slimline DIP, and the JEDEC standard 32-Pin LCC.

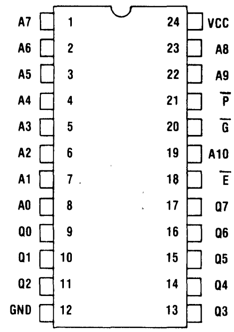
The HM-6616 utilizes a synchronous design technique. This includes on-chip address latches and a separate output enable control which makes this device ideal for applications utilizing recent generation microprocessors. This design technique, combined with the Harris advanced self-aligned silicon gate CMOS process technology offers ultra-low standby current. Low ICCSB is ideal for battery applications or other systems with low power requirements.

The Harris polysilicon fuse link technology is utilized on this and other Harris CMOS PROMS. This gives the user a PROM with permanent, stable storage characteristics over the full industrial and military temperature and voltage ranges. Polysilicon fuse technology combined with the low power characteristics of CMOS provides an excellent alternative to standard Bipolar PROMS or NMOS EPROMS.

All bits are manufactured storing a logical "0" and can be selectively programmed for a logical "1" at any bit location.

Pinouts

TOP VIEW

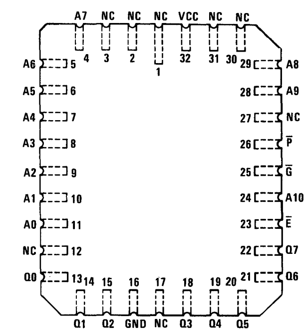


PIN NAMES

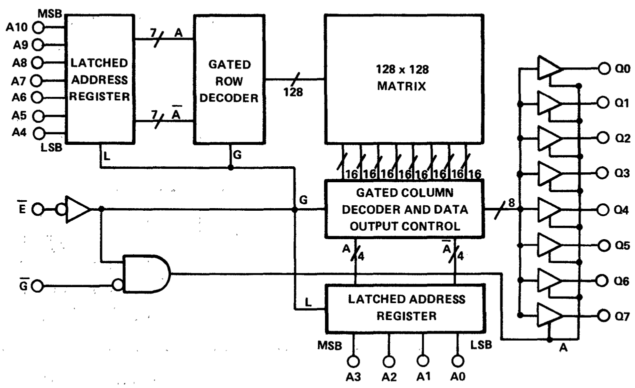
A Address Input
Q Data Output
Ē Chip Enable
Ḡ Output Enable
P̄ Program Enable
(P̄ = VCC except during Programming)

LCC

TOP VIEW



Functional Diagram



ALL LINES POSITIVE LOGIC:
ACTIVE HIGH
THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE
ADDRESS LATCHES & GATED DECODERS:
LATCH ON FALLING EDGE OF Ē
GATE ON FALLING EDGE OF Ḡ
P̄ = VCC EXCEPT DURING PROGRAMMING

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) .... +7.0V
Input or Output Voltage Applied .... (GND -0.3V) to (VCC +0.3V)
Storage Temperature ....-65°C to +150°C

Operating Range

Operating Temperature Range
HM-6616-2/-8 ....-55°C to +125°C
HM-6616-9 ....-40°C to +85°C

CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. Electrical Specifications

V_{CC} = 5.0V ±10%; T_A = -40°C to +85°C (HM-6616-9)
= -55°C to +125°C (HM-6616-2/-8)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	Logical One Input Voltage	2.4		V	④
VIL	Logical Zero Input Voltage		0.8	V	④
VOH	Logical One Output Voltage	2.4		V	IOH = −2.0 mA ④
VOL	Logical Zero Output Voltage		0.4	V	IOL = +4.8 mA ④
II	Input Leakage	−1.0	1.0	μA	VIN = VCC or GND ⑤
IOZ	Output Leakage	−1.0	1.0	μA	VO = VCC or GND ⑤ $\overline{G}$ = HIGH
ICCSB	Standby Power Supply Current		100	μA	VIN = VCC or GND VCC = 5.5 V IO = 0
ICCOP	Operating Power Supply Current		15	mA	f = 1 MHz VCC = 5.5 V IO = 0 VIN = VCC or GND
CIN	Input Capacitance②		10	pF	f = 1 MHz VIN = VCC = GND
COUT	Output Capactiance ②		12	pF	f = 1 MHz VIN = VCC = GND

A.C. Electrical Specifications ①③ V_{CC} = 5.0V ±10%; T_A = -40°C to +85°C (HM-6616-9)
= -55°C to +125°C (HM-6616-2/-8)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
TAVQV	Address Access Time		140	ns	④⑤
TELQV	Chip Enable Access Time		120	ns	④⑤
TELQX	Chip Enable Time	5		ns	②
TAVEL	Address Setup Time	20		ns	④⑤
TELAX	Address Hold Time	25		ns	④⑤
TELEH	Chip Enable Low Width	120		ns	④⑤
TEHEL	Chip Enable High Width	40		ns	④⑤
TELEL	Cycle Time	160		ns	④⑤
TGLQV	Output Access Time		50	ns	②
TGLQX	Output Enable Time	5		ns	②
TGHQZ	Output Disable Time		50	ns	②
TEHQZ	Chip Enable Disable Time		50	ns	②

Switching Waveforms

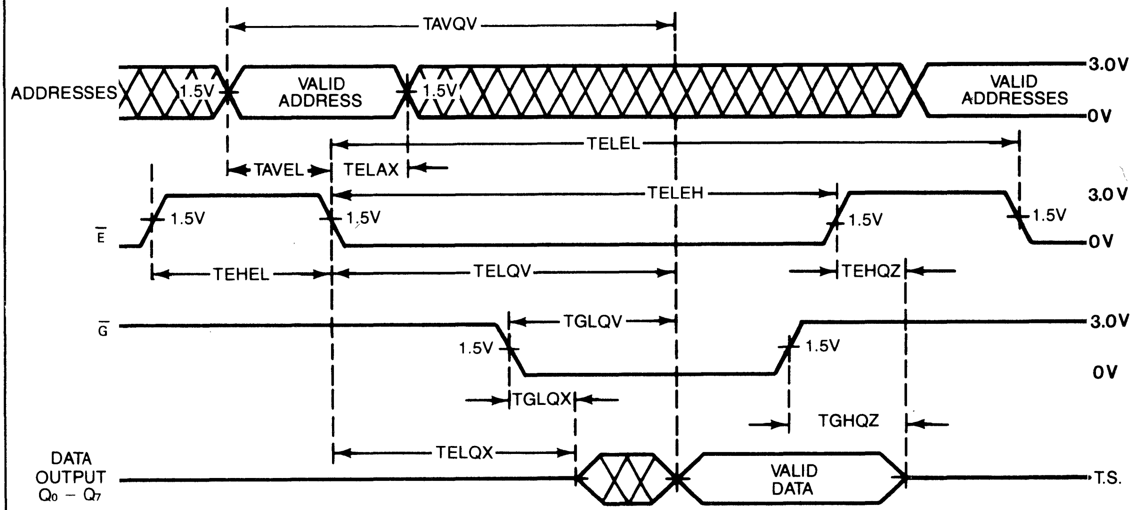


Figure 1 Read Cycle

NOTES:
① All devices tested at worst case temperature and VCC limits.
② Tested at initial design and after major design changes.
③ Input pulse levels: 0.0V to 3.0V, Input rise and fall times: 5ns max. Input and output timing reference levels: 1.5V. Output load: 1 TTL gate equivalent and CL = 50 to 300pF. For CL greater than 50pF, access times are derated by 0.15ns/pF. Output load for output enable/disable times: 1 TTL gate equivalent and CL = 5pF (min, including scope and jig).
④ VCC = 4.5V.
⑤ VCC = 5.5V.

Absolute Maximum Ratings*

Supply Voltage - (VCC - GND) .... +7.0V
Input or Output Voltage Applied.................. (GND -0.3V) to (VCC +0.3V)
Storage Temperature..............................-65°C to +150°C

Operating Range

Operating Temperature Range
HM-6616-2/-8 ....-55°C to +125°C
HM-6616-9 ....-40°C to +85°C

**CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

D.C. Electrical Specifications

VCC = 5.0V ± 10%;
HM-6616B-9 T_A = -40°C to +85°C
HM-6616B-2/-8 T_A = -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	Logical One Input Voltage	2.4		V	④
VIL	Logical Zero Input Voltage		0.8	V	④
VOH	Logical One Output Voltage	2.4		V	IOH = −2.0 mA ④
VOL	Logical Zero Output Voltage		0.4	V	IOL = +4.8 mA ④
II	Input Leakage	−1.0	1.0	μA	VIN = VCC or GND ⑤
IOZ	Output Leakage	−1.0	1.0	μA	VO = VCC or GND ⑤ $\overline{G}$ = HIGH
ICCSB	Standby Power Supply Current		100	μA	VIN = VCC or GND VCC = 5.5 V IO = 0
ICCOP	Operating Power Supply Current		15	mA	f = 1 MHz VCC = 5.5 V IO = 0 VIN = VCC or GND
CIN	Input Capacitance ②		10	pF	f = 1 MHz VIN = VCC = GND
COUT	Output Capactiance ②		12	pF	f = 1 MHz VIN = VCC = GND

A.C. Electrical Specifications ① ③ VCC = 5.0V ± 10%;
HM-6616B-9 T_A = -40°C to +85°C
HM-6616B-2/-8 T_A = -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
TAVQV	Address Access Time		105	ns	④ ⑤
TELQV	Chip Enable Access Time		90	ns	④ ⑤
TELQX	Chip Enable Time	5		ns	②
TAVEL	Address Setup Time	15		ns	④ ⑤
TELAX	Address Hold Time	20		ns	④ ⑤
TELEH	Chip Enable Low Width	95		ns	④ ⑤
TEHEL	Chip Enable High Width	40		ns	④ ⑤
TELEL	Cycle Time	135		ns	④ ⑤
TGLQV	Output Access Time		40	ns	②
TGLQX	Output Enable Time	5		ns	②
TGHQZ	Output Disable Time		40	ns	②
TEHQZ	Chip Enable Disable Time		45	ns	②

Switching Waveforms

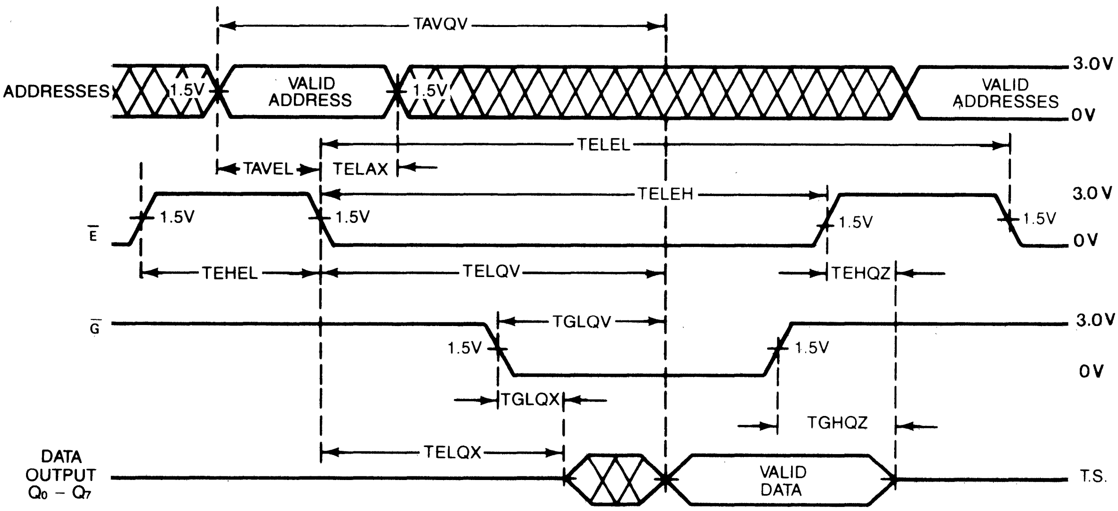


Figure 1 Read Cycle

NOTES:
① All devices tested at worst case temperature and VCC limits.
② Tested at initial design and after major design changes.
③ Input pulse levels: 0.0V to 3.0V, Input rise and fall times: 5ns max. Input and output timing reference levels: 1.5V. Output load: 1 TTL gate equivalent and CL = 50 to 300pF. For CL greater than 50pF, access times are derated by 0.15ns/pF. Output load for output enable/disable times: 1 TTL gate equivalent and CL = 5pF (min, including scope and jig).
④ VCC = 4.5V.
⑤ VCC = 5.5V.

CMOS PROM Programming Algorithm

The HM-6616 PROM is manufactured with all bits storing a logical "0" (output low). Any desired bit can be selectively programmed to a logical "1" (output high) by following the procedure shown below. One may build their own programmer to satisfy the specifications shown, or use any of the approved commercially available programmers.

PROGRAM SEQUENCE OF EVENTS

1) Apply V_{CC}(pin 24) = VCC1 to the PROM.
2) Read all fuse locations to verify (blank check) a 100% V_{OL} (unprogrammed) condition.
3) Place the PROM in the initial state for programming. $\overline{E}$ = VIH, $\overline{P}$ = VIH, $\overline{G}$ = VIL.
4) Apply the current binary address for the word to be programmed. An open circuit should not be used to address the PROM.
5) Apply $\overline{E}$ = VIL after a delay of td to access the addressed word.
6) Address may be held throughout cycle, but must be held at least time td (address hold time), after $\overline{E}$ = VIL.
7) After a delay of td tristate the outputs by applying $\overline{G}$ = VIH.
8) After a delay of td apply $\overline{P}$ = VIL.
9) After a delay of td raise VCC(pin 24) to VCCPROG with rise time = tr. All signals at VIH should track VCC(pin 24) within VCC-2V to VCC+0.3V (including outputs - pull-up resistors Rn to VCC would suffice).
10) After a delay of td pull the output to be programmed to VIL. After a duration tpw, allow the output to be pulled to VIH through the pull-up resistor Rn.
11) Repeat step 10 for all other bits to be programmed in the addressed word.
12) Lower Vcc(pin 24) to VCC1 with a fall time tf. Signals at VIH should track VCC (pin 24) in range VCC-2V to VCC+0.3V.
13) After a delay of td apply $\overline{E}$ = VIH for duration of TEHEL, and the apply $\overline{E}$ = VIL.
14) After a delay = TELPH1, apply $\overline{P}$ = VIH.
15) After a delay of td apply $\overline{G}$ = VIL. Following a delay of td examine the outputs for correct data.
16) If any location verifies incorrectly, repeat steps 4 through 15 (attempting to program only those bits in the word which verified incorrectly) up to a maximum of eight attempts for any given word. If a word does not program within eight attempts, it should be considered a programming reject.
17) Repeat steps 4 through 16 for all other words in the PROM.

POST PROGRAMMING VERIFICATION

18) Place the PROM in the post-programming verify mode. $\overline{E}$ = VIH, $\overline{G}$ = VIL, $\overline{P}$ = VIH. VCC(pin 24) = VCC1.
19) Apply the correct binary address of the word to be verified.
20) After a delay of td, apply $\overline{E}$ = VIL.
21) After a delay of td apply $\overline{G}$ = VIH to disable the outputs (outputs are tied to VCC through pull-up resistors Rn).
22) After a delay of td apply $\overline{P}$ = VIL.
23) After a delay of td apply $\overline{E}$ = VIH for duration TEHEL, then apply $\overline{E}$ = VIL.
24) After a delay = TELPH2 apply $\overline{P}$ = VIH.
25) After a delay of td apply $\overline{G}$ = VIL to enable the outputs. After a delay of td examine the outputs for correct data.
26) Repeat steps 19 through 25 for all possible address locations.

POST PROGRAMMING READ

27) Apply VCC2 = 4.0V to VCC(pin 24).
28) After a delay of td, apply $\overline{E}$ = VIH.
29) Apply the correct binary address of the word to be read.
30) After a delay of TAVEL, apply $\overline{E}$ = VIL.
31) After a delay of TELQV, examine the outputs for correct data. If any bit verifies incorrectly, the device is to be considered a programming reject.
32) Repeat steps 28 thru 31 for all other words in the PROM.
33) Repeat steps 27 thru 32 for VCC2 = 6.0V applied to VCC(pin 24).

Figure 3 — Programming and Verify Cycle

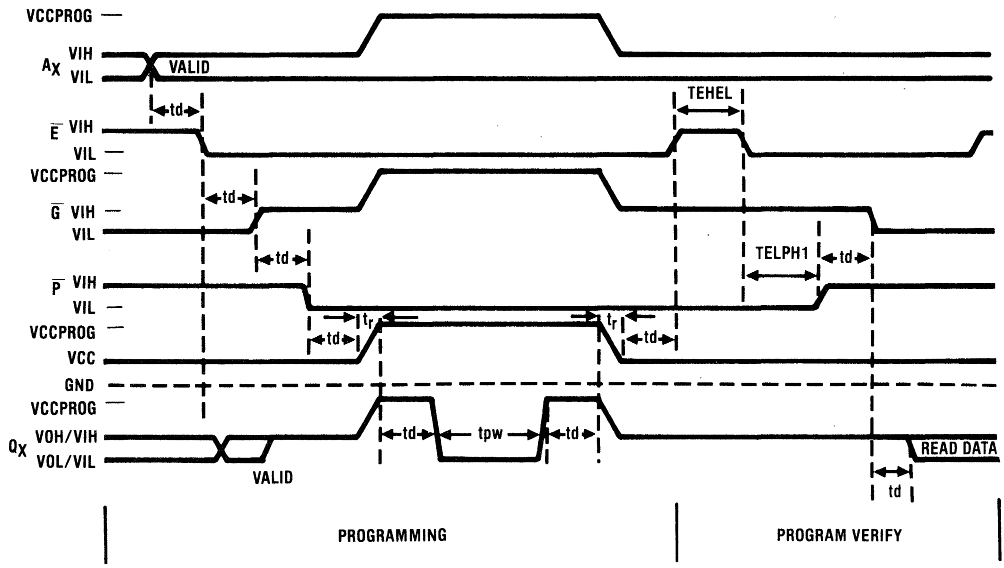
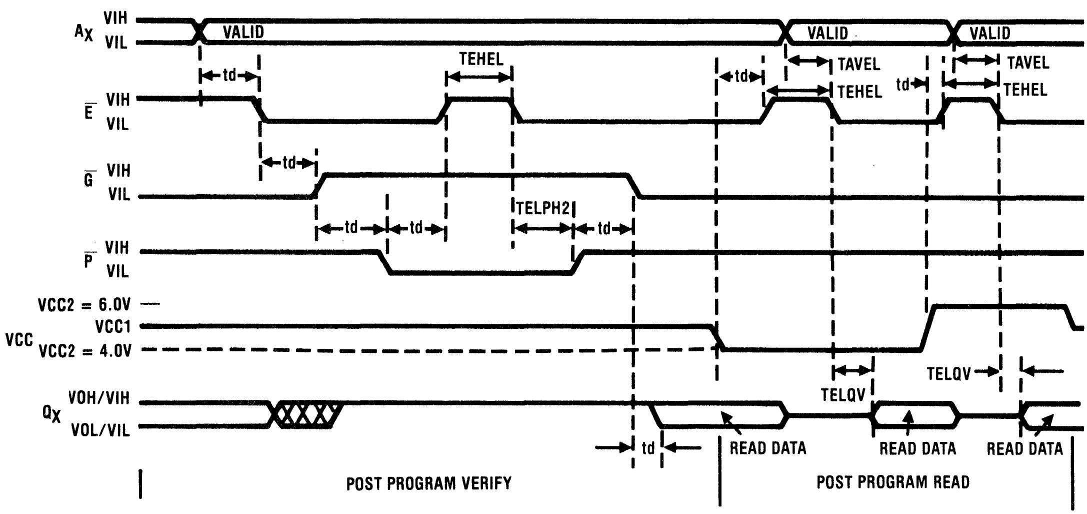


Figure 4 — Post Programming Verify & Read Cycle



Programming

SYMBOL	PARAMETER	MIN	TYP.	MAX.	UNITS
VIL VIH (1)	Input "0" Voltage "1"	0.0 VCC-2	0.2 VCC	0.8 VCC+0.3	V V
VCCPROG(2) VCC1 VCC2 (3)	Programming VCC Operating VCC Special Verify VCC	12.0 4.5 4.0	12.0 5.0 ----	12.5 5.5 6.0	V V V
td	Delay Time	1.0	1.0	----	us
tr tf	Programming VCC Rise and Fall Times	1.0 1.0	10.0 10.0	10.0 10.0	us us
TEHEL	Chip Enable Pulse Width	50	----	----	ns
TAVEL	Address valid to Chip Enable low time	20	----	----	ns
TELQV	Chip Enable low to Output Valid time	----	----	120	ns
TELPH1 (4) TELPH2 (5)	$\overline{E}$ Low to $\overline{P}$ High Time	400 5.0	500 5.0	600 10.0	us us
tpw (6)	Programming Pulse Width	0.9	1.0	1.1	ms
IIP	Input Leakage at VCC=VCCPROG	−10	+1.0	10	uA
IOP	Data Output Current at VCC = VCCProg	----	−5.0	−10	mA
Rn (7)	Output pull-up resistor	5	10	15	kohms
Ta	Ambient Temperature	----	25	----	°C

Notes:
1) All inputs must track VCC(pin 24) within these limits
2) VCCPROG must be capable of supplying 500mA.
3) See steps 27 thru 33 of the programming algorithm.
4) See steps 13 & 14 of the programming algorithm.
5) See steps 23 & 24 of the programming algorithm.
6) See step 10 of the programming algorithm.
7) All outputs should be pulled up to VCC thru a resistor of value Rn.

Data Entry Formats for Harris Custom Programming*

For Harris to custom program to a user data pattern specification, the user must supply the data in one of the following formats:

1. Master PROM of same organization and pinout as device ordered. Two pieces required, three preferred.
2. Paper tape in Binary or ASCII BPNF.

* BINARY PAPER TAPE FORMAT

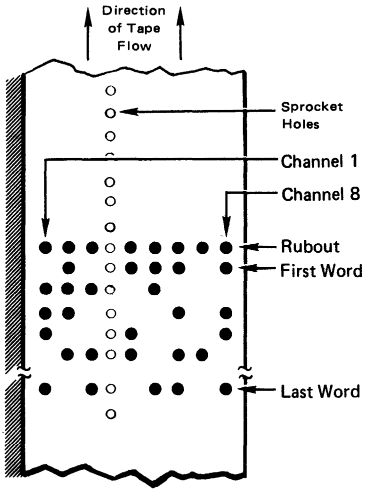
- A minimum of six inches of leader.
- A rubout (all eight locations punched).
- Data words beginning with the first word (word "0"), proceeding sequentially, ending with the last word (word "N"), with no interruptions or extraneous characters of any kind.
- Specify whether a punched hole is a VOH = "1" = logic high or is a VOL = "0" = logic low.
- A minimum trailer of six inches of tape.

* ASCII BPNF FORMAT

- A minimum leader of twenty rubouts (all eight locations punched).
- Any characters desired (none necessary) except "B".
- Data words beginning with the first word (word "0"), proceeding sequentially, ending with the last word (word "N").
- Data words consist of:
  1. The character "B" denoting the beginning of a data word.
  2. A sequence of characters, only "P" or "N", one character for each bit in the word.
  3. The character "F" denoting the finish of the data word.
- No extraneous characters of any kind may appear within a data word (between any "B" and the next "F").
- Errors may be deleted by rubouts superimposed over the entire word including the "B", and beginning the word again with a new "B".
- Any text of any kind (except the character "B") is allowed between data words (between any "F" and the next "B"), including carriage return and line feed.
- A minimum trailer of twenty-five rubouts.
- Specify whether a "P" is a "1" = VOH = logic high or is a "0" = VOL = logic low.
- The use of even or odd parity is optional.

* *Harris can not assume responsibility for PROMs programmed to data tapes or masters which contain errors. The user must insure the accuracy of the data provided to Harris. Harris guarantees that the programmed PROMs will contain the information provided if either of the following formats are followed.*

BINARY PAPER TAPE EXAMPLE



Punched Hole = "0" = VOL = Logic Low

Word				PROM Output Data ①							
				Channel	8	7	6	5	4	3	2	1
AX ···· A2	A1	A0		Output	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1
0 ···· 0	0	0	First		0	1	0	0	0	1	0	1
0 ···· 0	0	1	Second		1	1	1	0	1	0	0	0
0 ···· 0	1	0	Third		0	1	0	1	1	1	0	0
0 ···· 0	1	1	Fourth		0	1	1	1	0	1	1	0
0 ···· 1	0	0	Fifth		1	0	0	1	0	0	0	1
1 ···· 1	1	1	Last		0	1	0	0	1	0	1	0

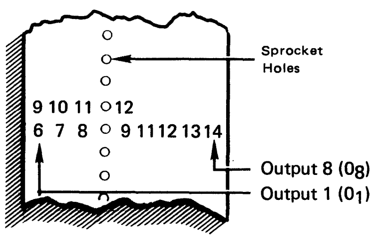
NOTES:

① PROMs with 4 bit wide data outputs require punching only first 4 channels on tape (Channels 1 thru 4).

② On HARRIS PROMs O_X (Example: O_1) designates a respective output pin on the device. O_1 (Output 1) is always LSB.

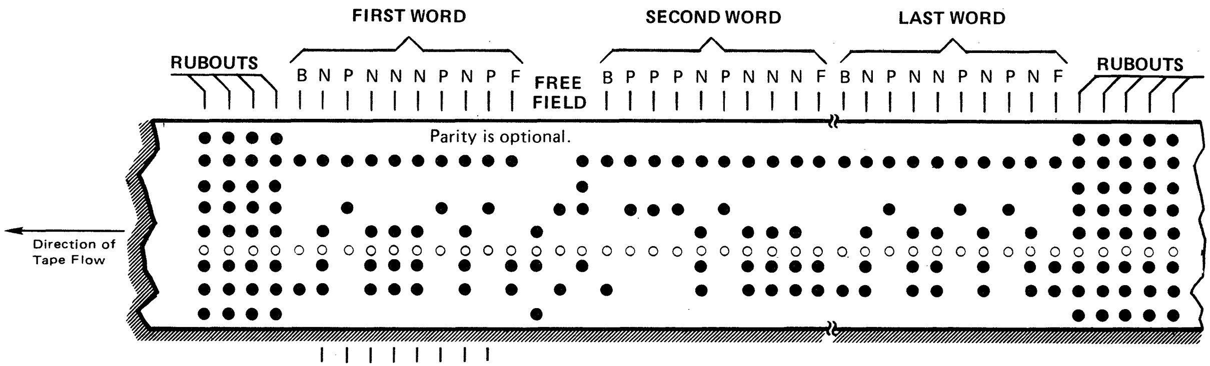
DEVICE OUTPUT PACKAGE PINS

EXAMPLE:



Package	Device Type
16 Pin CMOS	HM-6611

ASCII BPNF PAPER TAPE EXAMPLE



EXAMPLE	PACKAGE TYPE	DEVICE OUTPUT PINS
HM-6611	16 Pin Pkg.	12 11 10 9 (MOS)
HM-7649	20 Pin Pkg.	14 13 12 11 9 8 7 6

Truth Table
Character "D" = "1" = VOH = Logic High
Character "V" = "0" = VOL = Logic Low

Word					PROM Outputs Data ①							
AX ····	A2	A1	A0		O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1
0 ·····	0	0	0	First	0	1	0	0	0	1	0	1
0 ·····	0	0	1	Second	1	1	1	0	1	0	0	0
1 ·····	0	1	0	Last	0	1	0	0	1	0	1	0

NOTES:

① In the ASCII BPNF format, MSB data is punched after "B". On devices with 8 outputs, O_8 (Output 8) data is punched after "B" On devices with 4 outputs, O_4 (Output 4) data is punched after "B".

CMOS

CMOS 80C86 Family

3

PAGE

CMOS 80C86 FAMILY

80C86

CMOS 16 Bit Microprocessor

Features

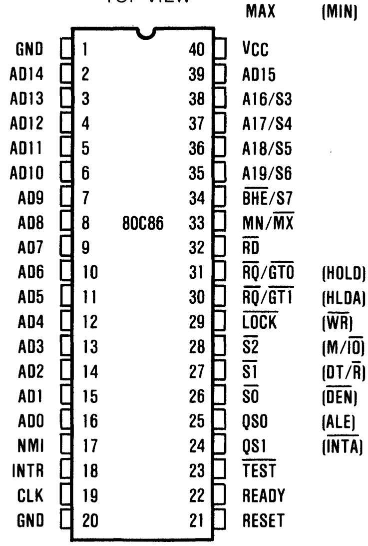
- **Compatible with NMOS 8086**
- **Completely Static CMOS Design**
  - ▸ **DC to 5MHz (80C86)**
  - ▸ **DC to 8MHz (80C86-2)**
- **Low Power Operation**
  - ▸ **ICCSB = 500μA Maximum**
  - ▸ **ICCOP = 10mA/MHz Typical**
- **1 MByte of Direct Memory Addressing Capability**
- **24 Operand Addressing Modes**
- **Bit, Byte, Word and Block Move Operations**
- **8 And 16 Bit Signed/Unsigned Arithmetic**
  - ▸ **Binary, or Decimal** ▸ **Multiply and Divide**
- **Wide Operating Temperature Ranges:**
  - ▸ **C80C86 .... 0°C to +70°C**
  - ▸ **I80C86 .... -40°C to +85°C**
  - ▸ **M80C86 .... -55°C to +125°C**

Description

The Harris 80C86 high performance 16 bit CMOS CPU is manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). Two modes of operation, MINimum for small systems and MAXimum for larger applications such as multi-processing, allow user configuration to achieve the highest performance level. Full TTL compatibility and industry standard operation allow use of existing NMOS 8086 hardware and software designs.

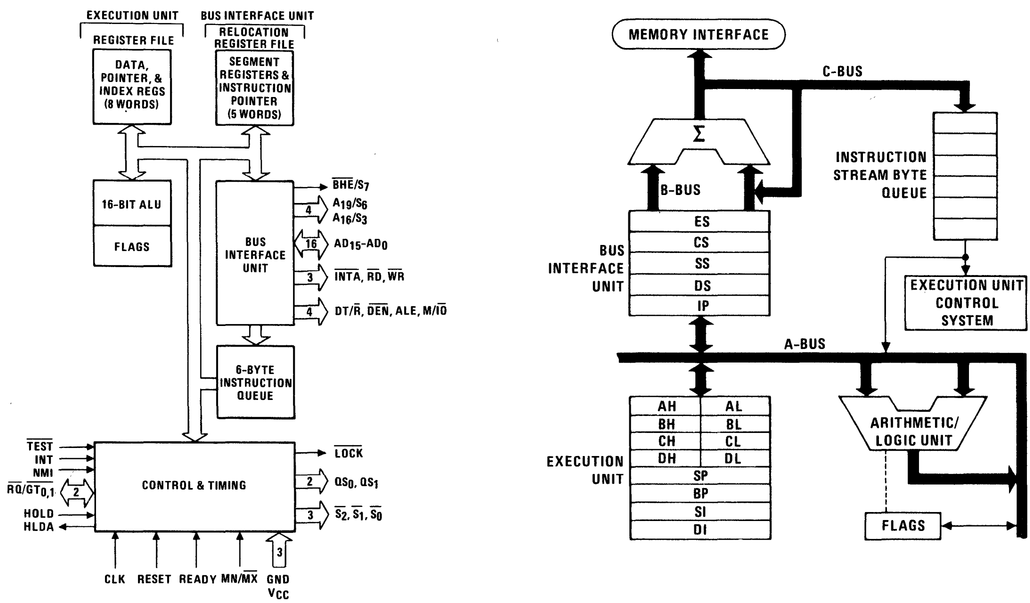
Pinout *

TOP VIEW



*LCC/PLCC Pinout on Page 3-19.

Functional Diagram



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Pin Description

The following pin function descriptions are for 80C86 systems in either minimum or maximum mode. The "Local Bus" in these descriptions is the direct multiplexed bus interface connection to the 80C86 (without regard to additional bus buffers).

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
AD_{15}-AD_0	2-16, 39	I/O	ADDRESS DATA BUS: These lines constitute the time multiplexed memory/IO address (T_1) and data (T_2, T_3, T_W, T_4) bus. A_0 is analogous to $\overline{BHE}$ for the lower byte of the data bus, pins D_7-D_0. It is LOW during T1 when a byte is to be transferred on the lower portion of the bus in memory or I/O operations. Eight-bit oriented devices tied to the lower half would normally use A_0 to condition chip select functions (See $\overline{BHE}$). These lines are active HIGH and are held at high impedance to the last valid logic level during interrupt acknowledge and local bus "hold acknowledge" or "grant sequence".
A_{19}/S_6 A_{18}/S_5 A_{17}/S_4 A_{16}/S_3	35-38	O	ADDRESSS/STATUS: During T_1, these are the four most significant address lines for memory operations. During I/O operations these lines are low. During memory and I/O operations, status information is available on these lines during T_2, T_3, T_W, T_4. S_6 is always zero. The status of the interrupt enable FLAG bit (S_5) is updated at the beginning of each CLK cycle. S_4 and S_3 are encoded as shown in (Table 1). This information indicates which segment register is presently being used for data accessing. These lines are held at high impedance to the last valid logic level during local bus "hold acknowledge" or "grant sequence".
$\overline{BHE}/S_7$	34	O	BUS HIGH ENABLE/STATUS: During T_1 the bus high enable signal ($\overline{BHE}$) should be used to enable data onto the most significant half of the data bus, pins D_{15}-D_8. Eight bit oriented devices tied to the upper half of the bus would normally use $\overline{BHE}$ to condition chip select functions. $\overline{BHE}$ is LOW during T_1 for read, write, and interrupt acknowledge cycles when a byte is to be transferred on the high portion of the bus. The S_7 status information is available during T_2, T_3 and T_4. The signal is active LOW, and is held at high impedance to the last valid logic level during interrupt acknowledge and local bus "hold acknowledge" or "grant sequence"; it is LOW during T_1 for the first interrupt acknowledge cycle. (See Table 2).
$\overline{RD}$	32	O	READ: Read strobe indicates that the processor is performing a memory or I/O read cycle, depending on the state of the $M/\overline{IO}$ or $\overline{S_2}$ pin. This signal is used to read devices which reside on the 80C86 local bus. $\overline{RD}$ is active LOW during T_2, T_3 and T_W of any read cycle, and is guaranteed to remain HIGH in T_2 until the 80C86 local bus has floated. This line is held at a high impedance logic one state during "hold acknowledge" or "grant sequence".
READY	22	I	READY: is the acknowledgement from the addressed memory or I/O device that will complete the data transfer. The RDY signal from memory or I/O is synchronized by the 82C84A Clock Generator to form READY. This signal is active HIGH. The 80C86 READY input is not synchronized. Correct operation is not guaranteed if the Setup and Hold Times are not met.
INTR	18	I	INTERRUPT REQUEST: is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. A subroutine is vectored to via an interrupt vector lookup table located in system memory. It can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized. This signal is active HIGH.
$\overline{TEST}$	23	I	TEST: input is examined by the "Wait" instruction. If the $\overline{TEST}$ input is LOW execution continues, otherwise the processor waits in an "Idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK.
NMI	17	I	NON-MASKABLE INTERRUPT: is an edge triggered input which causes a type 2 interrupt. A subroutine is vectored to via an interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized.
RESET	21	I	RESET: causes the processor to immediately terminate its present activity. The signal must transition LOW to HIGH and remain active HIGH for at least four clock cycles. It restarts execution, as described in the Instruction Set description, when RESET returns LOW. RESET is internally synchronized.
CLK	19	I	CLOCK: provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing.
VCC	40		VCC: +5V power supply pin. A 0.1μF capacitor between pins 20 and 40 is recommended for decoupling.
GND	1, 20		GND: Ground. Note: both must be connected. A 0.1μF capacitor between pins 1 and 20 is recommended for decoupling.
$MN/\overline{MX}$	33	I	MINIMUM/MAXIMUM: Indicates what mode the processor is to operate in. The two modes are discussed in the following sections.

Pin Description

The following pin function descriptions are for the 80C86/80C88 system in maximum mode (i.e., $MN/\overline{MX}$ = GND). Only the pin functions which are unique to maximum mode are described below.

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
$\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$	26-28	O	STATUS: is active during T_4, T_1 and T_2 and is returned to the passive state (1, 1, 1) during T_3 or during T_W when READY is HIGH. This status is used by the 82C88 Bus Controller to generate all memory and I/O access control signals. Any change by $\overline{S_2}$, $\overline{S_1}$ or $\overline{S_0}$ during T_4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T_3 or T_W is used to indicate the end of a bus cycle. These status lines are encoded as shown in Table 3. These signals are held at a high impedance logic one state during "grant sequence".
$\overline{RQ}/\overline{GT_0}$ $\overline{RQ}/\overline{GT_1}$	31, 30	I/O	REQUEST/GRANT: pins are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle. Each pin is bi-directional with $\overline{RQ}/\overline{GT_0}$ having higher priority than $\overline{RQ}/\overline{GT_1}$. $\overline{RQ}/\overline{GT}$ has an internal pull-up bus hold device so it may be left unconnected. The request/grant sequence is as follows (see $\overline{RQ}/\overline{GT}$ Sequence Timing) 1. A pulse of 1 CLK wide from another local bus master indicates a local bus request ("hold") to the 80C86 (pulse 1). 2. During a T_4 or T_I clock cycle, a pulse 1 CLK wide from the 80C86 to the requesting master (pulse 2) indicates that the 80C86 has allowed the local bus to float and that it will enter the "grant sequence" state at the next CLK. The CPU's bus interface unit is disconnected logically from the local bus during "grant sequence". 3. A pulse 1 CLK wide from the requesting master indicates to the 80C86 (pulse 3) that the "hold" request is about to end and that the 80C86 can reclaim the local bus at the next CLK. The CPU then enters T_4 (or T_I if no bus cycles pending). Each Master-Master exchange of the local bus is a sequence of 3 pulses. There must be one idle CLK cycle after each bus exchange. Pulses are active low. If the request is made while the CPU is performing a memory cycle, it will release the local bus during T_4 of the cycle when all the following conditions are met: 1. Request occurs on or before T_2. 2. Current cycle is not the low byte of a word (on an odd address). 3. Current cycle is not the first acknowledge of an interrupt acknowledge sequence. 4. A locked instruction is not currently executing. If the local bus is idle when the request is made the two possible events will follow: 1. Local bus will be released during the next cycle. 2. A memory cycle will start within three clocks. Now the four rules for a currently active memory cycle apply with condition number 1 already satisfied.
$\overline{LOCK}$	29	O	LOCK: output indicates that other system bus masters are not to gain control of the system bus while $\overline{LOCK}$ is active LOW. The $\overline{LOCK}$ signal is activated by the "LOCK" prefix instruction and remains active until the completion of the next instruction. This signal is active LOW, and is held at a HIGH impedance logic one state during "grant sequence". In MAX mode, $\overline{LOCK}$ is automatically generated during T_2 of the first INTA cycle and removed during T_2 of the second $\overline{INTA}$ cycle.
QS_1, QS_0	24, 25	O	QUEUE STATUS: The queue status is valid during the CLK cycle after which the queue operation is performed. QS_1 and QS_0 provide status to allow external tracking of the internal 80C86 instruction queue. Note that QS_1, QS_0 never become high impedance. **QS_1 / QS_0** 0 0 No Operation 0 1 First Byte of Op Code from Queue 1 0 Empty the Queue 1 1 Subsequent Byte from Queue

TABLE 1.

S_4	S_3	CHARACTERISTICS
0	0	Alternate Data
0	1	Stack
1	0	Code or None
1	1	Data

TABLE 2.

$\overline{BHE}$	A_0	CHARACTERISTICS
0	0	Whole word
0	1	Upper byte from/to odd address
1	0	Lower byte from/to even address
1	1	None

TABLE 3.

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	CHARACTERISTICS
0	0	0	Interrupt Acknowledge
0	0	1	Read I/O Port
0	1	0	Write I/O Port
0	1	1	Halt
1	0	0	Code Access
1	0	1	Read Memory
1	1	0	Write Memory
1	1	1	Passive

Pin Description

The following pin function descriptions are for the 80C86 in minimum mode (i.e. MN/$\overline{MX}$ = V_{CC}). Only the pin functions which are unique to minimum mode are described; all other pin functions are as described below.

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
M/$\overline{IO}$	28	O	STATUS LINE: logically equivalent to $\overline{S_2}$ in the maximum mode. It is used to distinguish a memory access from an I/O access. M/$\overline{IO}$ becomes valid in the T_4 preceding a bus cycle and remains valid until the final T_4 of the cycle (M = HIGH, IO = LOW). M/$\overline{IO}$ is held to a high impedance logic zero during local bus "hold acknowledge".
$\overline{WR}$	29	O	WRITE: indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the M/$\overline{IO}$ signal. $\overline{WR}$ is active for T_2, T_3 and TW of any write cycle. It is active LOW, and is held to high impedance logic one during local bus "hold acknowledge".
$\overline{INTA}$	24	O	INTERRUPT ACKNOWLEDGE: is used as a read strobe for interrupt acknowledge cycles. It is active LOW during T_2, T_3 and TW of each interrupt acknowledge cycle. Note that $\overline{INTA}$ is never floated.
ALE	25	O	ADDRESS LATCH ENABLE: is provided by the processor to latch the address into the 82C82/82C83 address latch. It is a HIGH pulse active during clock LOW of T1 of any bus cycle. Note that ALE is never floated.
DT/$\overline{R}$	27	O	DATA TRANSMIT/RECEIVE: is needed in a minimum system that desires to use a data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically, DT/$\overline{R}$ is equivalent to $\overline{S_1}$ in maximum mode, and its timing is the same as for M/$\overline{IO}$ (T = HIGH, R = LOW). DT/$\overline{R}$ is held to a high impedance logic one during local bus "hold acknowledge".
$\overline{DEN}$	26	O	DATA ENABLE: provided as an output enable for a bus transceiver in a minimum system which uses the transceiver. $\overline{DEN}$ is active LOW during each memory and I/O access and for $\overline{INTA}$ cycles. For a read or $\overline{INTA}$ cycle it is active from the middle of T_2 until the middle of T_4, while for a write cycle it is active from the beginning of T_2 until the middle of T_4. $\overline{DEN}$ is held to a high impedance logic one during local bus "hold acknowledge".
HOLD HLDA	31, 30	I 0	HOLD: indicates that another master is requesting a local bus "hold". To be acknowledged, HOLD must be active HIGH. The processor receiving the "hold" will issue a "hold acknowledge" (HLDA) in the middle of a T_4 or T_I clock cycle. Simultaneously with the issuance of HLDA, the processor will float the local bus and control lines. After HOLD is detected as being LOW, the processor will lower HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines. HOLD is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the setup time.

Functional Description

Static Operation

All 80C86 circuitry is of static design. Internal registers, counters and latches are static and require no refresh as with dynamic circuit design. This eliminates the minimum operating frequency restriction placed on other microprocessors. The CMOS 80C86 can operate from DC to the specified upper frequency limit. The processor clock may be stopped in either state (HIGH/LOW) and held there indefinitely. This type of operation is especially useful for system debug or power critical applications.

The 80C86 can be single stepped using only the CPU clock. This state can be maintained as long as is necessary. Single step clock operation allows simple interface circuitry to provide critical information for bringing up your system.

Static design also allows very low frequency operation (down to DC). In a power critical situation, this can provide extremely low power operation since 80C86 power dissipation is directly related to operating frequency. As the system frequency is reduced, so is the operating power until, ultimately, at a DC input frequency, the 80C86 power requirement is the standby current, (500μA maximum).

Internal Architecture

The internal functions of the 80C86 processor are partitioned logically into two processing units. The first is the Bus Interface Unit (BIU) and the second is the Execution Unit (EU) as shown in the CPU functional diagram.

These units can interact directly but for the most part perform as separate asynchronous operational processors. The bus interface unit provides the functions related to instruction fetching and queuing, operand fetch and store, and address relocating. This unit also provides the basic bus control. The overlap of instruction pre-fetching provided by this unit serves to increase processor performance through improved bus bandwidth utitization. Up to 6 bytes of the instruction stream can be queued while waiting for decoding and execution.

The instruction stream queuing mechanism allows the BIU to keep the memory utilized very efficiently. Whenever there is space for at least 2 bytes in the queue, the BIU will attempt a word fetch memory cycle. This greatly reduces "dead-time" on the memory bus. The queue acts as a First-In-First-Out (FIFO) buffer, from which the EU extracts instruction bytes as required. If the queue is empty (following a branch instruction, for example), the first byte into the queue immediately becomes available to the EU.

The execution unit receives pre-fetched instructions from the BIU queue and provides un-relocated operand addresses to the BIU. Memory operands are passed through the BIU for processing by the EU, which passes results to the BIU for storage.

Memory Organization

The processor provides a 20-bit address to memory, which locates the byte being referenced. The memory is organized as a linear array of up to 1 million bytes, addressed as 00000(H) to FFFFF(H). The memory is logically divided into code, data, extra and stack segments of up to 64K bytes each, with each segment falling on 16-byte boundaries. (See Figure 1).

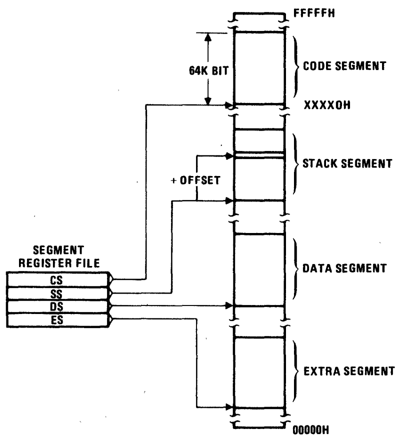


FIGURE 1. 80C86 MEMORY ORGANIZATION

TABLE 4.

TYPE OF MEMORY REFERENCE	DEFAULT SEGMENT BASE	ALTERNATE SEGMENT BASE	OFFSET
Instruction Fetch	CS	None	IP
Stack Operation	SS	None	SP
Variable (except following)	DS	CS, ES, SS	Effective Address
String Source	DS	CS, ES, SS	SI
String Destination	ES	None	DI
BP Used As Base Register	SS	CS, DS, ES	Effective Address

All memory references are made relative to base addresses contained in high speed segment registers. The segment types were chosen based on the addressing needs of programs. The segment register to be selected is automatically chosen according to the specific rules of Table 4. All information in one segment type share the same logical attributes (e.g. code or data). By structuring memory into relocatable areas of similar characteristics and by automatically selecting segment registers, programs are shorter, faster and more structured. (See Table 4).

Word (16-bit) operands can be located on even or odd address boundaries and are thus not constrained to even boundaries as is the case in many 16-bit computers. For address and data operands, the least significant byte of the word is stored in the lower valued address location and the most significant byte in the next higher address location. The BIU automatically performs the proper number of memory accesses, one if the word operand is on an even byte boundary and two if it is on an odd byte boundary. Except for the performance penalty, this double access is transparent to the software. The performance penalty does not occur for instruction fetches; only word operands.

Physically, the memory is organized as a high bank (D15-D8) and a low bank (D7-D0) of 512K bytes addressed in parallel by the processor's address lines.

Byte data with even addresses is transferred on the D7-D0 bus lines while odd addressed byte data (A0 HIGH) is transferred on the D15-D8 bus lines. The processor provides two enable signals, BHE and A0, to selectively allow reading from or writing into either an odd byte location, even byte location, or both. The instruction stream is fetched from memory as words and is addressed internally by the processor at the byte level as necessary.

In referencing word data, the BIU requires one or two memory cycles depending on whether the starting byte of the word is on an even or odd address, respectively. Consequently, in referencing word operands performance can be optimized by locating data on even address boundaries. This is an especially useful technique for using the stack, since odd address references to the stack may adversely affect the context switching time for interrupt processing or task multiplexing.

Certain locations in memory are reserved for specific CPU operations (See Figure 2). Locations from address FFFF0H through FFFFFH are reserved for operations including a jump to the initial program loading routine. Following RESET, the CPU will always begin execution at location FFFF0H where the jump must be located. Locations 00000H through 003FFH are reserved for interrupt operations. Each of the 256 possible interrupt service routines is accessed thru its own pair of 16-bit pointers - segment address pointer and offset address pointer. The first pointer, used as the offset address, is loaded into the IP and the second pointer, which designates the base address is loaded into the CS. At this point program control is transferred to the interrupt routine. The pointer elements are assumed to have been stored at the respective places in reserved memory prior to occurrence of interrupts.

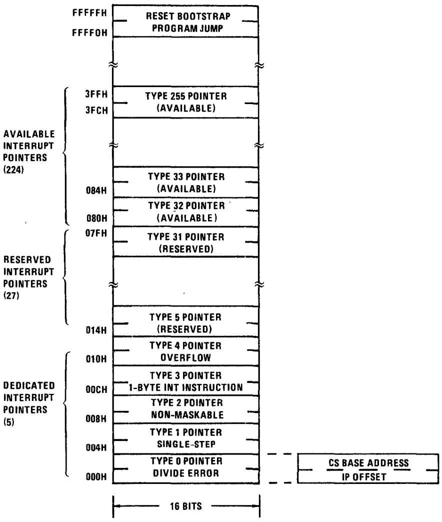


FIGURE 2. RESERVED MEMORY LOCATIONS

Minimum and Maximum Operation Modes

The requirements for supporting minimum and maximum 80C86 systems are sufficiently different that they cannot be met efficiently using 40 uniquely defined pins. Consequently, the 80C86 is equipped with a strap pin (MN/$\overline{MX}$) which defines the system configuration. The definition of a certain subset of the pins changes, dependent on the condition of the strap pin. When the MN/$\overline{MX}$ pin is strapped to GND, the 80C86 defines pins 24 through 31 and 34 in maximum mode. When the MN/$\overline{MX}$ pin is strapped to VCC, the 80C86 generates bus control signals itself on pins 24 through 31 and 34.

The minimum mode 80C86 can be used with either a multiplexed or demultiplexed bus. This architecture provides the 80C86 processing power in a highly integrated form.

The demultiplexed mode requires two 82C82 latches (for 64K addressability) or three 82C82 latches (for a full megabyte of addressing). An 82C86 or 82C87 transceiver can also be used if data bus buffering is required. (See Figure 6a.) The 80C86 provides $\overline{DEN}$ and DT/$\overline{R}$ to control the transceiver, and ALE to latch the addresses. This configuration of the minimum mode provides the standard demultiplexed bus structure with heavy bus buffering and relaxed bus timing requirements.

The maximum mode employs the 82C88 bus controller (See Figure 6b). The 82C88 decodes status lines $\overline{S_0}$, $\overline{S_1}$ and $\overline{S_2}$, and provides the system with all bus control signals.

Moving the bus control to the 82C88 provides better source and sink current capability to the control lines, and frees the 80C86 pins for extended large system features. Hardware lock, queue status, and two request/grant interfaces are provided by the 80C86 in maximum mode. These features allow coprocessors in local bus and remote bus configurations.

Bus Operation

The 80C86 has a combined address and data bus commonly referred to as a time multiplexed bus. This technique provides the most efficient use of pins on the processor while permitting the use of a standard 40-lead package. This "local bus" can be buffered directly and used throughout the system with address latching provided on memory and I/O modules. In addition, the bus can also be demultiplexed at the processor with a single set of 82C82 address latches if a standard non-multiplexed bus is desired for the system.

Each processor bus cycle consists of at least four CLK cycles. These are referred to as T_1, T_2, T_3 and T_4 (see Figure 3). The address is emitted from the processor during T_1 and data transfer occurs on the bus during T_3 and T_4. T_2 is used primarily for changing the direction of the bus during read operations. In the event that a "NOT READY" indication is given by the addressed device, "Wait" states (TW) are inserted between T_3 and T_4. Each inserted wait state is the same duration as a CLK cycle. Periods can occur between 80C86 driven bus cycles. These are referred to as "idle" states (T_I) or inactive CLK cycles. The processor uses these cycles for internal housekeeping and processing.

During T_1 of any bus cycle, the ALE (Address Latch Enable) signal is emitted (by either the processor or the 82C88 bus controller, depending on the MN/$\overline{MX}$ strap). At the trailing edge of this pulse, a valid address and certain status information for the cycle may be latched.

Status bits $\overline{S_0}$, $\overline{S_1}$ and $\overline{S_2}$ are used by the bus controller, in maximum mode, to identify the type of bus transaction according to Table 5.

TABLE 5.

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	CHARACTERISTICS
0	0	0	Interrupt
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (no bus cycle)

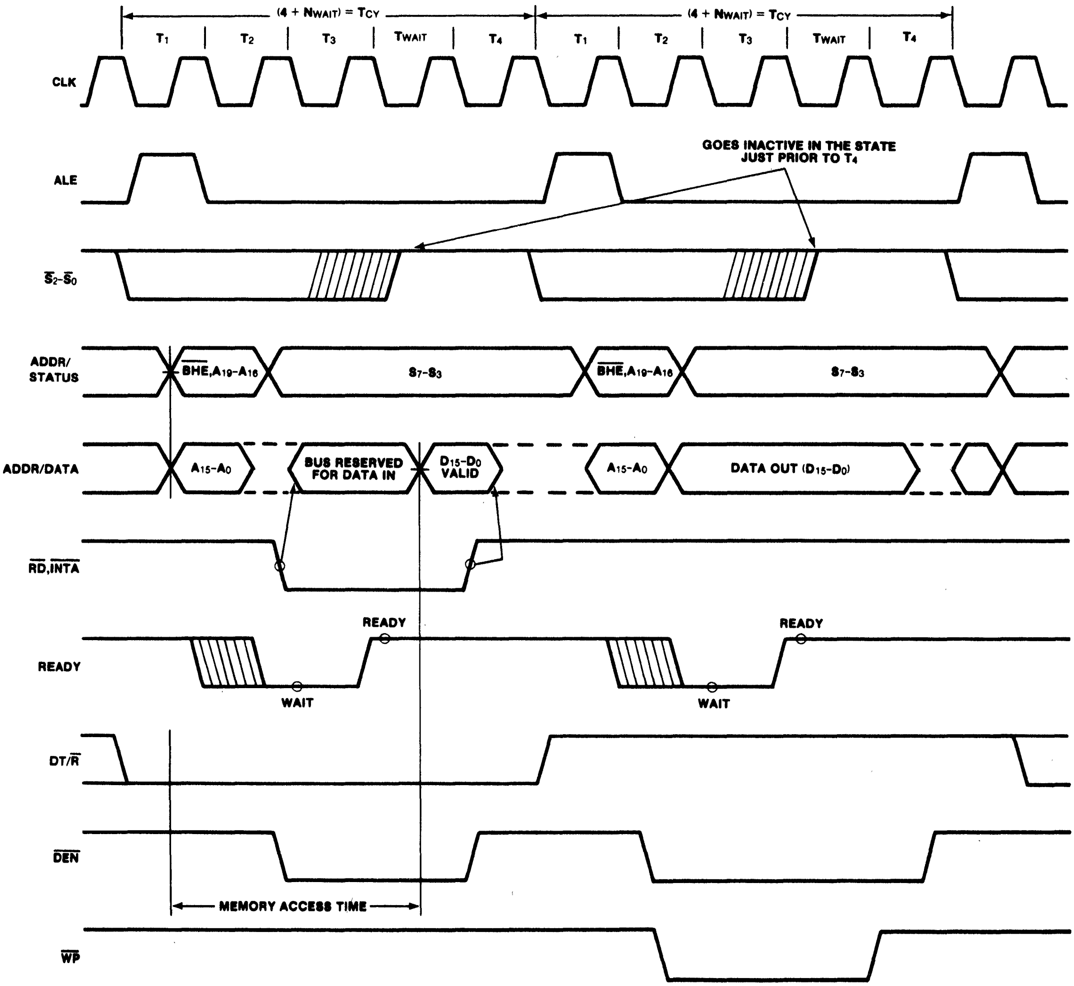


FIGURE 3. BASIC SYSTEM TIMING

Status bits S_3 through S_7 are time multiplexed with high order address bits and the $\overline{BHE}$ signal, and are therefore valid during T_2 through T_4. S_3 and S_4 indicate which segment register (see Instruction Set Description) was used for this bus cycle in forming the address, according to Table 6.

TABLE 6.

S_4	S_3	CHARACTERISTICS
0	0	Alternate Data (extra segment)
0	1	Stack
1	0	Code or None
1	1	Data

S_5 is a reflection of the PSW interrupt enable bit. S_6 is always zero and S_7 is a spare status bit.

I/O Addressing

In the 80C86, I/O operations can address up to a maximum of 64K I/O byte registers or 32K I/O word registers. The I/O address appears in the same format as the memory address on bus lines A15-A0. The address lines A19-A16 are zero in I/O operations. The variable I/O instructions which use register DX as a pointer have full address capability while the direct I/O instructions directly address one or two of the 256 I/O byte locations in page 0 of the I/O address space.

I/O ports are addressed in the same manner as memory locations. Even addressed bytes are transferred on the D7-D0 bus lines and odd addressed bytes on D15-D8. Care must be taken to ensure that each register within an 8-bit peripheral located on the lower portion of the bus be addressed as even.

External Interface

Processor RESET and Initialization

Processor initialization or start up is accomplished with activation (HIGH) of the RESET pin. The 80C86 RESET is required to be HIGH for greater than 4 CLK cycles. The 80C86 will terminate operations on the high-going edge of RESET and will remain dormant as long as RESET is HIGH. The low-going transition of RESET triggers an internal reset sequence for approximately 7 clock cycles. After this interval, the 80C86 operates normally beginning with the instruction in absolute location FFFF0H. (See Figure 2). The RESET input is internally synchronized to the processor clock. At initialization, the HIGH-to-LOW transition of RESET must occur no sooner than 50μs (or 4 CLK cycles, whichever is greater) after power-up, to allow complete initialization of the 80C86.

NMI will not be recognized prior to the second CLK cycle following the end of RESET. If NMI is asserted sooner than nine clock cycles after tthe end of RESET, the processor may execute one instruction before responding to the interrupt.

Bus Hold Circuitry

To avoid high current conditions caused by floating inputs to CMOS devices and to eliminate need for pull-up/down resistors, "bus-hold" circuitry has been used on the 80C86 pins 2-16, 26-32 and 34-39. (See Figure 4A and 4B). These circuits will maintain the last valid logic state if no driving source is present (i.e. an unconnected pin or a driving source which goes to a high impedance state). To overdrive the "bus hold" circuits, an external driver must be capable of supplying approximately 400μA minimum sink or source current at valid input voltage levels. Since this "bus hold" circuitry is active and not a "resistive" type element, the associated power supply current is negligible and power dissipation is significantly reduced when compared to the use of passive pull-up resistors.

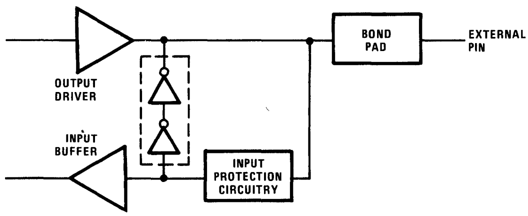


FIGURE 4A. BUS HOLD CIRCUITRY PIN 2-16, 34-39

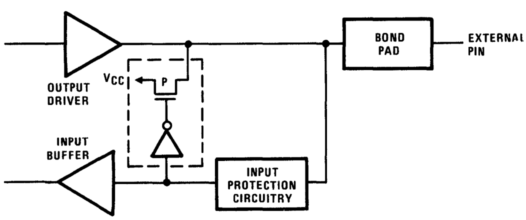


FIGURE 4B. BUS HOLD CIRCUITRY PIN 26-32

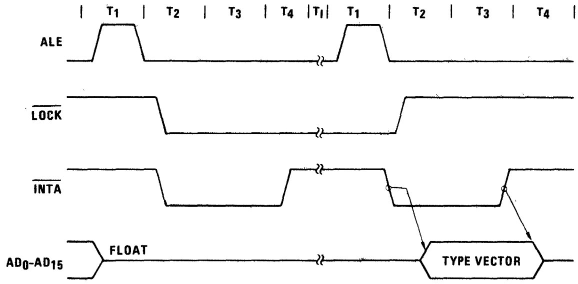


FIGURE 5. INTERRUPT ACKNOWLEDGE SEQUENCE

Interrupt Operations

Interrupt operations fall into two classes: software or hardware initiated. The software initiated interrupts and software aspects of hardware interrupts are specified in the Instruction Set Description. Hardware interrupts can be classified as non-maskable or maskable.

Interrupts result in a transfer of control to a new program location. A 256-element table containing address pointers to the interrupt service program locations resides in absolute locations 0 through 3FFH, which are reserved for this purpose. Each element in the table is 4 bytes in size and corresponds to an interrupt "type". An interrupting device supplies an 8-bit type number during the interrupt acknowledge sequence, which is used to "vector" through the appropriate element to the new interrupt service program location. All flags and both the Code Segment and Instruction Pointer register are saved as part of the $\overline{INTA}$ sequence. These are restored upon execution of an Interrupt Return (IRET) instruction.

Non-Maskable Interrupt (NMI)

The processor provides a single non-maskable interrupt pin (NMI) which has higher priority than the maskable interrupt request pin (INTR). A typical use would be to activate a power failure routine. The NMI is edge-triggered on a LOW-to-HIGH transition. The activation of this pin causes a type 2 interrupt.

NMI is required to have a duration in the HIGH state of greater than two CLK cycles, but is not required to be synchronized to the clock. Any positive transition of NMI is latched on-chip and will be serviced at the end of the current instruction or between whole moves of a block-type instruction. Worst case response to NMI would be for multiply, divide, and variable shift instructions. There is no specification on the occurrence of the low-going edge; it may occur before, during or after the servicing of NMI. Another positive edge triggers another response if it occurs after the start of the NMI procedure. The signal must be free of logical spikes in general and be free of bounces on the low-going edge to avoid triggering extraneous responses.

Maskable Interrupt (INTR)

The 80C86 provides a single interrupt request input (INTR) which can be masked internally by software with the resetting of the interrupt enable flag (IF) status bit. The interrupt request signal is level triggered. It is internally synchronized during each clock cycle on the high-going edge of CLK. To be responded to, INTR must be present (HIGH) during the clock period preceding the end of the current instruction or the end of a whole move for a block- type instruction. INTR may be removed anytime after the falling edge of the first $\overline{INTA}$ signal. During the interrupt response sequence further interrupts are disabled. The enable bit is reset as part of the response to any interrupt (INTR, NMI, software interrupt or single-step), although the FLAGS register which is automatically pushed onto the stack reflects the state of the processor prior to the interrupt. Until the old FLAGS register is restored the enable bit will be zero unless specifically set by an instruction.

During the response sequence (Figure 5) the processor executes two successive (back-to-back) interrupt acknowledge cycles. The 80C86 emits the LOCK signal (Max mode only) from T_2 of the first bus cycle until T_2 of the second. A local bus "hold" request will not be honored until the end of the second bus cycle. In the second bus cycle, a byte is supplied to the 80C86 by the 82C59A Interupt Controller, which identifies the source (type) of the interrupt. This byte is multiplied by four and used as a pointer into the interrupt vector look-up table. An INTR signal left HIGH will be continually responded to within the limitations of the enable bit and sample period. The INTERRUPT RETURN instruction includes a FLAGS pop which returns the status of the original interrupt enable bit when is restores the FLAGS.

Halt

When a software "HALT" instruction is executed the processor indicates that it is entering the "HALT" state in one of two ways depending upon which mode is strapped. In minimum mode, the processor issues one ALE with no qualifying bus control signals. In maximum mode the processor issues appropriate HALT status on $\overline{S_2}$, $\overline{S_1}$, $\overline{S_0}$ and the 82C88 bus controller issues one ALE. The 80C86 will not leave the "HALT" state when a local bus "hold" is entered while in "HALT". In this case, the processor reissues the HALT indicator at the end of the local bus hold. An NMI or interrupt request (when interrupts enabled) or RESET will force the 80C86 out of the "HALT" state.

Read/Modify/Write (Semaphore)

Operations Via Lock

The $\overline{LOCK}$ status information is provided by the processor when consecutive bus cycles are required during the execution of an instruction. This gives the processor the capability of performing read/modify/write operations on memory (via the Exchange Register With Memory instruction, for example) without another system bus master receiving intervening memory cycles. This is useful in multiprocessor system configurations to accomplish "test and set lock" operations. the LOCK signal is activated (forced LOW) in the clock cycle following decoding of the software "LOCK" prefix instruction. It is deactivated at the end of the last bus cycle of the instruction following the "LOCK" prefix instruction. While LOCK is active a request on a RQ/GT pin will be recorded and then honored at the end of the LOCK.

External Synchronization Via TEST

As an alternative to interrupts, the 80C86 provides a single software-testable input pin (TEST). This input is utilized by executing a WAIT instruction. The single WAIT instruction is repeatedly executed until the TEST input goes active (LOW). The execution of WAIT does not consume bus cycles once the queue is full.

If a local bus request occurs during WAIT execution, the 80C86 tri-states all output drivers while inputs and I/O pins are held at valid logic levels by internal bus-hold circuits. If interrupts are enabled, the 80C86 will recognize interrupts and process them when it regains control of the bus. The WAIT instruction is then refetched, and reexecuted.

Basic System Timing

Typical system configurations for the processor operating in minimum mode and in maximum mode are shown in Figures 6A and 6B, respectively. In minimum mode, the MN/MX pin is strapped to V_{CC} and the processor emits bus control signals (e.g. RD, WR, etc.) directly. In maximum mode, the MN/MX pin is strapped to GND and the processor emits coded status information which the 82C88 bus controller used to generate MULTIBUS™ compatible bus control signals. Figure 3 shows the signal timing relationships.

TABLE 7. 80C86 REGISTER MODEL

AX	AH	AL	ACCUMULATOR
BX	BH	BL	BASE
CX	CH	CL	COUNT
DX	DH	DL	DATA
	SP		STACK POINTER
	BP		BASE POINTER
	SI		SOURCE INDEX
	DI		DESTINATION INDEX
	IP		INSTRUCTION POINTER
	$FLAGS_H$	$FLAGS_L$	STATUS FLAGS
	CS		CODE SEGMENT
	DS		DATA SEGMENT
	SS		STACK SEGMENT
	ES		EXTRA SEGMENT

System Timing - Minimum System

The read cycle begins in T1 with the assertion of the Address Latch Enable (ALE) signal. The trailing (low-going) edge of this signal is used to latch the address information, which is valid on the address/data bus (AD0-AD15) at this time, into the 82C82/82C83 latch. The BHE and A0 signals address the low, high or both bytes. From T1 to T4 the M/IO signal indicates a memory or I/O operation. At T2, the address is removed from the address/data bus and the bus is held at the last valid logic state by internal bus hold devices. The read control signal is also asserted at T2. The read (RD) signal causes the addressed device to enable its data bus drivers to the local bus. Some time later, valid data will be available on the bus and the addressed device will drive the READY line HIGH. When the processor returns the read signal to a HIGH level, the addressed device will again tri-state its bus drivers. If a transceiver (82C86/82C87) is required to buffer the 80C86 local bus, signals DT/R and DEN are provided by the 80C86.

A write cycle also begins with the assertion of ALE and the emission of the address. The M/IO signal is again asserted to indicate a memory or I/O write operation. In T_2, immediately following the address emission, the processor emits the data to be written into the addressed location. This data remains valid until at least the middle of T_4. During T_2, T_3 and T_W, the processor asserts the write control signal. The write (WR) signal becomes active at the beginning of T_2 as opposed to the read which is delayed somewhat into T_2 to provide time for output drivers to become inactive.

The BHE and A0 signals are used to select the proper byte(s) of the memory/IO word to be read or written according to Table 8.

TABLE 8.

BHE	A_0	CHARACTERISTCS
0	0	Whole word
0	1	Upper byte from/to odd address
1	0	Lower byte from/to even address
1	1	None

I/O ports are addressed in the same manner as memory location. Even addressed bytes are transferred on the D7-D0 bus lines and odd address bytes on D15-D8.

The basic difference between the interrupt acknowledge cycle and a read cycle is that the interrupt acknowledge signal (INTA) is asserted in place of the read (RD) signal and the address bus is held at the last valid logic state by internal bus hold devices. (See Figure 4). In the second of two successive INTA cycles a byte of information is read from the data bus (D7-D0) as supplied by the interrupt system logic (i.e. 82C59A Priority Interrupt Controller). This byte identifies the source (type) of the interrupt. It is multiplied by four and used as a pointer into an interrupt vector lookup table, as described earlier.

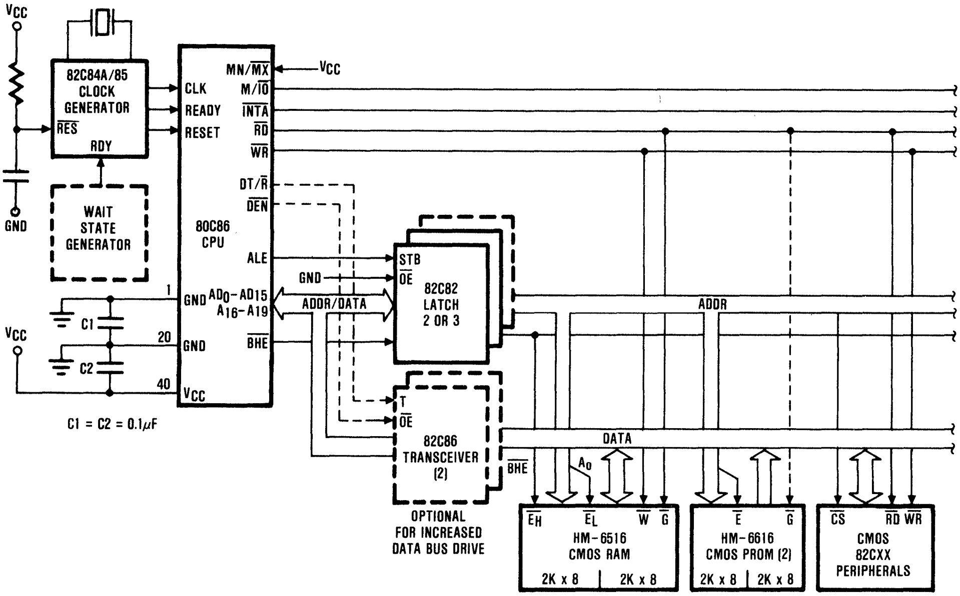


FIGURE 6A. MINIMUM MODE 80C86 TYPICAL CONFIGURATION

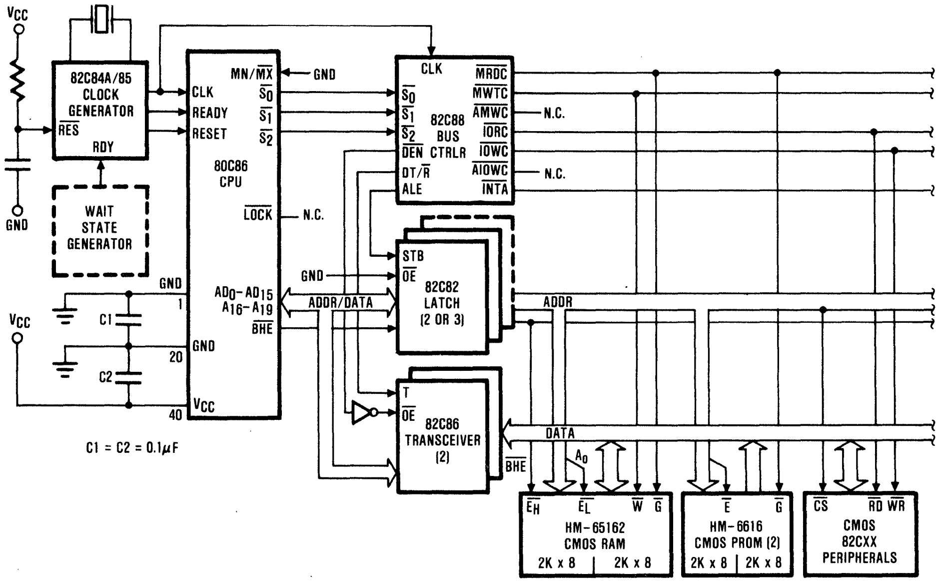


FIGURE 6B. MAXIMUM MODE 80C86 TYPICAL CONFIGURATION

Bus Timing - Medium Size Systems

For medium complexity systems the MN/$\overline{MX}$ pin is connected to GND and the 82C88 Bus Controller is added to the system as well as an 82C82/82C83 latch for latching the system address, and an 82C86/82C87 transceiver to allow for bus loading greater than the 80C86 is capable of handling. Signals ALE, $\overline{DEN}$, and DT/$\overline{R}$ are generated by the 82C88 instead of the processor in this configuration, although their timing remains relatively the same. The 80C86 status outputs ($\overline{S_2}$, $\overline{S_1}$ and $\overline{S_0}$) provide type-of-cycle information and become 82C88 inputs. This bus cycle information specifies read (code, data or I/O), write (data or I/O), interrupt acknowledge, or software halt. The 82C88 issues control signals specifying memory read or write, I/O read or write, or interrupt acknowledge. The 82C88 provides two types of write strobes, normal and advanced, to be applied as required. The normal write strobes have data valid at the leading edge of write. The advanced write strobes have the same timing as read strobes, and hence, data is not valid at the leading edge of write. The 82C86/82C87 transceiver receives the usual T and OE inputs from the 82C88 DT/R and DEN signals.

The pointer into the interrupt vector table, which is passed during the second $\overline{INTA}$ cycle, can be derived from an 82C59A located on either the local bus or the system bus. If the master 82C59A Priority Interrupt Controller is positioned on the local bus, the 82C86/82C87 transceiver must be disabled when reading from the master 82C59A during the interrupt acknowledge sequence and software "poll".

Absolute Maximum Ratings

Supply Voltage .... +8.0 Volts
Input, Output or I/O Voltage Applied .... GND -0.5V to V_{CC} +0.5V
Maximum Package Power Dissipation .... 1 Watt
Storage Temperature Range .... -65°C to +150°C
θ_{jc} .... 16°C/W (CERDIP package), 21°C/W (LCC package)
θ_{ja} .... 36°C/W (CERDIP package), 41°C/W (LCC package)
Gate Count .... 9750 Gates
Junction Temperature .... +150°C
Lead Temperature (Soldering, Ten Seconds) .... +260°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +4.5V to +5.5V
M80C86-2 Only .... +4.75V to +5.25V
Operating Temperature Range
C80C86 .... 0°C to +70°C
I80C86 .... -40°C to +85°C
M80C86 .... -55°C to +125°C

D.C. Electrical Specifications

V_{CC} = 5.0V ± 10%; T_A = 0°C to +70°C (C80C86) (C80C86-2)
V_{CC} = 5.0V ± 10%; T_A = -40°C to +85°C (I80C86) (I80C86-2)
V_{CC} = 5.0V ± 10%; T_A = -55°C to +125°C (M80C86)
V_{CC} = 5.0V ± 5%; TA = -55°C to +125°C (M80C86-2)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIN	Logical One Input Voltage	2.0 2.2		V V	C80C86, I80C86 M80C86
VIL	Logical Zero Input Voltage		0.8	V	
VIHC	CLK Logical One Input Voltage	V_{CC} -0.8		V	
VILC	CLK Logical Zero Input Voltage		0.8	V	
VOH	Output High Voltage	3.0 V_{CC} -0.4		V V	IOH = -2.5mA IOH = -100μA
VOL	Output Low Voltage		0.4	V	IOL = +2.5mA
II	Input Leakage Current	-1.0	1.0	μA	VIN = GND or VCC DIP Pins 17-19, 21-23, 33
IBHH	Input Current-Bus Hold High	-40	-400	μA	VIN = 3.0V (See Note 1)
IBHL	Input Current-Bus Hold Low	40	400	μA	VIN = 0.8V (See Note 2)
IO	Output Leakage Current	-10.0	10.0	μA	VOUT = GND or VCC DIP Pins 24, 25
ICCSB	Standby Power Supply Current		500	μA	V_{CC} = 5.5V (See Note 3)
ICCOP	Operating Power Supply Current		10	mA/MHz	T_A = 25°C V_{CC} = 5V, TYP, FREQ = CLK Cycle Time (TCLCL) (MHz)

Capacitance

T_A = 25°C; V_{CC} = GND = 0V; VIN = +5V or GND.

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
CIN	Input Capacitance	20	pF	FREQ = 1MHz. Unmeasured pins returned to GND
COUT	Output Capacitance	20	pF	T_A = 25°C
CI/O	I/O Capacitance	20	pF	VIN or VOUT = V_{CC} or GND

NOTES:
1. IBHH should be measured after raising VIN to V_{CC} and then lowering to 3.0V on the following pins: 2-16, 26-32, 34-39.
2. IBHL should be measured after lowering VIN to GND and then raising to 0.8V on the following pins: 2-16, 34-39.
3. ICCSB tested during clock high time after halt instruction executed. VIN = V_{CC} or GND, V_{CC} = 5.5V, Outputs unloaded.

A.C. Electrical Specifications

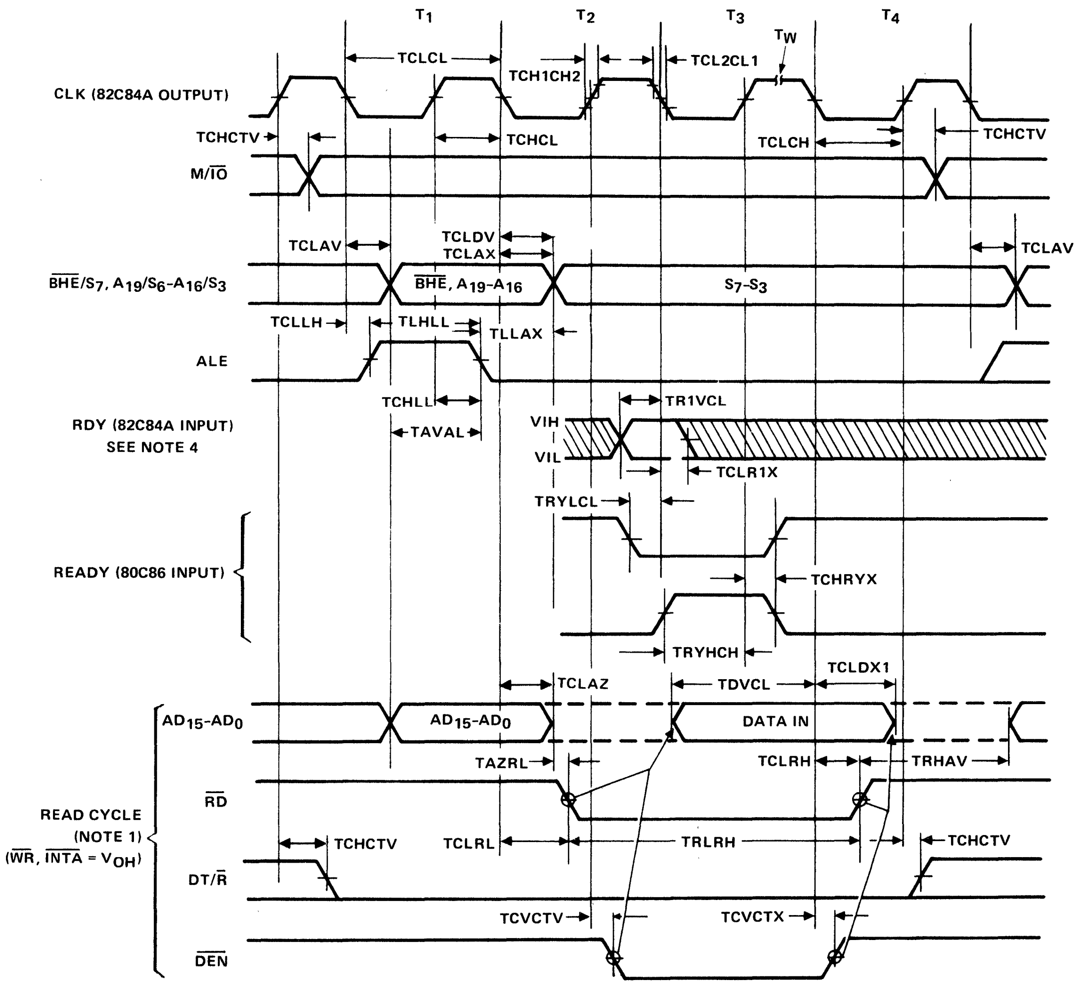
V_{CC} = 5.0V ± 10%; T_A = 0°C to +70°C (C80C86) (C80C86-2)
V_{CC} = 5.0V ± 10%; T_A = -40°C to +85°C (I80C86) (I80C86-2)
V_{CC} = 5.0V ± 10%; T_A = -55°C to +125°C (M80C86)
V_{CC} = 5.0V ± 5%; T_A = -55°C to +125°C (M80C86-2)

MINIMUM COMPLEXITY SYSTEM

SYMBOL	PARAMETER	80C86-2 MIN	80C86-2 MAX	80C86 MIN	80C86 MAX	UNITS	TEST CONDITIONS
TIMING REQUIREMENTS							
TCLCL	CLK Cycle Period	125		200		ns	
TCLCH	CLK Low Time	68		118		ns	
TCHCL	CLK High Time	44		69		ns	
TCH1CH2	CLK Rise Time		10		10	ns	From 1.0V to 3.5V
TCL2CL1	CLK Fall Time		10		10	ns	From 3.5V to 1.0V
TDVCL	Data In Setup Time	20		30		ns	
TCLDX1	Data In Hold Time	10		10		ns	
TR1VCL	RDY Setup Time into 82C84A (Notes 1, 2)	35		35		ns	
TCLR1X	RDY Hold Time into 82C84A (Notes 1, 2)	0		0		ns	
TRYHCH	READY Setup Time into 80C86	68		118		ns	
TCHRYX	READY Hold Time into 80C86	20		30		ns	
TRYLCL	READY Inactive to CLK (Note 3)	-8		-8		ns	
THVCH	HOLD Setup Time	20		35		ns	
TINVCH	INTR, NMI, $\overline{\text{TEST}}$ Setup Time (Note 2)	15		30		ns	
TILIH	Input Rise Time (Except CLK)		15		15	ns	From 0.8V to 2.0V
TIHIL	Input Fall Time (Except CLK)		15		15	ns	From 2.0V to 0.8V
TIMING RESPONSES							
TCLAV	Address Valid Delay	10	60	10	110	ns	CL = 100pF
TCLAX	Address Hold Time	10		10		ns	↓
TCLAZ	Address Float Delay	TCLAX	50	TCLAX	80	ns	↓
TCHSZ	Status Float Delay		50		80	ns	↓
TCHSV	Status Active Delay	10	60	10	110	ns	↓
TLHLL	ALE Width	TCLCH-10		TCLCH-20		ns	↓
TCLLH	ALE Active Delay		50		80	ns	↓
TCHLL	ALE Inactive Delay		55		85	ns	↓
TLLAX	Address Hold Time to ALE Inactive	TCHCL-10		TCHCL-10		ns	↓
TCLDV	Data Valid Delay	10	60	10	110	ns	↓
TCLDX2	Data Hold Time	10		10		ns	↓
TWHDX	Data Hold Time After WR	TCLCL-30		TCLCL-30		ns	↓
TCVCTV	Control Active Delay1	10	70	10	110	ns	↓
TCHCTV	Control Active Delay2	10	60	10	110	ns	↓
TCVCTX	Control Inactive Delay	10	70	10	110	ns	↓
TAZRL	Address Float to READ Active	0		0		ns	↓
TCLRL	RD Active Delay	10	100	10	165	ns	↓
TCLRH	RD Inactive Delay	10	80	10	150	ns	↓
TRHAV	RD Inactive to Next Address Active	TCLCL-40		TCLCL-45		ns	↓
TCLHAV	HLDA Valid Delay	10	100	10	160	ns	↓
TRLRH	RD Width	2TCLCL-50		2TCLCL-75		ns	↓
TWLWH	WR Width	2TCLCL-40		2TCLCL-60		ns	↓
TAVAL	Address Valid to ALE Low	TCLCH-40		TCLCH-60		ns	↓
TOLOH	Output Rise Time		15		20	ns	From 0.8V to 2.0V
TOHOL	Output Fall Time		15		20	ns	From 2.0V to 0.8V

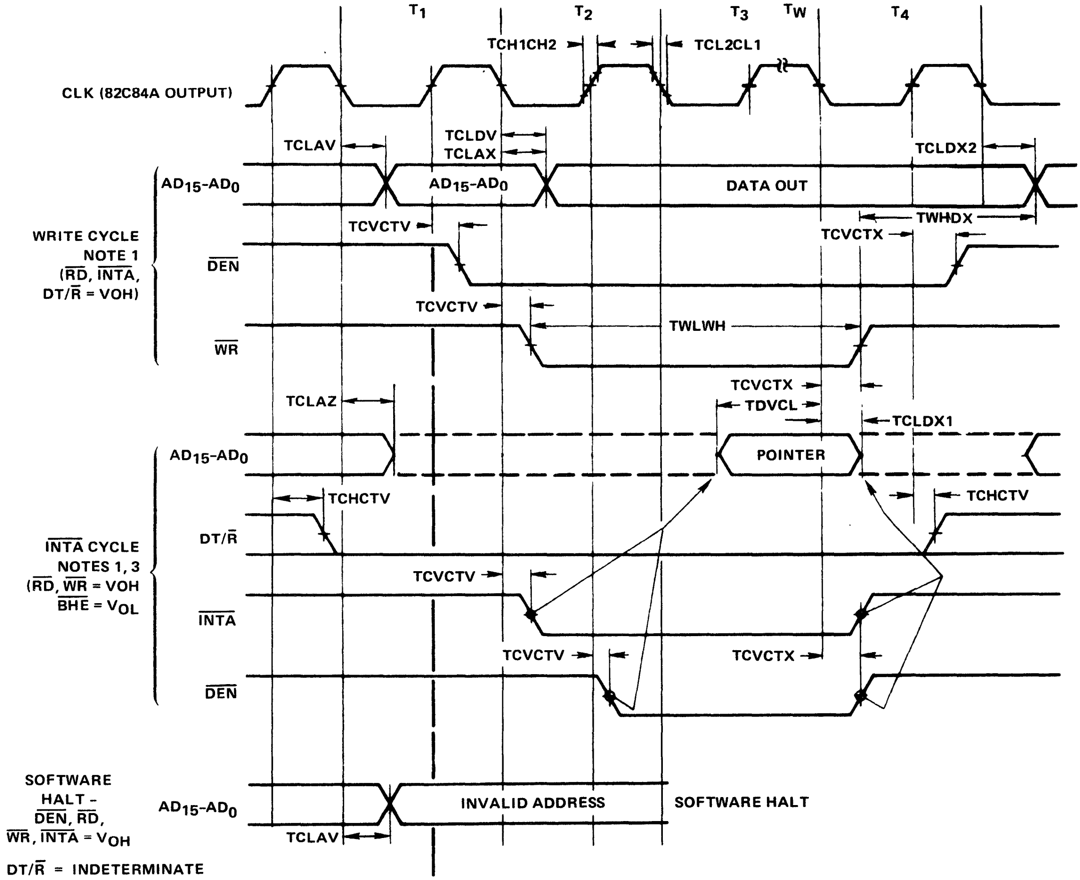
NOTES: 1. Signal at 82C84A shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T_2 state (8ns into T_3).

Waveforms



BUS TIMING - MINIMUM MODE SYSTEM

Waveforms



NOTES:
1. All signals switch between VOH and VOL unless otherwise specified.
2. RDY is sampled near the end of T_2, T_3, TW to determine if TW machines states are to be inserted.
3. Two INTA cycles run back-to-back. The 80C86 local ADDR/DATA bus is floating during both INTA cycles. Control signals are shown for the second INTA cycle.
4. Signals at 82C84A are shown for reference only.
5. All timing measurements are made at 1.5V unless otherwise noted.

BUS TIMING - MINIMUM MODE SYSTEM (Continued)

A.C. Electrical Specifications

V_{CC} = 5.0V ± 10%; T_A = 0°C to +70°C (C80C86) (C80C86-2)
V_{CC} = 5.0V ± 10%; T_A = -40°C to +85°C (I80C86) (I80C86-2)
V_{CC} = 5.0V ± 10%; T_A = -55°C to +125°C (M80C86)
V_{CC} = 5.0V ± 5%; T_A = -55°C to +125°C (M80C86-2)

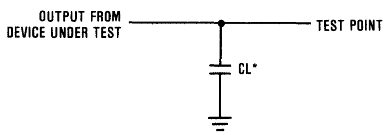
MAX MODE SYSTEM (USING 82C88 BUS CONTROLLER)

TIMING REQUIREMENTS		80C86-2		80C86			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS	TEST CONDITIONS
TCLCL	CLK Cycle Period	125		200		ns	
TCLCH	CLK Low Time	68		118		ns	
TCHCL	CLK High Time	44		69		ns	
TCH1CH2	CLK Rise Time		10		10	ns	From 1.0V to 3.5V
TCL2CL1	CLK Fall Time		10		10	ns	From 3.5V to 1.0V
TDVCL	Data in Setup Time	20		30		ns	
TCLDX1	Data In Hold Time	10		10		ns	
TR1VCL	RDY Setup Time into 82C84A (Notes 1, 2)	35		35		ns	
TCLR1X	RDY Hold Time into 82C84A (Notes 1, 2)	0		0		ns	
TRYHCH	READY Setup Time into 80C86	68		118		ns	
TCHRYX	READY Hold Time into 80C86	20		30		ns	
TRYLCL	READY Inactive to CLK (Note 3)	-8		-8		ns	
TINVCH	Setup Time for Recognition (INTR, NMI, $\overline{TEST}$)(Note 2)	15		30		ns	
TGVCH	$\overline{RQ}/\overline{GT}$ Setup Time	15		30		ns	
TCHGX	$\overline{RQ}$ Hold Time into 80C86 (Note 4)	30	TCHCL + 10	40	TCHCL + 10	ns	
TILIH	Input Rise Time (Except CLK)		15		15	ns	From 0.8V to 2.0V
TIHIL	Input Fall Time (Except CLK)		15		15	ns	From 2.0V to 0.8V
TIMING RESPONSES							
TCLML	Command Active Delay (Note 1)	5	35	5	35	ns	↑
TCLMH	Command Inactive	5	35	5	35	ns	
TRYHSH	READY Active to Status Passive (Notes 3, 5)		65		110	ns	
TCHSV	Status Active Delay	10	60	10	110	ns	
TCLSH	Status Inactive Delay (Note 5)	10	70	10	130	ns	
TCLAV	Address Valid Delay	10	60	10	110	ns	
TCLAX	Address Hold Time	10		10		ns	
TCLAZ	Address Float Delay	TCLAX	50	TCLAX	80	ns	
TCHSZ	Status Float Delay		50		80	ns	
TSVLH	Status Valid to ALE High (Note 1)		20		20	ns	
TSVMCH	Status Valid to MCE High (Note 1)		30		30	ns	CL = 100pF for all 80C86 Outputs (In addition to 80C86 self-load)
TCLLH	CLK low to ALE Valid		20		20	ns	
TCLMCH	CLK low to MCE High (Note 1)		25		25	ns	
TCHLL	ALE Inactive Delay (Note 1)	4	18	4	18	ns	
TCLMCL	MCE Inactive Delay (Note 1)		15		15	ns	
TCLDV	Data Valid Delay	10	60	10	110	ns	
TCLDX2	Data Hold Time	10		10		ns	
TCVNV	Control Active Delay (Note 1)	5	45	5	45	ns	↓

TIMING REQUIREMENTS		80C86-2		80C86			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS	TEST CONDITIONS
TIMING RESPONSES							
TCVNX	Control Inactive Delay (Note 1)	5	45	10	45	ns	↑
TAZRL	Address Float to Read Active	0		0		ns	
TCLRL	RD Active Delay	10	100	10	165	ns	CL = 100pF
TCLRH	RD Inactive Delay	10	80	10	150	ns	
TRHAV	RD Inactive to Next Address Active	TCLCL-45		TCLCL-45		ns	
TCHDTL	Direction Control Active Delay (Note 1)		50		50	ns	
TCHDTH	Direction Control Inactive Delay (Note 1)		30		30	ns	
TCLGL	GT Active Delay	10	50	10	85	ns	
TCLGH	GT Inactive Delay	10	50	10	85	ns	
TRLRH	RD Width	2TCLCL-50		2TCLCL-75		ns	↓
TOLOH	Output Rise Time		15		20	ns	From 0.8V to 2.0V
TOHOL	Output Fall Time		15		20	ns	From 2.0V to 0.8V

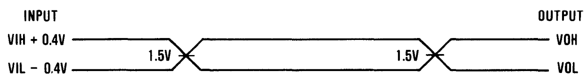
Notes:
1. Signal at 82C84A or 82C88 shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T2 state (8 nanoseconds into T3).
4. The 80C86 actively pulls the $\overline{RQ}/\overline{GT}$ pin to a logic one on the following clock low time.
5. Status lines return to their inactive (logic one) state after CLK goes low and READY goes high.

A. C. Test Circuits



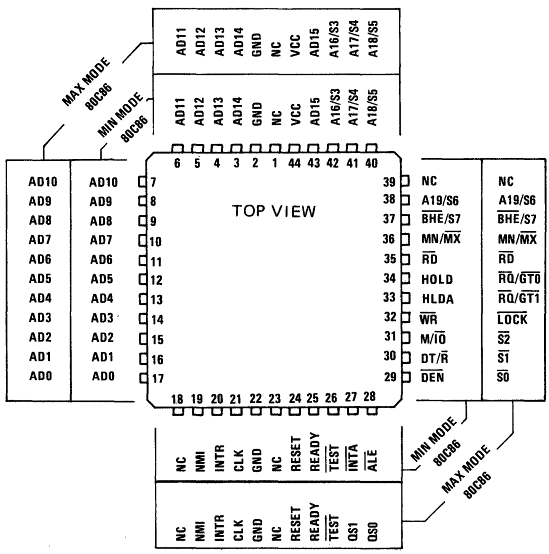
*Includes stray and jig capacitance

A. C. Testing Input, Output Waveform

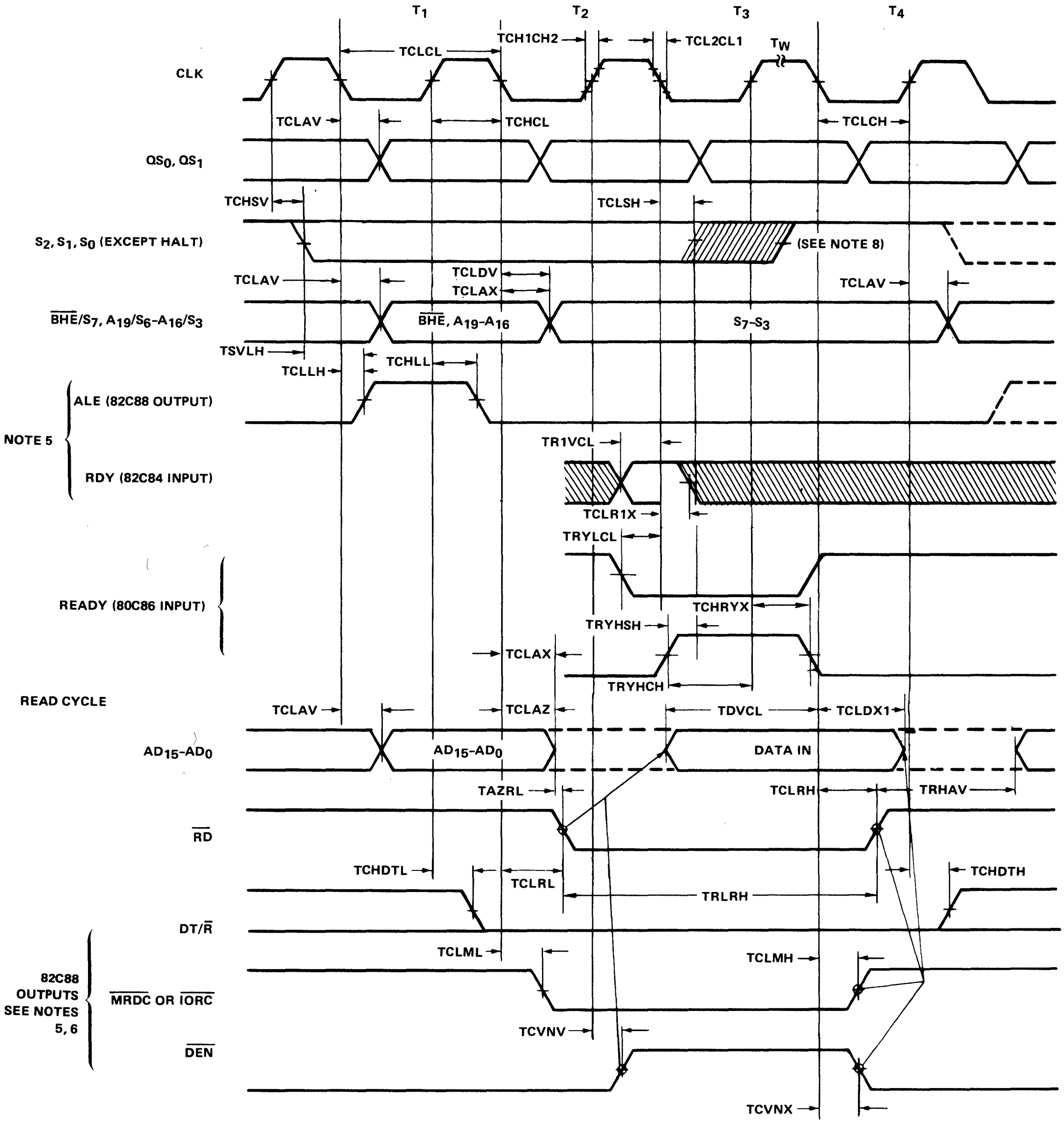


A. C. Testing: All input signals (other than CLK) must switch between VIL_{max} -0.4 and VIH_{min} +0.4V. CLK must switch between 0.4V and VCC -0.4V. Input Rise, and fall times are driven at 1ns/V

LCC/PLCC Pinout

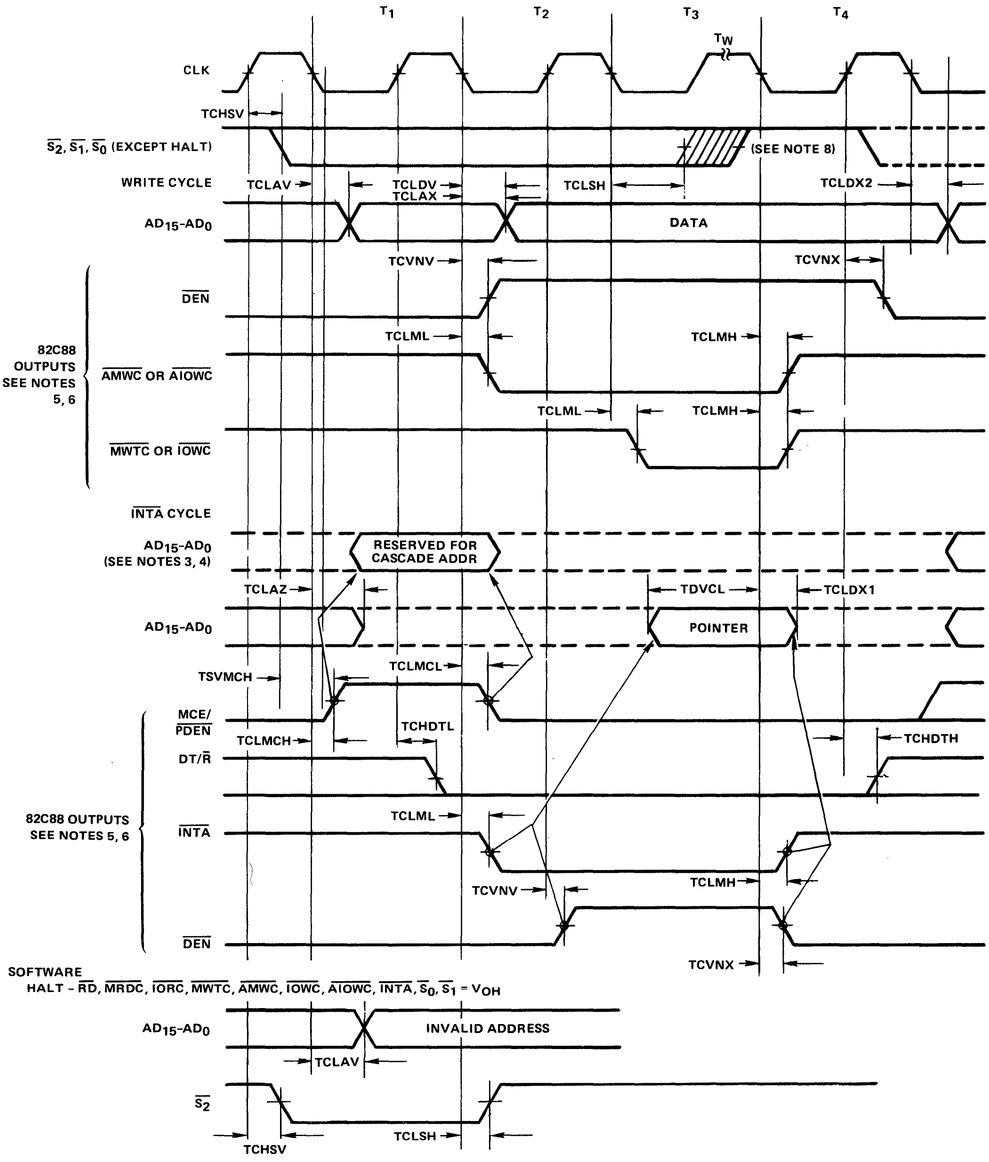


Waveforms



BUS TIMING - MAXIMUM MODE SYSTEM

Waveforms



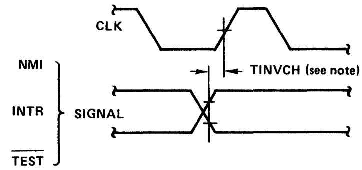
BUS TIMING-MAXIMUM MODE SYSTEM (USING 82C88)

NOTES:

1. All signals switch between V_{OH} and V_{OL} unless otherwise specified.
2. RDY is sampled near the end of T_2, T_3, T_W to determine if T_W machines states are to be inserted.
3. Cascade address is valid between first and second $\overline{INTA}$ cycle.
4. Two $\overline{INTA}$ cycles run back-to-back. The 80C86 LOCAL ADDR/DATA BUS is floating during both INTA cycles. Control for pointer address is shown for second $\overline{INTA}$ cycle.
5. Signals at 82C84A or 82C88 are shown for reference only.
6. The issuance of the 82C88 command and control signals ($\overline{MRDC}$, $\overline{MWTC}$, $\overline{AMWC}$, $\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{INTA}$ and $\overline{DEN}$) lags the active high 82C88 CEN.
7. All timing measurements are made at 1.5V unless otherwise noted.
8. Status inactive in state just prior to T_4.

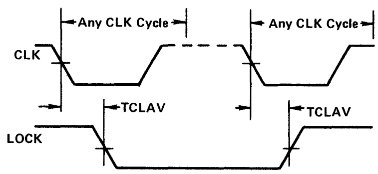
Waveforms

ASYNCHRONOUS SIGNAL RECOGNITION

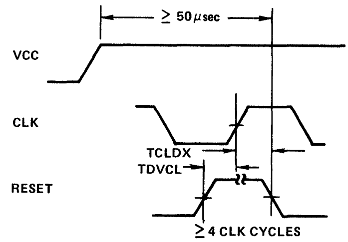


Note: Setup Requirements for asynchronous signals only to guarantee recognition at next CLK.

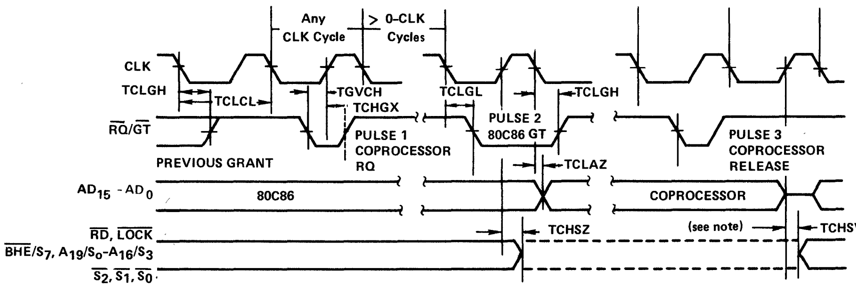
BUS LOCK SIGNAL TIMING (MAXIMUM MODE ONLY)



RESET TIMING

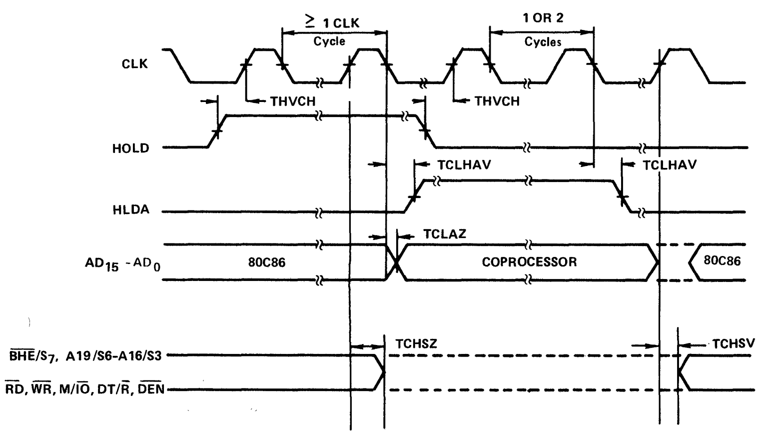


REQUEST/GRANT SEQUENCE TIMING (MAXIMUM MODE ONLY)



Note: The Coprocessor may not drive the busses outside the region shown without risking contention.

HOLD/HOLD ACKNOWLEDGE TIMING (MINIMUM MODE ONLY)



Instruction Set Summary

DATA TRANSFER

MOV = Move:	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
Register/memory to/from register	1 0 0 0 1 0 d w	mod reg r/m		
Immediate to register/memory	1 1 0 0 0 1 1 w	mod 0 0 0 r/m	data	data if w 1
Immediate to register	1 0 1 1 w reg	data	data if w 1	
Memory to accumulator	1 0 1 0 0 0 0 w	addr-low	addr-high	
Accumulator to memory	1 0 1 0 0 0 1 w	addr-low	addr-high	
Register/memory to segment register	1 0 0 0 1 1 1 0	mod 0 reg r/m		
Segment register to register/memory	1 0 0 0 1 1 0 0	mod 0 reg r/m		
PUSH = Push:				
Register/memory	1 1 1 1 1 1 1 1	mod 1 1 0 r/m		
Register	0 1 0 1 0 reg			
Segment register	0 0 0 reg 1 1 0			
POP = Pop:				
Register/memory	1 0 0 0 1 1 1 1	mod 0 0 0 r/m		
Register	0 1 0 1 1 reg			
Segment register	0 0 0 reg 1 1 1			
XCHG = Exchange:				
Register/memory with register	1 0 0 0 0 1 1 w	mod reg r/m		
Register with accumulator	1 0 0 1 0 reg			
IN=Input from:				
Fixed port	1 1 1 0 0 1 0 w	port		
Variable port	1 1 1 0 1 1 0 w			
OUT = Output to:				
Fixed port	1 1 1 0 0 1 1 w	port		
Variable port	1 1 1 0 1 1 1 w			
XLAT=Translate byte to AL	1 1 0 1 0 1 1 1			
LEA=Load EA to register	1 0 0 0 1 1 0 1	mod reg r/m		
LDS=Load pointer to DS	1 1 0 0 0 1 0 1	mod reg r/m		
LES=Load pointer to ES	1 1 0 0 0 1 0 0	mod reg r/m		
LAHF=Load AH with flags	1 0 0 1 1 1 1 1			
SAHF=Store AH into flags	1 0 0 1 1 1 1 0			
PUSHF=Push flags	1 0 0 1 1 1 0 0			
POPF=Pop flags	1 0 0 1 1 1 0 1			

ARITHMETIC

ADD = Add:				
Reg./memory with register to either	0 0 0 0 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 s w	mod 0 0 0 r/m	data	data if s w 01
Immediate to accumulator	0 0 0 0 0 1 0 w	data	data if w 1	
ADC = Add with carry:				
Reg./memory with register to either	0 0 0 1 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 s w	mod 0 1 0 r/m	data	data if s w 01
Immediate to accumulator	0 0 0 1 0 1 0 w	data	data if w 1	
INC = Increment:				
Register/memory	1 1 1 1 1 1 1 w	mod 0 0 0 r/m		
Register	0 1 0 0 0 reg			
AAA=ASCII adjust for add	0 0 1 1 0 1 1 1			
DAA=Decimal adjust for add	0 0 1 0 0 1 1 1			
SUB = Subtract:				
Reg./memory and register to either	0 0 1 0 1 0 d w	mod reg r/m		
Immediate from register/memory	1 0 0 0 0 0 s w	mod 1 0 1 r/m	data	data if s w 01
Immediate from accumulator	0 0 1 0 1 1 0 w	data	data if w 1	
SBB = Subtract with borrow				
Reg./memory and register to either	0 0 0 1 1 0 d w	mod reg r/m		
Immediate from register/memory	1 0 0 0 0 0 s w	mod 0 1 1 r/m	data	data if s w 01
Immediate from accumulator	0 0 0 1 1 1 0 w	data	data if w 1	

DEC Decrement:	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
Register/memory	1 1 1 1 1 1 1 w	mod 0 0 1 r/m		
Register	0 1 0 0 1 reg			
NEG Change sign	1 1 1 1 0 1 1 w	mod 0 1 1 r/m		
CMP Compare:				
Register/memory and register	0 0 1 1 1 0 d w	mod reg r/m		
Immediate with register/memory	1 0 0 0 0 0 s w	mod 1 1 1 r/m	data	data if s w 01
Immediate with accumulator	0 0 1 1 1 1 0 w	data	data if w 1	
AAS ASCII adjust for subtract	0 0 1 1 1 1 1 1			
DAS Decimal adjust for subtract	0 0 1 0 1 1 1 1			
MUL Multiply (unsigned)	1 1 1 1 0 1 1 w	mod 1 0 0 r/m		
IMUL Integer multiply (signed)	1 1 1 1 0 1 1 w	mod 1 0 1 r/m		
AAM ASCII adjust for multiply	1 1 0 1 0 1 0 0	0 0 0 0 1 0 1 0		
DIV Divide (unsigned)	1 1 1 1 0 1 1 w	mod 1 1 0 r/m		
IDIV Integer divide (signed)	1 1 1 1 0 1 1 w	mod 1 1 1 r/m		
AAD ASCII adjust for divide	1 1 0 1 0 1 0 1	0 0 0 0 1 0 1 0		
CBW Convert byte to word	1 0 0 1 1 0 0 0			
CWD Convert word to double word	1 0 0 1 1 0 0 1			

LOGIC

NOT Invert	1 1 1 1 0 1 1 w	mod 0 1 0 r/m		
SHL/SAL Shift logical/arithmetic left	1 1 0 1 0 0 v w	mod 1 0 0 r/m		
SHR Shift logical right	1 1 0 1 0 0 v w	mod 1 0 1 r/m		
SAR Shift arithmetic right	1 1 0 1 0 0 v w	mod 1 1 1 r/m		
ROL Rotate left	1 1 0 1 0 0 v w	mod 0 0 0 r/m		
ROR Rotate right	1 1 0 1 0 0 v w	mod 0 0 1 r/m		
RCL Rotate through carry flag left	1 1 0 1 0 0 v w	mod 0 1 0 r/m		
RCR Rotate through carry right	1 1 0 1 0 0 v w	mod 0 1 1 r/m		
AND And:				
Reg./memory and register to either	0 0 1 0 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 0 0 r/m	data	data if w 1
Immediate to accumulator	0 0 1 0 0 1 0 w	data	data if w 1	
TEST And function to flags, no result:				
Register/memory and register	1 0 0 0 0 1 0 w	mod reg r/m		
Immediate data and register/memory	1 1 1 1 0 1 1 w	mod 0 0 0 r/m	data	data if w 1
Immediate data and accumulator	1 0 1 0 1 0 0 w	data	data if w 1	
OR Or:				
Reg./memory and register to either	0 0 0 0 1 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 0 0 1 r/m	data	data if w 1
Immediate to accumulator	0 0 0 0 1 1 0 w	data	data if w 1	
XOR Exclusive or:				
Reg./memory and register to either	0 0 1 1 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 1 0 r/m	data	data if w 1
Immediate to accumulator	0 0 1 1 0 1 0 w	data	data if w 1	

STRING MANIPULATION

REP=Repeat	1 1 1 1 0 0 1 z
MOVS=Move byte/word	1 0 1 0 0 1 0 w
CMPS=Compare byte/word	1 0 1 0 0 1 1 w
SCAS=Scan byte/word	1 0 1 0 1 1 1 w
LODS=Load byte/wd to AL/AX	1 0 1 0 1 1 0 w
STOS=Stor byte/wd from AL/A	1 0 1 0 1 0 1 w

Instruction Set Summary

CONTROL TRANSFER

CALL = Call:	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
Direct within segment	1 1 1 0 1 0 0 0	disp-low	disp-high
Indirect within segment	1 1 1 1 1 1 1 1	mod 0 1 0 r/m	
Direct intersegment	1 0 0 1 1 0 1 0	offset-low	offset-high
		seg-low	seg-high
Indirect intersegment	1 1 1 1 1 1 1 1	mod 0 1 1 r/m	
JMP = Unconditional Jump:			
Direct within segment	1 1 1 0 1 0 0 1	disp-low	disp-high
Direct within segment-short	1 1 1 0 1 0 1 1	disp	
Indirect within segment	1 1 1 1 1 1 1 1	mod 1 0 0 r/m	
Direct intersegment	1 1 1 0 1 0 1 0	offset-low	offset-high
		seg-low	seg-high
Indirect intersegment	1 1 1 1 1 1 1 1	mod 1 0 1 r/m	
RET = Return from CALL:			
Within segment	1 1 0 0 0 0 1 1		
Within seg adding immed to SP	1 1 0 0 0 0 1 0	data-low	data-high
Intersegment	1 1 0 0 1 0 1 1		
Intersegment, adding immediate to SP	1 1 0 0 1 0 1 0	data-low	data-high
JE/JZ=Jump on equal/zero	0 1 1 1 0 1 0 0	disp	
JL/JNGE=Jump on less/not greater or equal	0 1 1 1 1 1 0 0	disp	
JLE/JNG=Jump on less or equal/not greater	0 1 1 1 1 1 1 0	disp	
JB/JNAE=Jump on below/not above or equal	0 1 1 1 0 0 1 0	disp	
JBE/JNA=Jump on below or equal/not above	0 1 1 1 0 1 1 0	disp	
JP/JPE=Jump on parity/parity even	0 1 1 1 1 0 1 0	disp	
JO=Jump on overflow	0 1 1 1 0 0 0 0	disp	
JS=Jump on sign	0 1 1 1 1 0 0 0	disp	
JNE/JNZ=Jump on not equal/not zero	0 1 1 1 0 1 0 1	disp	
JNL/JGE=Jump on not less/greater or equal	0 1 1 1 1 1 0 1	disp	
JNLE/JG=Jump on not less or equal/greater	0 1 1 1 1 1 1 1	disp	

	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
JNB/JAE Jump on not below/above or equal	0 1 1 1 0 0 1 1	disp
JNBE/JA Jump on not below or equal/above	0 1 1 1 0 1 1 1	disp
JNP/JPO Jump on not par/par odd	0 1 1 1 1 0 1 1	disp
JNO Jump on not overflow	0 1 1 1 0 0 0 1	disp
JNS Jump on not sign	0 1 1 1 1 0 0 1	disp
LOOP Loop CX times	1 1 1 0 0 0 1 0	disp
LOOPZ/LOOPE Loop while zero/equal	1 1 1 0 0 0 0 1	disp
LOOPNZ/LOOPNE Loop while not zero/equal	1 1 1 0 0 0 0 0	disp
JCXZ Jump on CX zero	1 1 1 0 0 0 1 1	disp
INT Interrupt		
Type specified	1 1 0 0 1 1 0 1	type
Type 3	1 1 0 0 1 1 0 0	
INTO Interrupt on overflow	1 1 0 0 1 1 1 0	
IRET Interrupt return	1 1 0 0 1 1 1 1	

PROCESSOR CONTROL

CLC Clear carry	1 1 1 1 1 0 0 0	
CMC Complement carry	1 1 1 1 0 1 0 1	
STC Set carry	1 1 1 1 1 0 0 1	
CLD Clear direction	1 1 1 1 1 1 0 0	
STD Set direction	1 1 1 1 1 1 0 1	
CLI Clear interrupt	1 1 1 1 1 0 1 0	
STI Set interrupt	1 1 1 1 1 0 1 1	
HLT Halt	1 1 1 1 0 1 0 0	
WAIT Wait	1 0 0 1 1 0 1 1	
ESC Escape (to external device)	1 1 0 1 1 x x x	mod x x x r/m
LOCK Bus lock prefix	1 1 1 1 0 0 0 0	

Footnotes:

AL = 8-bit accumulator
AX = 16-bit accumulator
CX = Count register
DS = Data segment
ES = Extra segment
Above/below refers to unsigned value.
Greater = more positive;
Less = less positive (more negative) signed values
if d = 1 then "to" reg; if d = 0 then "from" reg
if w = 1 then word instruction; if w = 0 then byte instruction

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low
if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP
DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.

if s:w = 01 then 16 bits of immediate data form the operand.
if s:w = 11 then an immediate data byte is sign extended to form the 16-bit operand.
if v = 0 then "count" = 1; if v = 1 then "count" in (CL)
x = don't care
z is used for string primitives for comparison with Z.F FLAG.

SEGMENT OVERRIDE PREFIX

0 0 1 reg 1 1 0

REG is assigned according to the following table:

16-Bit (w = 1)	8-Bit (w = 0)	Segment
000 AX	000 AL	00 ES
001 CX	001 CL	01 CS
010 DX	010 DL	10 SS
011 BX	011 BL	11 DS
100 SP	100 AH	
101 BP	101 CH	
110 SI	110 DH	
111 DI	111 BH	

Instructions which reference the flag register file as a 16-bit object use the symbol FLAGS to represent the file:

FLAGS = X:X:X:X:(OF):(DF):(IF):(TF):(SF):(ZF):X:(AF):X:(PF):X:(CF)

80C88

CMOS 8/16 Bit Microprocessor

Features

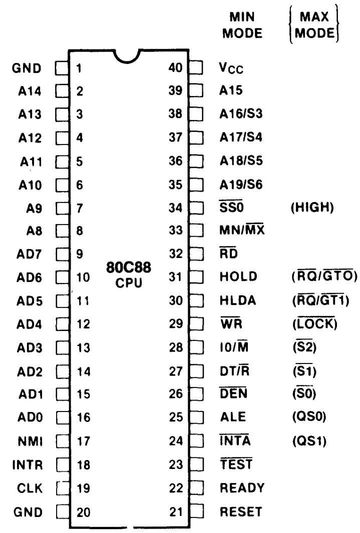
- Compatible with NMOS 8088
- Direct Software Compatibility with 80C86, 8086, 80C88
- 8-Bit Data bus Interface; 16-Bit Internal Architecture
- Completely Static CMOS Design
  - DC 5MHz (80C88)
  - DC 8MHz (80C88-2)
- Low Power Operation
  - ICCSB .... 500μA Maximum
  - ICCOP .... 10mA/MHz Maximum
- 1 Megabyte of Direct Memory Addressing Capability
- 24 Operand Addressing Modes
- Bit, Byte, Word, and Block Move Operations
- 8 and 16-Bit Signed/Unsigned Arithmetic
- Bus-Hold Circuitry Eliminates Pull-up Resistors
- Wide Operating Temperature Ranges
  - C80C88 .... -55°C to +125°C
  - I80C88 .... -40°C to + 85°C
  - M80C88 .... 0°C to +70°C

Description

The Harris 80C88 high performance 8/16-bit CMOS CPU is manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). Two modes of operation, MINimum for small systems and MAXimum for larger applications such as multiprocessing, allow user configuration to achieve the highest performance level. Full TTL compatibility and industry-standard operation allow use of existing NMOS 8088 hardware and Harris CMOS 80C86 peripherals. Complete software compatibility with the 80C86, 8086 and 8088 microprocessors allows use of existing software in new designs.

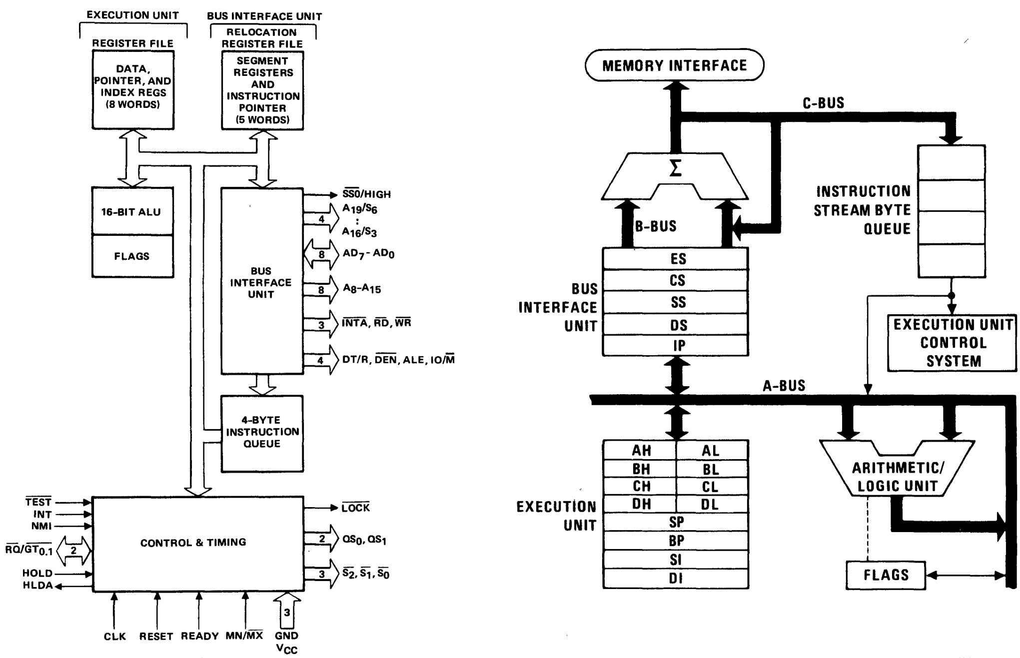
Pinout*

TOP VIEW



*LCC/PLCC Pinout on Page 3-47

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper I. C. handling procedures should be followed.

Pin Description

The following pin function descriptions are for 80C88 systems in either minimum or maximum mode. The "local bus" in these descriptions is the direct multiplexed bus interface connection to the 80C88 (without regard to additional bus buffers).

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
AD7-AD0	9-16	I/O	ADDRESS DATA BUS: These lines constitute the time multiplexed memory/IO address (T1) and data (T2, T3, Tw, and T4) bus. These lines are active HIGH and are held at high impedance to the last valid logic level during interrupt acknowledge and local bus "hold acknowledge" or "grant sequence".
A15-A8	2-8, 39	O	ADDRESS BUS: These lines provide address bits 8 through 15 for the entire bus cycle (T1-T4). These lines do not have to be latched by ALE to remain valid. A15-A8 are active HIGH and are held at high impedance to the last valid logic level during interrupt acknowledge and local bus "hold acknowledge" or "grant sequence".
A19/S6, A18/S5, A17/S4, A16/S3	35 36 37 38	O O O O	ADDRESS/STATUS: During T1, these are the four most significant address lines for memory operations. During I/O operations, these lines are LOW. During memory and I/O operations, status information is available on these lines during T2, T3, Tw, and T4. S6 is always low. The status of the interrupt enable flag bit (S5) is updated at the beginning of each clock cycle. S4 and S3 are encoded as shown. This information indicates which segment register is presently being used for data accessing. These lines are held at high impedance to the last valid logic level during local bus "hold acknowledge" or "grant sequence". S4 / S3 / CHARACTERISTICS: 0 / 0 / Alternate Data 0 / 1 / Stack 1 / 0 / Code or None 1 / 1 / Data
$\overline{RD}$	32	O	READ: Read strobe indicates that the processor is performing a memory or I/O read cycle, depending on the state of the IO/$\overline{M}$ pin or $\overline{S2}$. This signal is used to read devices which reside on the 80C88 local bus. $\overline{RD}$ is active LOW during T2, T3 and Tw of any read cycle, and is guaranteed to remain HIGH in T2 until the 80C88 local bus has floated. This line is held at a high impedance logic one state during "hold acknowledge" or "grant sequence".
READY	22	I	READY: is the acknowledgment from the addressed memory or I/O device that it will complete the data transfer. The RDY signal from memory or I/O is synchronized by the 82C84A clock generator to form READY. This signal is active HIGH. The 80C88 READY input is not synchronized. Correct operation is not guaranteed if the set up and hold times are not met.
INTR	18	I	INTERRUPT REQUEST: is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. A subroutine is vectored to via an interrupt vector lookup table located in system memory. It can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized. This signal is active HIGH.
$\overline{TEST}$	23	I	TEST: input is examined by the "wait for test" instruction. If the $\overline{TEST}$ input is LOW, execution continues, otherwise the processor waits in an "idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK.
NMI	17	I	NON-MASKABLE INTERRUPT: is an edge triggered input which causes a type 2 interrupt. A subroutine is vectored to via an interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from a LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized.
RESET	21	I	RESET: causes the processor to immediately terminate its present activity. The signal must transition LOW to HIGH and remain active HIGH for at least four clock cycles. It restarts execution, as described in the instruction set description, when RESET returns LOW. RESET is internally synchronized.
CLK	19	I	CLOCK: provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing.
V_{CC}	40		V_{CC}: is the +5 V power supply pin. A 0.1 μF capacitor between pins 20 and 40 is recommended for decoupling.
GND	1, 20		GND: are the ground pins (both pins must be connected to system ground). A 0.1 μF capacitor between pins 1 and 20 is recommended for decoupling.
MN/$\overline{MX}$	33	I	MINIMUM/MAXIMUM: indicates the mode in which the processor is to operate. The two modes are discussed in the following sections.

Pin Description

The following pin descriptions are for the 80C88 system in maximum mode (i.e., MN/$\overline{MX}$ = GND). Only the pin functions which are unique to maximum mode are described; all other pin functions are as described above.

MAX MODE SYSTEM

<table>
<tr><th>SYMBOL</th><th>PIN NUMBER</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>$\overline{S0}$
$\overline{S1}$
$\overline{S2}$</td><td>26
27
28</td><td>O</td><td>STATUS: is active during clock high of T4, T1, and T2, and is returned to the passive state (1,1,1) during T3 or during Tw when READY is HIGH. This status is used by the 82C88 bus controller to generate all memory and I/O access control signals. Any change by $\overline{S2}$, $\overline{S1}$, or $\overline{S0}$ during T4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T3 or Tw is used to indicate the end of a bus cycle.

These signals are held at a high impedance logic one state during "grant sequence".

<table>
<tr><th>$\overline{S2}$</th><th>$\overline{S1}$</th><th>$\overline{S0}$</th><th>CHARACTERISTICS</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Interrupt Acknowledge</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Read I/O port</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Write I/O port</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Halt</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Code access</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Read memory</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Write memory</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Passive</td></tr>
</table></td></tr>
<tr><td>$\overline{RQ}/\overline{GT0}$,
$\overline{RQ}/\overline{GT1}$</td><td>31
30</td><td>I/O</td><td>REQUEST/GRANT: pins are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle. Each pin is bidirectional with $\overline{RQ}/\overline{GT0}$ having higher priority than $\overline{RQ}/\overline{GT1}$. $\overline{RQ}/\overline{GT}$ has internal bus-hold high circuitry and, if unused, may be left unconnected. The request/grant sequence is as follows (see RQ/GT Timing Sequence):

1. A pulse of one CLK wide from another local bus master indicates a local bus request ("hold") to the 80C88 (pulse 1).
2. During a T4 or TI clock cycle, a pulse one clock wide from the 80C88 to the requesting master (pulse 2), indicates that the 80C88 has allowed the local bus to float and that it will enter the "grant sequence" state at the next CLK. The CPU's bus interface unit is disconnected logically from the local bus during "grant sequence".
3. A pulse one CLK wide from the requesting master indicates to the 80C88 (pulse 3) that the "hold" request is about to end and that the 80C88 can reclaim the local bus at the the next CLK. The CPU then enters T4 (or TI if no bus cycles pending).

Each master-master exchange of the local bus is a sequence of three pulses. There must be one idle CLK cycle after each bus exchange. Pulses are active LOW.

If the request is made while the CPU is performing a memory cycle, it will release the local bus during T4 of the cycle when all the following conditions are met:
1. Request occurs on or before T2.
2. Current cycle is not the low bit of a word.
3. Current cycle is not the first acknowledge of an interrupt acknowledge sequence.
4. A locked instruction is not currently executing.

If the local bus is idle when the request is made the two possible events will follow:
1. Local bus will be released during the next clock.
2. A memory cycle will start within 3 clocks. Now the four rules for a currently active memory cycle apply with condition number 1 already satisfied.</td></tr>
<tr><td>$\overline{LOCK}$</td><td>29</td><td>O</td><td>LOCK: indicates that other system bus masters are not to gain control of the system bus while $\overline{LOCK}$ is active (LOW). The $\overline{LOCK}$ signal is activated by the "LOCK" prefix instruction and remains active until the completion of the next instruction. This signal is active LOW, and is held at a high impedance logic one state during "grant sequence". In Max mode, $\overline{LOCK}$ is automatically generated during T2 of the first INTA cycle and removed during T2 of the second INTA cycle.</td></tr>
<tr><td>QS1,
QS0</td><td>24, 25</td><td>O</td><td>QUEUE STATUS: provide status to allow external tracking of the internal 80C88 instruction queue.

The queue status is valid during the CLK cycle after which the queue operation is performed. Note that the queue status never goes to a high impedance state (floated).

<table>
<tr><th>QS1</th><th>QS0</th><th>CHARACTERISTICS</th></tr>
<tr><td>0</td><td>0</td><td>No operation</td></tr>
<tr><td>0</td><td>1</td><td>First byte of opcode from queue</td></tr>
<tr><td>1</td><td>0</td><td>Empty the queue</td></tr>
<tr><td>1</td><td>1</td><td>Subsequent byte from queue</td></tr>
</table></td></tr>
<tr><td>– –</td><td>34</td><td>O</td><td>Pin 34 is always a logic one in the maximum mode and is held at a high impedance logic one during a "grant sequence".</td></tr>
</table>

Pin Description

The following pin function descriptions are for the 80C88 minimum mode (i.e., MN/$\overline{MX}$ = V_{CC}). Only the pin functions which are unique to the minimum mode are described; all other pin functions are as described above.

MINIMUM MODE SYSTEM

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
IO/$\overline{M}$	28	O	STATUS LINE: is an inverted maximum mode $\overline{S2}$. It is used to distinguish a memory access from an I/O access. IO/$\overline{M}$ becomes valid in the T4 preceding a bus cycle and remains valid until the final T4 of the cycle (I/O=HIGH, M = LOW). IO/$\overline{M}$ is held to a high impedance logic zero during local bus "hold acknowledge".
$\overline{WR}$	29	O	WRITE: strobe indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the IO/$\overline{M}$ signal. $\overline{WR}$ is active for T2, T3, and Tw of any write cycle. It is active LOW, and is held to high impedance logic one during local bus "hold acknowledge".
$\overline{INTA}$	24	O	INTA: is used as a read strobe for interrupt acknowledge cycles. It is active LOW during T2, T3, and Tw of each interrupt acknowledge cycle. Note that $\overline{INTA}$ is never floated.
ALE	25	O	ADDRESS LATCH ENABLE: is provided by the processor to latch the address into the 82C82/82C83 address latch. It is a HIGH pulse active during clock low of T1 of any bus cycle. Note that ALE is never floated.
DT/$\overline{R}$	27	O	DATA TRANSMIT/RECEIVE: is needed in a minimum system that desires to use an 82C86/82C87 data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically, DT/$\overline{R}$ is equivalent to $\overline{S1}$ in the maximum mode, and its timing is the same as for IO/$\overline{M}$ (T = HIGH, R = LOW). This signal is held to a high impedance logic one during local bus "hold acknowledge".
$\overline{DEN}$	26	O	DATA ENABLE: is provided as an output enable for the 82C86/82C87 in a minimum system which uses the trasceiver. $\overline{DEN}$ is active LOW during each memory and I/O access, and for $\overline{INTA}$ cycles. For a read or $\overline{INTA}$ cycle, it is active from the middle of T2 until the middle of T4, while for a write cycle, it is active from the beginning of T2 until the middle of T4. $\overline{DEN}$ is held to high impedance logic one during local bus "hold acknowledge".
HOLD, HLDA	31 30	I O	HOLD: indicates that another master is requesting a local bus "hold". To be acknowledged, HOLD must be active HIGH. The processor receiving the "hold" request will issue HLDA (HIGH) as an acknowledgment, in the middle of a T4 or TI clock cycle. Simultaneous with the issuance of HLDA the processor will float the local bus and control lines. After HOLD is detected as being LOW, the processor lowers HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines. Hold is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the set up time.
$\overline{SS0}$	34	O	STATUS LINE: is logically equivalent to $\overline{S0}$ in the maximum mode. The combination of $\overline{SS0}$, IO/$\overline{M}$, and DT/$\overline{R}$allows the system to completely decode the current bus cycle status. $\overline{SS0}$ is held to high impedance logic one during local bus "hold acknowledge".

IO/$\overline{M}$	DT/$\overline{R}$	$\overline{SS0}$	CHARACTERISTICS
1	0	0	Interrupt Acknowledge
1	0	1	Read I/O port
1	1	0	Write I/O port
1	1	1	Halt
0	0	0	Code access
0	0	1	Read memory
0	1	0	Write memory
0	1	1	Passive

Functional Description

Static Operation

All 80C88 circuitry is static in design. Internal registers, counters and latches are static and require no refresh as with dynamic circuit design. This eliminates the minimum operating frequency restriction placed on other microprocessors. The CMOS 80C88 can operate from DC to the specified upper frequency limit. The processor clock may be stopped in either state (high/low) and held there indefinitely. This type of operation is especially useful for system debug or power critical applications.

The 80C88 can be single stepped using only the CPU clock. This state can be maintained as long as is necessary. Single step clock operation allows simple interface circuitry to provide critical information for start-up.

Static design also allows very low frequency operation (as low as DC). In a power critical situation, this can provide extremely low power operation since 80C88 power dissipation is directly related to operating frequency. As the system frequency is reduced, so is the operating power until, at a DC input frequency, the power requirement is the 80C88 standby current.

Internal Architecture

The internal functions of the 80C88 processor are partitioned logically into two processing units. The first is the Bus Interface Unit (BIU) and the second is the Execution Unit (EU) as shown in the CPU block diagram.

These units can interact directly but for the most part perform as separate asynchronous operational processors. The bus interface unit provides the functions related to instruction fetching and queuing, operand fetch and store, and address relocation. This unit also provides the basic bus control. The overlap of instruction pre-fetching provided by this unit serves to increase processor performance through improved bus bandwidth utilization. Up to 4 bytes of the instruction stream can be queued while waiting for decoding and execution.

The instruction stream queuing mechanism allows the BIU to keep the memory utilized very efficiently. Whenever there is space for at least 1 byte in the queue, the BIU will attempt a byte fetch memory cycle. This greatly reduces "dead time" on the memory bus. The queue acts as a First-In-First-Out (FIFO) buffer, from which the EU extracts instruction bytes as required. If the queue is empty (following a branch instruction, for example), the first byte into the queue immediately becomes available to the EU.

The execution unit receives pre-fetched instructions from the BIU queue and provides un-relocated operand addresses to the BIU. Memory operands are passed through the BIU for processing by the EU, which passes results to the BIU for storage.

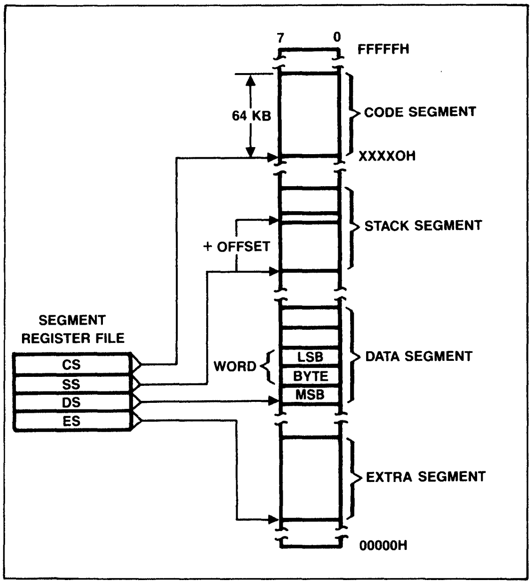


Figure 1. Memory Organization

Memory Organization

The processor provides a 20-bit address to memory which locates the byte being referenced. The memory is organized as a linear array of up to 1 million bytes, addressed as 00000(H) to FFFFF(H). The memory is logically divided into code, data, extra, and stack segments of up to 64K bytes each, with each segment falling on 16-byte boundaries. (See FIGURE 1).

All memory references are made relative to base addresses contained in high speed segment registers. The segment types were chosen based on the addressing needs of programs. The segment register to the selected is automatically chosen according to specific rules as shown in Table 2. All information in one segment type share the same logical attributes (e.g., code or data). By structuring memory into relocatable areas of similar characteristics and by automatically selecting segment registers, programs are shorter, faster, and more structured.

Word (16-bit) operands can be located on even or odd address boundaries. For address and data operands, the least significant byte of the word is stored in the lower valued address location and the most significant byte in the next higher address location.

Table 2.

Memory Reference Need	Segment Register Used	Segment Selection Rule
Instructions	CODE (CS)	Automatic with all instruction prefetch.
Stack	STACK (SS)	All stack pushes and pops. Memory references relative to BP base register except data references.
Local Data	DATA (DS)	Data references when: relative to stack, destination of string operation, or explicitly overridden.
External (Global) Data	EXTRA (ES)	Destination of string operations: Explicitly selected using a segment override.

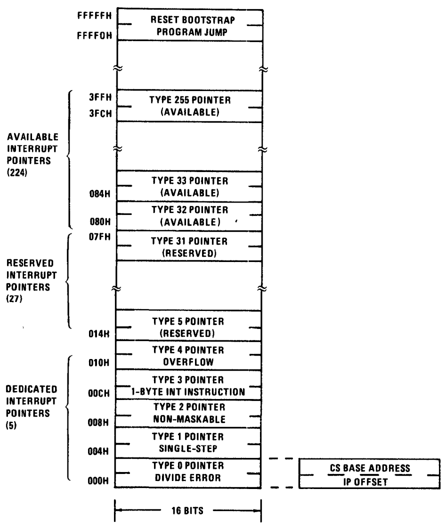


Figure 2. Reserved Memory Locations

The BIU will automatically execute two fetch or write cycles for 16-bit operands.

Certain locations in memory are reserved for specific CPU operations. (See FIGURE 2). Locations from addresses FFFF0H through FFFFFH are reserved for operations including a jump to the initial system initialization routine. Following RESET, the CPU will always begin execution at location FFFF0H where the jump must be located. Locations 00000H through 003FFH are reserved for interrupt operations. Each of the 256 possible interrupt service routines is accessed through its own pair of 16-bit pointers — segment address pointer and offset address pointer. The first pointer, used as the offset address, is loaded into the IP, and the second pointer, which designates the base address, is loaded into the CS. At this point program control is transferred to the interrupt routine. The pointer elements are assumed to have been stored at their respective places in reserved memory prior to the occurrence of interrupts.

Minimum and Maximum Modes

The requirements for supporting minimum and maximum 80C88 systems are sufficiently different that they cannot be done efficiently with 40 uniquely defined pins. Consequently, the 80C88 is equipped with a strap pin (MN/$\overline{MX}$) which defines the system configuration. The definition of a certain subset of the pins changes, dependent on the condition of the strap pin. When the MN/$\overline{MX}$ pin is strapped to GND, the 80C88 defines pins 24 through 31 and 34 in maximum mode. When the MN/$\overline{MX}$ pin is strapped to VCC, the 80C88 generates bus control signals itself on pins 24 through 31 and 34.

The minimum mode 80C88 can be used with either a multiplexed or demultiplexed bus. This architecture provides the 80C88 processing power in a highly integrated form.

The demultiplexed mode requires one latch (for 64K addressability) or two latches (for a full megabyte of addressing). An 82C86 or 82C87 transceiver can also be used if data bus buffering is required. (See FIGURE 3.) The 80C88 provides $\overline{DEN}$ and DT/$\overline{R}$ to control the transceiver, and ALE to latch the addresses. This configuration of the minimum mode provides the standard demultiplexed bus structure with heavy bus buffering and relaxed bus timing requirements.

The maximum mode employs the 82C88 bus controller (See FIGURE 4). The 82C88 decodes status lines $\overline{S0}$, $\overline{S1}$, and $\overline{S2}$, and provides the system with all bus control signals. Moving the bus control to the 82C88 provides better source and sink current capability to the control lines, and frees the 80C88 pins for extended large system features. Hardware lock, queue status, and two request/grant interfaces are provided by the 80C88 in maximum mode. These features allow coprocessors in local bus and remote bus configurations.

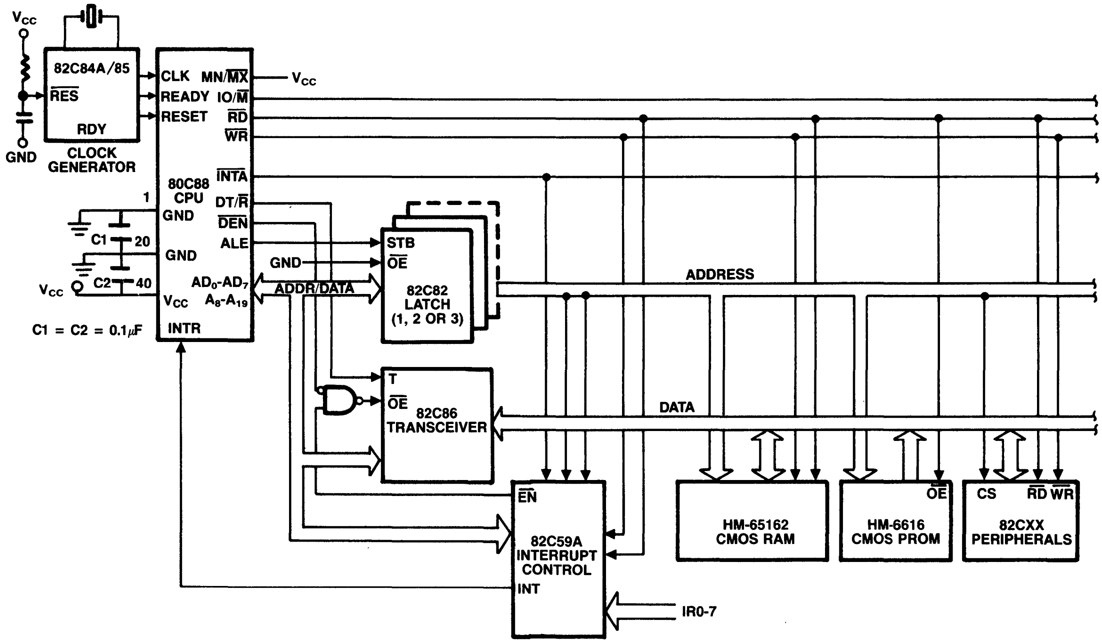


Figure 3. Demultiplexed Bus Configuration

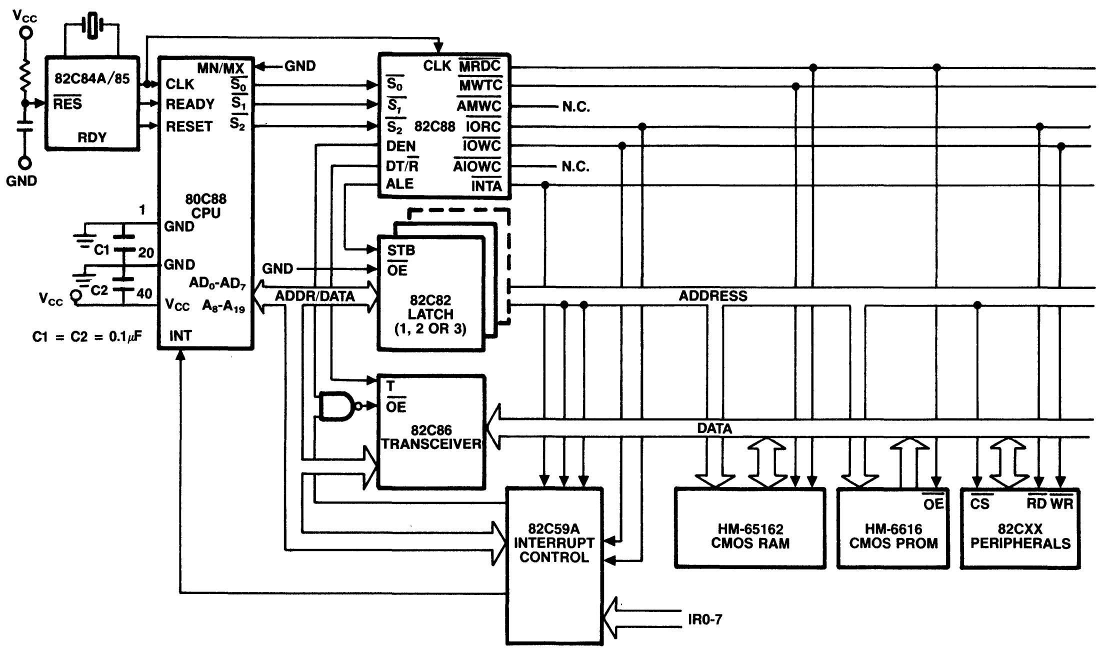


Figure 4. Fully Buffered System Using Bus Controller

Bus Operation

The 80C88 address/data bus is broken into three parts – the lower eight address/data bits (AD0-AD7), the middle eight address bits (A8-A15), and the upper four address bits (A16-A19). The address/data bits and the highest four address bits are time multiplexed. This technique provides the most efficient use of pins on the processor, permitting the use of a standard 40 lead package. The middle eight address bits are not multiplexed, i.e. they remain valid throughout each bus cycle. In addition, the bus can be demultiplexed at the processor with a single address latch if a standard, non-multiplexed bus is desired for the system.

Each processor bus cycle consists of at least four CLK cycles. These are referred to as T1, T2, T3, and T4. (See FIGURE 5). The address is emitted from the processor during T1 and data transfer occurs on the bus during T3 and T4. T2 is used primarily for changing the direction of the bus during read operations. In the event that a "NOT READY" indication is given by the addressed device, "wait" states (Tw) are inserted between T3 and T4. Each inserted "wait" state is of the same duration as a CLK cycle. Periods can occur between 80C88 driven bus cycles. These are referred to as "idle" states (Ti), or inactive CLK cycles. The processor uses these cycles for internal housekeeping.

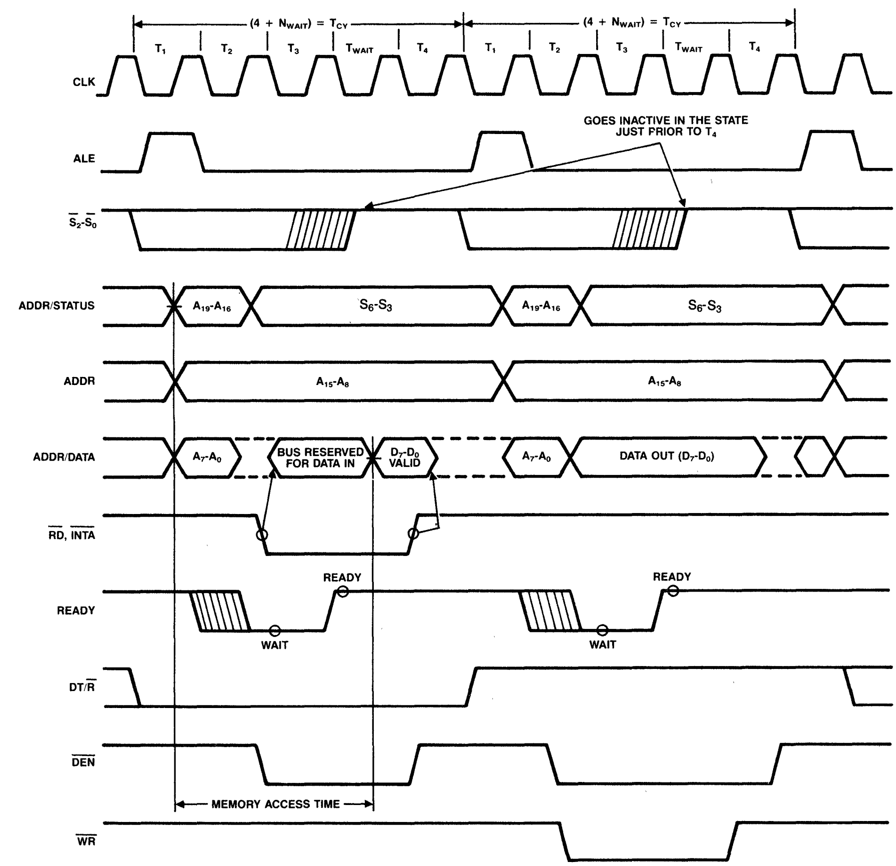


Figure 5. Basic System Timing

During T1 of any bus cycle, the ALE (address latch enable) signal is emitted (by either the processor or the 82C88 bus controller, depending on the MN/$\overline{MX}$ strap). At the trailing edge of this pulse, a valid address and certain status information for the cycle may be latched.

Status bits $\overline{S0}$, $\overline{S1}$, and $\overline{S2}$ are used by the bus controller, in maximum mode, to identify the type of bus transaction according to the following table:

$\overline{S}_2$	$\overline{S}_1$	$\overline{S}_0$	CHARACTERISTICS
0	0	0	Interrupt Acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (no bus cycle)

Table 3.

Status bits S_3 through S_6 are multiplexed with high order address bits and are therefore valid during T2 through T4. S_3 and S_4 indicate which segment register was used for this bus cycle in forming the address according to the following table:

S_4	S_3	CHARACTERISTICS
0	0	Alternate Data (extra segment)
0	1	Stack
1	0	Code or None
1	1	Data

Table 4.

S_5 is a reflection of the PSW interrupt enable bit. S_6 is always equal to 0.

I/O Addressing

In the 80C88, I/O operations can address up to a maximum of 64K I/O registers. The I/O address appears in the same format as the memory address on bus lines A15-A0. The address lines A19-A16 are zero in I/O operations. The variable I/O instructions, which use register DX as a pointer, have full address capability, while the direct I/O instructions directly address one or two of the 256 I/O byte locations in page 0 of the I/O address space. I/O ports are addressed in the same manner as memory locations.

Designers familiar with the 8085 or upgrading an 8085 design should note that the 8085 address I/O with an 8-bit address on both halves of the 16-bit address bus. The 80C88 uses a full 16-bit address on its lower 16 address lines.

External Interface

Processor Reset and Initialization

Processor initialization or start up is accomplished with activation (HIGH) of the RESET pin. The 80C88 RESET is required to be HIGH for greater than four clock cycles. The 80C88 will terminate operations on the high-going edge of RESET and will remain dormant as long as RESET is HIGH. The low-going transition of RESET triggers an internal reset sequence for approximately 7 clock cycles. After this interval the 80C88 operates normally, beginning with the instruction in absolute location FFFF0H (see FIGURE 2). The RESET input is internally synchronized to the processor clock. At initialization, the HIGH to LOW transition of RESET must occur no sooner than 50 μs after power up, to allow complete initialization of the 80C88.

NMI will not be recognized if asserted prior to the second CLK cycle following the end of RESET.

Bus Hold Circuitry

To avoid high current conditions caused by floating inputs to CMOS devices and to eliminate the need for pull-up/down resistors, "bus-hold" circuitry has been used on 80C88 pins 2-16, 26-32 and 34-39 (see FIGURE 6A, 6B). These circuits maintain a valid logic state if no driving source is present (i.e.,

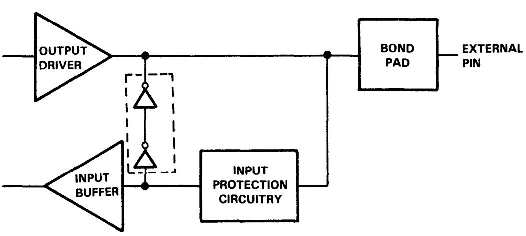


Figure 6A. Bus hold circuitry pin 2-16, 35-39.

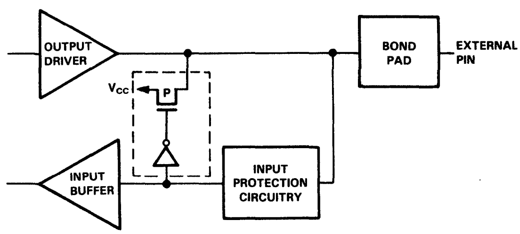


Figure 6B. Bus hold circuitry pin 26-32, 34.

3
CMOS 80C86 FAMILY

an unconnected pin or a driving source which goes to a high impedance state).

To overdrive the "bus hold" circuits, an external driver must be capable of supplying 400µA minimum sink or source current at valid input voltage levels. Since this "bus hold" circuitry is active and not a "resistive" type element, the associated power supply current is negligible. Power dissipation is significantly reduced when compared to the use of passive pull-up resistors.

Interrupt Operations

Interrupt operations fall into two classes: software or hardware initiated. The software initiated interrupts and software aspects of hardware interrupts are specified in the instruction set description. Hardware interrupts can be classified as non-maskable or maskable.

Interrupts result in a transfer of control to a new program location. A 256 element table containing address pointers to the interrupt service program locations resides in absolute locations 0 through 3FFH (see FIGURE 2), which are reserved for this purpose. Each element in the table is 4 bytes in size and corresponds to an interrupt "type." An interrupting device supplies an 8-bit type number, during the interrupt acknowledge sequence, which is used to vector through the appropriate element to the new interrupt service program location.

Non-Maskable Interrupt (NMI)

The processor provides a single non-maskable interrupt (NMI) pin which has higher priority than the maskable interrupt request (INTR) pin. A typical use would be to activate a power failure routine. The NMI is edge-triggered on a LOW to HIGH transition. The activation of this pin causes a type 2 interrupt.

NMI is required to have a duration in the HIGH state of greater than two clock cycles, but is not required to be synchronized to the clock. Any high going transition of NMI is latched on-chip and will be serviced at the end of the current instruction or between whole moves (2 bytes in the case of word moves) of a block type instruction. Worst case response to NMI would be for multiply, divide, and variable shift instructions. There is no specification on the occurrence of the low-going edge; it may occur before, during, or after the servicing of NMI. Another high-going edge triggers another response if it occurs after the start of the NMI procedure.

The signal must be free of logical spikes in general and be free of bounces on the low-going edge to avoid triggering extraneous responses.

Maskable Interrupt (INTR)

The 80C88 provides a single interrupt request input (INTR) which can be masked internally by software with the resetting of the interrupt enable (IF) flag bit. The interrupt request signal is level triggered. It is internally synchronized during each clock cycle on the high-going edge of CLK.

To be responded to, INTR must be present (HIGH) during the clock period preceding the end of the current instruction or the end of a whole move for a block type instruction. INTR may be removed anytime after the falling edge of the first INTA signal. During interrupt response sequence, further interrupts are disabled. The enable bit is reset as part of the response to any interrupt (INTR, NMI, software interrupt, or single step). The FLAGS register, which is automatically pushed onto the stack, reflects the state of the processor prior to the interrupt. The enable bit will be zero until the old FLAGS register is restored, unless specifically set by an instruction.

During the response sequence (see FIGURE 7), the processor executes two successive (back to back) interrupt acknowledge cycles. The 80C88 emits the LOCK signal (maximum mode only) from T2 of the first bus cycle until T2 of the second. A local bus "hold" request will not be honored until the end of the second bus cycle. In the second bus cycle, a byte is fetched from the external interrupt system (e.g., 82C59A PIC) which identifies the source (type) of the interrupt. This byte is multiplied by four and used as a pointer into the interrupt vector lookup table.

An INTR signal left HIGH will be continually responded to within the limitations of the enable bit and sample period. INTR may be removed anytime after the falling edge of the first INTA signal. The interrupt return instruction includes a flags pop which returns the status of the original interrupt enable bit when it restores the flags.

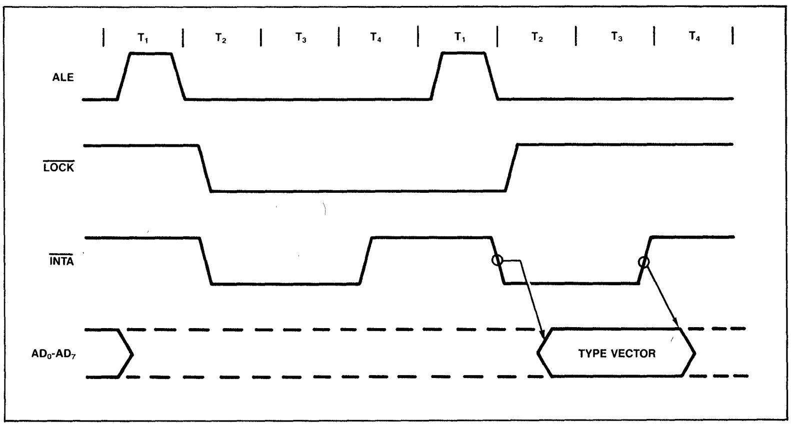


Figure 7. Interrupt Acknowledge Sequence

Halt

When a software HALT instruction is executed, the processor indicates that it is entering the HALT state in one of two ways, depending upon which mode is strapped. In minimum mode, the processor issues ALE, delayed by one clock cycle, to allow the system to latch the halt status. Halt status is available on IO/$\overline{M}$, DT/$\overline{R}$, and $\overline{SS0}$. In maximum mode, the processor issues appropriate HALT status on $\overline{S2}$, $\overline{S1}$, and $\overline{S0}$, and the 82C88 bus controller issues one ALE. The 80C88 will not leave the HALT state when a local bus hold is entered while in HALT. In this case, the processor reissues the HALT indicator at the end of the local bus hold. An interrupt request or RESET will force the 80C88 out of the HALT state.

Read/Modify/Write (Semaphore) Operations Via LOCK

The LOCK status information is provided by the processor when consecutive bus cycles are required during the execution of an instruction. This allows the processor to perform read/modify/write operations on memory (via the "exchange register with memory" instruction), without another system bus master receiving intervening memory cycles. This is useful in multiprocessor system configurations to accomplish "test and set lock" operations. The $\overline{LOCK}$ signal is activated (LOW) in the clock cycle following decoding of the LOCK prefix instruction. It is deactivated at the end of the last bus cycle of the instruction following the $\overline{LOCK}$ prefix. While $\overline{LOCK}$ is active, a request on a $\overline{RQ}/\overline{GT}$ pin will be recorded, and then honored at the end of the LOCK.

External Synchronization Via $\overline{TEST}$

As an alternative to interrupts, the 80C88 provides a single software-testable input pin ($\overline{TEST}$). This input is utilized by executing a WAIT instruction. The single WAIT instruction is repeatedly executed until the TEST input goes active (LOW). The execution of WAIT does not consume bus cycles once the queue is full.

If a local bus request occurs during WAIT execution, the 80C88 3-states all output drivers while inputs and I/O pins are held at valid logic levels by internal bus-hold circuits. If interrupts are enabled, the 80C88 will recognize interrupts and process them when it regains control of the bus.

Basic System Timing

In minimum mode, the MN/$\overline{MX}$ pin is strapped to V_{CC} and the processor emits bus control signals ($\overline{RD}$, $\overline{WR}$, IO/$\overline{M}$, etc.) directly. In maximum mode, the MN/$\overline{MX}$ pin is strapped to GND and the processor emits coded status information which the 82C88 bus controller uses to generate MULTIBUS™ compatible bus control signals.

System Timing – Minimum System

The read cycle begins in T1 with the assertion of the address latch enable (ALE) signal (See FIGURE 5). The trailing (low going) edge of this signal is used to latch the address information, which is valid on the address/data bus (AD0-AD7) at this time, into the 82C82/82C83 latch. Address lines A8 through A15 do not need to be latched because they remain valid throughout the bus cycle. From T1 to T4 the IO/$\overline{M}$ signal indicates a memory or I/O operation. At T2 the address is removed from the address/data bus and the bus is held at the last valid logic state by internal bus-hold devices. The read control signal is also asserted at T2. The read ($\overline{RD}$) signal causes the addressed device to enable its data bus drivers to the local bus. Some time later, valid data will be available on the bus and the addressed device will drive the READY line HIGH. When the processor returns the read signal to a HIGH level, the addressed device will again 3-state its bus drivers. If a transceiver (82C86/82C87) is required to buffer the local bus, signals DT/$\overline{R}$ and $\overline{DEN}$ are provided by the 80C88.

A write cycle also begins with the assertion of ALE and the emission of the address. The IO/$\overline{M}$ signal is again asserted to indicate a memory or I/O write operation. In T2, immediately following the address emission, the processor emits the data to be written into the addressed location. This data remains valid until at least the middle of T4. During T2, T3, and Tw, the processor asserts the write control signal. The write ($\overline{WR}$) signal becomes active at the beginning of T2, as opposed to the read, which is delayed somewhat into T2 to provide time for output drivers to become inactive.

The basic difference between the interrupt acknowledge cycle and a read cycle is that the interrupt acknowledge ($\overline{INTA}$) signal is asserted in place of the read ($\overline{RD}$) signal and the address bus is held at the last valid logic state by internal bus-hold devices (see FIGURE 6). In the second of two successive INTA cycles, a byte of information is read from the data bus, as supplied by the interrupt system logic (i.e., 82C59A priority interrupt controller). This byte identifies the source (type) of the interrupt. It is multiplied by four and used as a pointer into the interrupt vector lookup table, as described earlier.

Bus Timing – Medium Complexity Systems

For medium complexity systems, the MN/$\overline{MX}$ pin is connected to GND and the 82C88 bus controller is added to the system, as well as an 82C82/82C83 latch for latching the system address, and an 82C86/82C87 transceiver to allow for bus loading greater than the 80C88 is capable of handling (see FIGURE 8). Signals ALE, $\overline{DEN}$, and DT/$\overline{R}$ are generated by the 82C88 instead of the processor in this configuration, although their timing remains relatively the same. The 80C88 status outputs ($\overline{S2}$, $\overline{S1}$, and $\overline{S0}$) provide type of cycle information and become 82C88 inputs. This bus cycle information specifies read (code, data, or I/O), write (data or I/O), interrupt acknowledge, or software halt. The 82C88 thus issues control signals specifying memory read or write, I/O read or write, or interrupt acknowledge. The 82C88 provides two types of write strobes, normal and advanced, to be applied as required. The normal write strobes have data valid at the leading edge of write. The advanced write strobes have the same timing as read strobes, and hence, data is not valid at the leading edge of write. The 82C86/82C87 transceiver receives the usual T and $\overline{OE}$ inputs from the 82C88 DT/$\overline{R}$ and $\overline{DEN}$ outputs.

The pointer into the interrupt vector table, which is passed during the second $\overline{INTA}$ cycle, can derive from an 82C59A located on either the local bus or the system bus. If the master 82C59A priority interrupt controller is positioned on the local bus, the 82C86/82C87 transceiver must be disabled when reading from the master 82C59A during the interrupt acknowledge sequence and software "poll".

The 80C88 Compared To The 80C86

The 80C88 CPU is an 8-bit processor designed around the 8086 internal structure. Most internal functions of the 80C88 are identical to the equivalent 80C86 functions. The 80C88 handles the external bus the same way the 80C86 does with the distinction of handling only 8 bits at a time. Sixteen-bit

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operands are fetched or written in two consecutive bus cycles. Both processors will appear identical to the software engineer, with the exception of execution time. The internal register structure is identical and all instructions have the same end result. Internally, there are three differences between the 80C88 and the 80C86. All changes are related to the 8-bit bus interface.

- The queue length is 4 bytes in the 80C88, whereas the 80C86 queue contains 6 bytes, or three words. The queue was shortened to prevent overuse of the bus by the BIU when prefetching instructions. This was required because of the additional time necessary to fetch instructions 8 bits at a time.
- To further optimize the queue, the prefetching algorithm was changed. The 80C88 BIU will fetch a new instruction to load into the queue each time there is a 1 byte space available in the queue. The 80C86 waits until a 2-byte space is available.
- The internal execution time of the instruction set is affected by the 8-bit interface. All 16-bit fetches and writes from/to memory take an additional four clock cycles. The CPU is also limited by the speed of instruction fetches. This latter problem only occurs when a series of simple operations occur. When the more sophisticated instructions of the 80C88 are being used, the queue has time to fill and the execution proceeds as fast as the execution unit will allow.

The 80C88 and 80C86 are completely software compatible by virtue of their identical execution units. Software that is system dependent may not be completely transferable, but software that is not system dependent will operate equally as well on an 80C88 or an 80C86.

The hardware interface of the 80C88 contains the major differences between the two CPUs. The pin assignments are nearly identical, however, with the following functional changes:

- A8-A15 – These pins are only address outputs on the 80C88. These address lines are latched internally and remain valid throughout a bus cycle in a manner similar to the 8085 upper address lines.
- $\overline{BHE}$ has no meaning on the 80C88 and has been eliminated.
- $\overline{SS0}$ provides the $\overline{S0}$ status information in the minimum mode. This output occurs on pin 34 in minimum mode only. DT/$\overline{R}$, IO/$\overline{M}$, and $\overline{SS0}$ provide the complete bus status in minimum mode.
- IO/$\overline{M}$ has been inverted to be compatible with the 8085 bus structure.
- ALE is delayed by one clock cycle in the minimum mode when entering HALT, to allow the status to be latched with ALE.

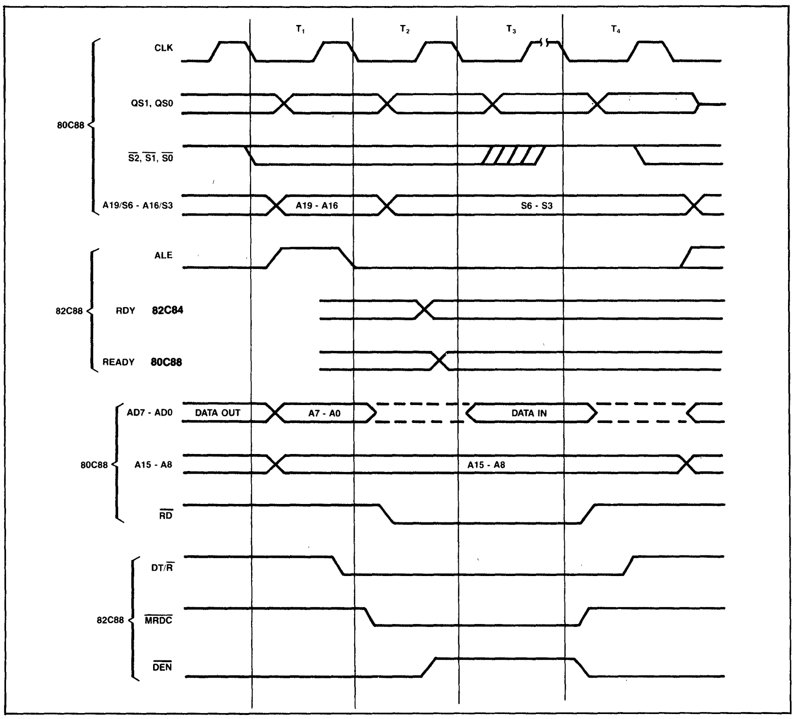


Figure 8. Medium Complexity System Timing

Absolute Maximum Ratings

Supply Voltage .... +8.0 Volts
Input, Output or I/O Voltage Applied .... GND -0.5V to VCC +0.5V
Storage Temperature Range .... -65°C to +150°C
Maximum Package Power Dissipation .... 1 Watt
θ_{jc} .... 16°C/W (CERDIP Package), 21°C/W (LCC Package)
θ_{ja} .... 36°C/W (CERDIP Package), 41°C/W (LCC Package)
Gate Count .... 9750 Gates
Junction Temperature .... +150°C
Lead Temperature (Soldering, Ten Seconds) .... +260°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +4.5V to +5.5V
M80C88-2 Only .... +4.75V to +5.25V
Operating Temperature Range
C80C88 .... 0°C to +70°C
I80C88 .... -40°C to +85°C
M80C88 .... -55°C to +125°C

D.C. Electrical Specifications

V_{CC} = 5.0V ± 10%; T_A = 0°C to +70°C (C80C88) (C80C88-2)
V_{CC} = 5.0V ± 10%; T_A = -40°C to +85°C (I80C88) (I80C88-2)
V_{CC} = 5.0V ± 10%; T_A = -55°C to +125°C (M80C88)
V_{CC} = 5.0V ± 5%; T_A = -55°C to +125°C (M80C88-2)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	Logical One Input Voltage	2.0 2.2		V V	C80C88, I80C88 M80C88
VIL	Logical Zero Input Voltage		0.8	V	
VIHC	CLK Logical One Input Voltage	VCC -0.8V		V	
VILC	CLK Logical Zero Input Voltage		0.8	V	
VOH	Output High Voltage	3.0 VCC -0.4		V V	IOH = -2.5mA IOH = -100μA
VOL	Output Low Voltage		0.4	V	IOL = +2.5mA
II	Input Leakage Current	-1.0	1.0	μA	VIN = 0V or VCC, DIP Pins 17-19, 21-23, 33
IBHH	Input Current Bus Hold High	-40	-400	μA	VIN = 3.0V (See Note 1)
IBHL	Input current Bus Hold Low	40	400	μA	VIN = 0.8V (See Note 2)
IO	Output Leakage Current	-10.0	10.0	μA	VO = 0V or VCC DIP Pins 24, 25
ICCSB	Standby Power Supply Current		500	μA	VCC = 5.5V (See Note 3.)
ICCOP	Operating Power Supply Current		10	mA/MHz	VCC = 5.5V Freq (MHz) = CLK Cycle Time (TCLCL)

NOTES: 1. IBHH should be measured after raising VIN to VCC and then lowering to 3.0V on the following pins: 2-16, 26-32, 34-39.
2. IBHL should be measured after lowering VIN to GND and then raising to 0.8V on the following pins: 2-16, 35.
3. ICCSB tested during clock high time after HALT instruction execution. VIN = VCC or GND VCC = 5.5V outputs unloaded.

Capacitance

T_A = 25°C; VCC = GND = 0V; VIN = +5V or GND

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
CIN	Input Capacitance	20	pF	FREQ = 1MHz Unmeasured Pins Returned to GND
COUT	Output Capacitance	20	pF	T_A = 25°C
CI/O	I/O Capacitance	20	pF	V_{IN} or V_{OUT} = VCC or GND

A.C. Electrical Specifications

V_{CC} = 5.0V ± 10%; T_A = 0°C to +70°C (C80C88) (C80C88-2)
V_{CC} = 5.0V ± 10%; T_A = -40°C to +85°C (I80C88) (I80C88-2)
V_{CC} = 5.0V ± 10%; T_A = -55°C to +125°C (M80C88)
V_{CC} = 5.0V ± 5%; T_A = -55°C to +125°C (M80C88-2)

MINIMUM COMPLEXITY SYSTEM TIMING REQUIREMENTS

SYMBOL	PARAMETER	80C88-2		80C88		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
TCLCL	CLK Cycle Period	125		200		ns	
TCLCH	CLK Low Time	68		118		ns	
TCHCL	CLK High Time	44		69		ns	
TCH1CH2	CLK Rise Time		10		10	ns	From 1.0V to 3.5V
TCL2CL1	CLK Fall Time		10		10	ns	From 3.5V to 1.0V
TDVCL	Data in Setup Time	20		30		ns	
TCLDX1	Data in Hold Time	10		10		ns	
TR1VCL	RDY Setup Time into 82C84A (See Notes 1, 2)	35		35		ns	
TCLR1X	RDY Hold Time into 82C84A (See Notes 1, 2)	0		0		ns	
TRYHCH	READY Setup Time into 80C88	68		118		ns	
TCHRYX	READY Hold Time into 80C88	20		30		ns	
TRYLCL	READY Inactive to CLK (See Note 3)	−8		−8		ns	
THVCH	HOLD Setup Time	20		35		ns	
TINVCH	INTR, NMI, $\overline{\text{TEST}}$ Setup Time (See Note 2)	15		30		ns	
TILIH	Input Rise Time (Except CLK)		15		15	ns	From 0.8V to 2.0V
TIHIL	Input Fall Time (Except CLK)		15		15	ns	From 2.0V to 0.8V

A.C. Electrical Specifications V_{CC} = 5.0V ± 10%; T_A = 0°C to +70°C (C80C88) (C80C88-2)
V_{CC} = 5.0V ± 10%; T_A = -40°C to +85°C (I80C88) (I80C88-2)
V_{CC} = 5.0V ± 10%; T_A = -55°C to +125°C (M80C88)
V_{CC} = 5.0V ± 5%; T_A = -55°C to +125°C (M80C88-2)

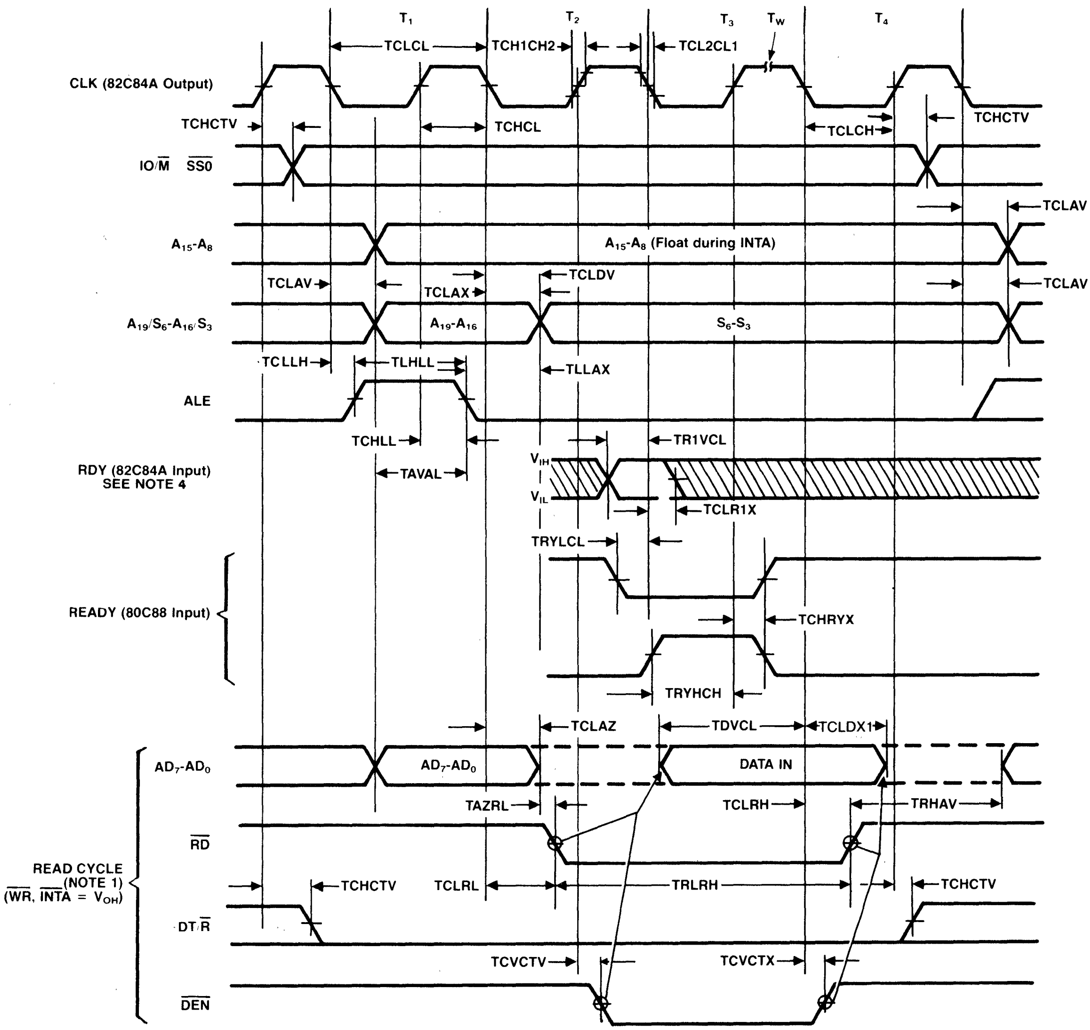
MINIMUM COMPLEXITY SYSTEM TIMING RESPONSES

SYMBOL	PARAMETER	80C88-2		80C88		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
TCLAV	Address Valid Delay	10	60	10	110	ns	
TCLAX	Address Hold Time	10		10		ns	
TCLAZ	Address Float Delay	TCLAX	50	TCLAX	80	ns	
TCHSZ	Status Float Delay		50		80	ns	
TLHLL	ALE Width	TCLCH-10		TCLCH-20		ns	
TCLLH	ALE Active Delay		50		80	ns	
TCHLL	ALE Inactive Delay		55		85	ns	
TLLAX	Address Hold Time to ALE Inactive	TCHCL-10		TCHCL-10		ns	
TCLDV	Data Valid Delay	10	60	10	110	ns	C_L = 100 pF for all 80C88 Outputs in addition to internal loads
TCLDX2	Data Hold Time	10		10		ns	
TWHDX	Data Hold Time After $\overline{WR}$	TCLCL-30		TCLCL-30		ns	
TCVCTV	Control Active Delay 1	10	70	10	110	ns	
TCHCTV	Control Active Delay 2	10	60	10	110	ns	
TCVCTX	Control Inactive Delay	10	70	10	110	ns	
TAZRL	Address Float to READ Active	0		0		ns	
TCLRL	$\overline{RD}$ Active Delay	10	100	10	165	ns	
TCLRH	$\overline{RD}$ Inactive Delay	10	80	10	150	ns	
TRHAV	$\overline{RD}$ Inactive to Next Address Active	TCLCL-40		TCLCL-45		ns	
TCLHAV	HLDA Valid Delay	10	100	10	160	ns	
TRLRH	$\overline{RD}$ Width	2TCLCL-50		2TCLCL-75		ns	
TWLWH	$\overline{WR}$ Width	2TCLCL-40		2TCLCL-60		ns	
TAVAL	Address Valid to ALE Low	TCLCH-40		TCLCH-60		ns	
TOLOH	Output Rise Time		15		15	ns	From 0.8V to 2.0V
TOHOL	Output Fall Time		15		15	ns	From 2.0V to 0.8V
TCHSV	Status Active Delay	10	60	10	110	ns	

NOTES: 1. Signal at 82C84A shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next clock.
3. Applies only to T2 state (8 nanoseconds into T3).

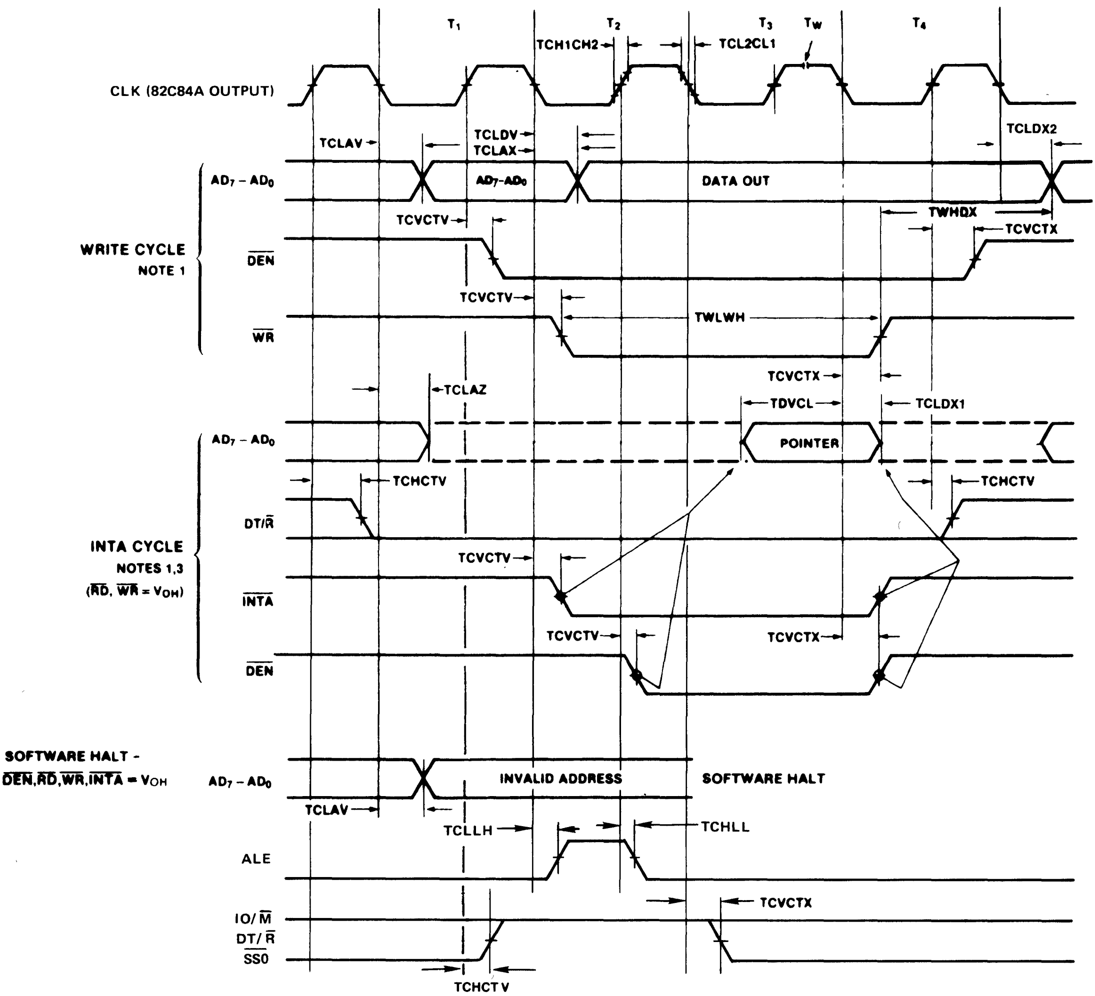
Waveforms

BUS TIMING – MINIMUM MODE SYSTEM



Waveforms

BUS TIMING — MINIMUM MODE SYSTEM



NOTES:
1. All signals switch between V_{OH} and V_{OL} unless otherwise specified.
2. RDY is sampled near the end of T_2, T_3, T_W to determine if T_W machines states are to be inserted.
3. Two INTA cycles run back-to-back. The 80C88 local ADDR/DATA bus is floating during both INTA cycles. Control Signals are shown for the second INTA cycle.
4. Signals at 82C84A are shown for reference only.
5. All timing measurements are made at 1.5V unless otherwise noted.

A.C. Electrical Specifications V_{CC} = 5.0V ± 10%; T_A = 0°C to +70°C (C80C88) (C80C88-2)
V_{CC} = 5.0V ± 10%; T_A = -40°C to +85°C (I80C88) (I80C88-2)
V_{CC} = 5.0V ± 10%; T_A = -55°C to +125°C (M80C88)
V_{CC} = 5.0V ± 5%; T_A = -55°C to +125°C (M80C88-2)

MAX MODE SYSTEM (USING 82C88 BUS CONTROLLER) TIMING REQUIREMENTS

SYMBOL	PARAMETER	80C88-2 MIN	80C88-2 MAX	80C88 MIN	80C88 MAX	UNITS	TEST CONDITIONS
TCLCL	CLK Cycle Period	125		200		ns	
TCLCH	CLK Low Time	68		118		ns	
TCHCL	CLK High Time	44		69		ns	
TCH1CH2	CLK Rise Time		10		10	ns	From 1.0V to 3.5V
TCL2CL1	CLK Fall Time		10		10	ns	From 3.5V to 1.0V
TDVCL	Data in Setup Time	20		30		ns	
TCLDX1	Data in Hold Time	10		10		ns	
TR1VCL	RDY Setup Time into 82C84 (See Notes 1, 2)	35		35		ns	
TCLR1X	RDY Hold Time into 82C84 (See Notes 1, 2)	0		0		ns	
TRYHCH	READY Setup Time into 80C88	68		118		ns	
TCHRYX	READY Hold Time into 80C88	20		30		ns	
TRYLCL	READY Inactive to CLK (See Note 3)	−8		−8		ns	
TINVCH	Setup Time for Recognition (INTR, NMI, $\overline{TEST}$) (See Note 2)	15		30		ns	
TGVCH	$\overline{RQ}/\overline{GT}$ Setup Time	15		30		ns	
TCHGX	$\overline{RQ}$ Hold Time into 80C88 (See Note 4)	30	TCHCL+10	40	TCHCL+10	ns	
TILIH	Input Rise Time (Except CLK)		15		15	ns	From 0.8V to 2.0V
TIHIL	Input Fall Time (Except CLK)		15		15	ns	From 2.0V to 0.8V

A.C. Electrical Specifications V_{CC} = 5.0V ± 10%; T_A = 0°C to +70°C (C80C88) (C80C88-2)
V_{CC} = 5.0V ± 10%; T_A = -40°C to +85°C (I80C88) (I80C88-2)
V_{CC} = 5.0V ± 10%; T_A = -55°C to +125°C (M80C88)
V_{CC} = 5.0V ± 5%; T_A = -55°C to +125°C (M80C88-2)

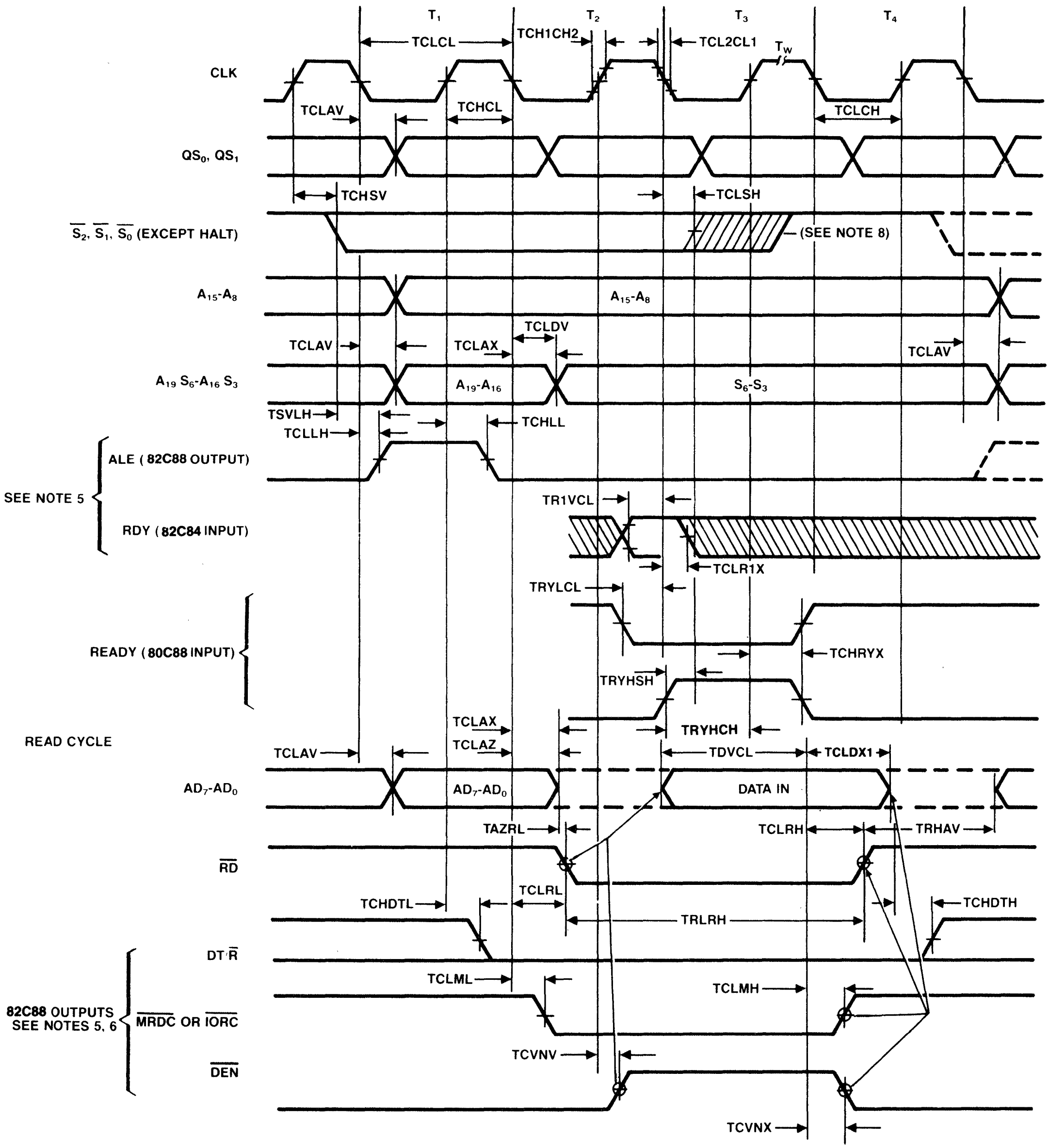
MAX MODE SYSTEM (USING 82C88 BUS CONTROLLER) TIMING RESPONSES

SYMBOL	PARAMETER	80C88-2		80C88		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
TCLML	Command Active Delay (See Note 1)	5	35	5	35	ns	
TCLMH	Command Inactive Delay (See Note 1)	5	35	5	35	ns	
TRYHSH	READY Active to Status Passive (See Notes 3, 5)		65		110	ns	
TCHSV	Status Active Delay	10	60	10	110	ns	
TCLSH	Status Inactive Delay (See Note 5)	10	130	10	130	ns	
TCLAV	Address Valid Delay	10	110	10	110	ns	
TCLAX	Address Hold Time	10		10		ns	
TCLAZ	Address Float Delay	TCLAX	80	TCLAX	80	ns	
TCHSZ	Status Float Delay		50		80	ns	
TSVLH	Status Valid to ALE High (See Note 1)		20		20	ns	
TSVMCH	Status Valid to MCE High (See Note 1)		30		30	ns	
TCLLH	CLK Low to ALE Valid (See Note 1)		20		20	ns	
TCLMCH	CLK Low to MCE High (See Note 1)		25		25	ns	
TCHLL	ALE Inactive Delay (See Note 1)	4	18	4	18	ns	
TCLMCL	MCE Inactive Delay (See Note 1)		15		15	ns	C_L = 100 pF for all 80C88 Outputs in addition to internal loads
TCLDV	Data Valid Delay	10	60	10	110	ns	
TCLDX2	Data Hold Time	10		10		ns	
TCVNV	Control Active Delay (See Note 1)	5	45	5	45	ns	
TCVNX	Control Inactive Delay (See Note 1)	10	45	10	45	ns	
TAZRL	Address Float to Read Active	0		0		ns	
TCLRL	$\overline{RD}$ Active Delay	10	100	10	165	ns	
TCLRH	$\overline{RD}$ Inactive Delay	10	80	10	150	ns	
TRHAV	$\overline{RD}$ Inactive to Next Address Active	TCLCL-40		TCLCL-45		ns	
TCHDTL	Direction Control Active Delay (See Note 1)		50		50	ns	
TCHDTH	Direction Control Inactive Delay (See Note 1)		30		30	ns	
TCLGL	$\overline{GT}$ Active Delay	10	50	10	85	ns	
TCLGH	$\overline{GT}$ Inactive Delay	10	50	10	85	ns	
TRLRH	$\overline{RD}$ Width	2TCLCL-50		2TCLCL-75		ns	
TOLOH	Output Rise Time		15		15	ns	From 0.8V to 2.0V
TOHOL	Output Fall Time		15		15	ns	From 2.0V to 0.8V

NOTES: 1. Signal at 82C84A or 82C88 shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next clock.
3. Applies only to T2 state (8 nanoseconds into T3).
4. The 80C88 actively pulls the $\overline{RQ}/\overline{GT}$ pin to a logic one on the following clock low time.
5. Status lines return to their inactive (logic one) state after CLK goes low and READY goes high.

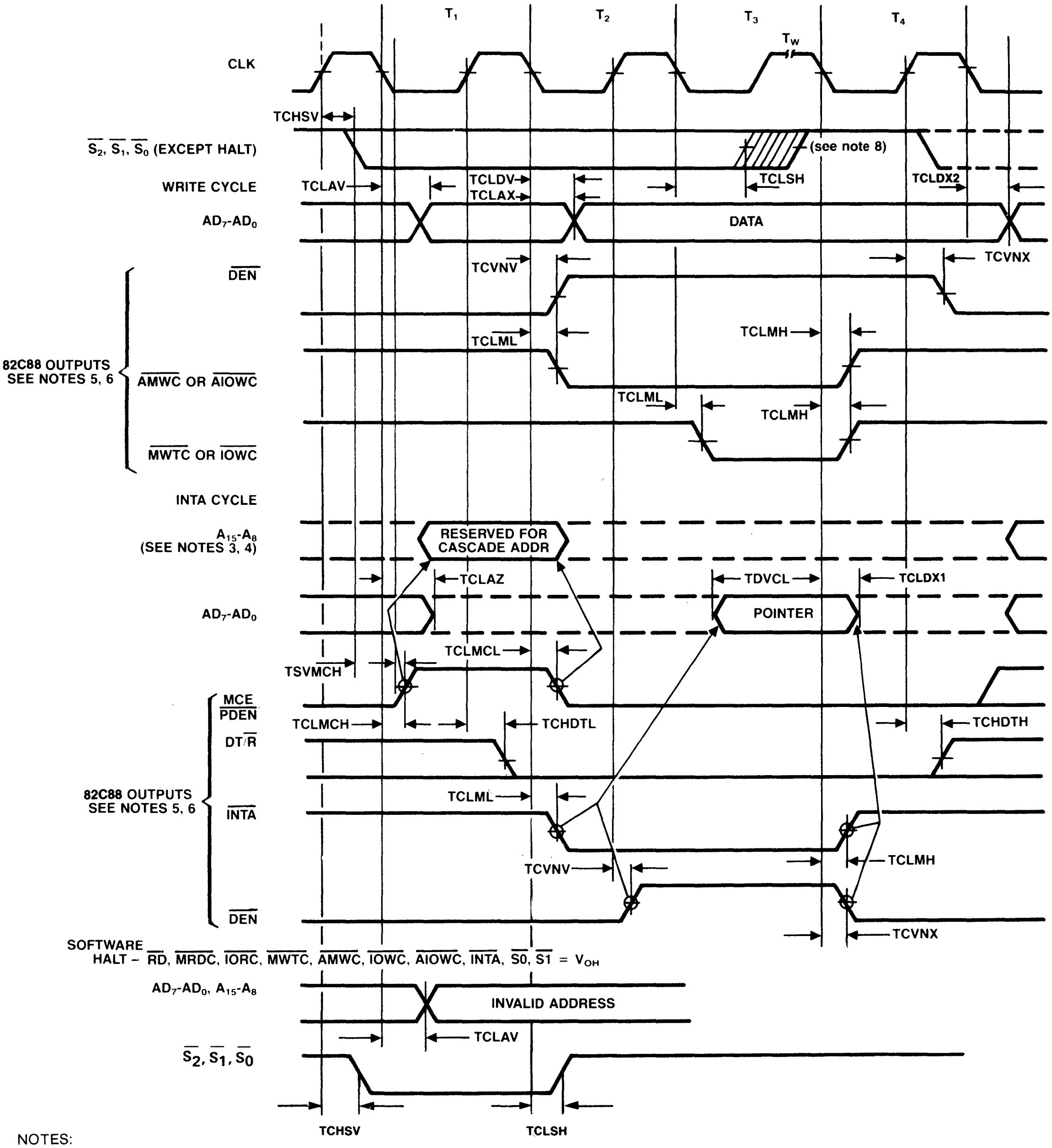
Waveforms

BUS TIMING – MAXIMUM MODE



Waveforms

BUS TIMING — MAXIMUM MODE SYSTEM (USING 82C88)

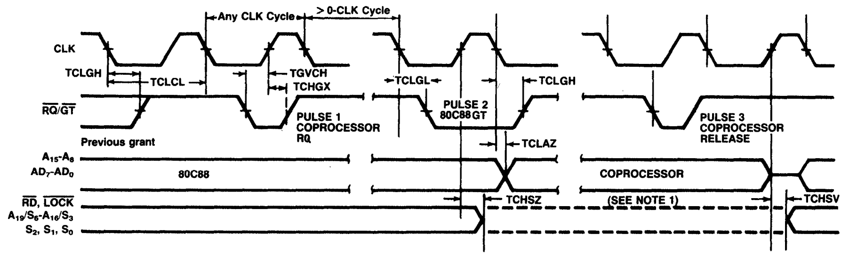


NOTES:

1. All signals switch between V_{OH} and V_{OL} unless otherwise specified.
2. RDY is sampled near the end of T_2, T_3, T_W to determine if T_W machine states are to be inserted.
3. Cascade address is valid between first and second INTA cycles.
4. Two INTA cycles run back-to-back. The 80C88 local ADDR/DATA bus is floating during both INTA cycles. Control for pointer address is shown for second INTA cycle.
5. Signals at 82C84A or 82C88 are shown for reference only.
6. The issuance of the 82C88 command and control signals (MRDC, MWTC, AMWC, IORC, IOWC, AIOWC, INTA and DEN) lags the active high 82C88 CEN.
7. All timing measurements are made at 1.5V unless otherwise noted.
8. Status inactive in state just prior to T_4.

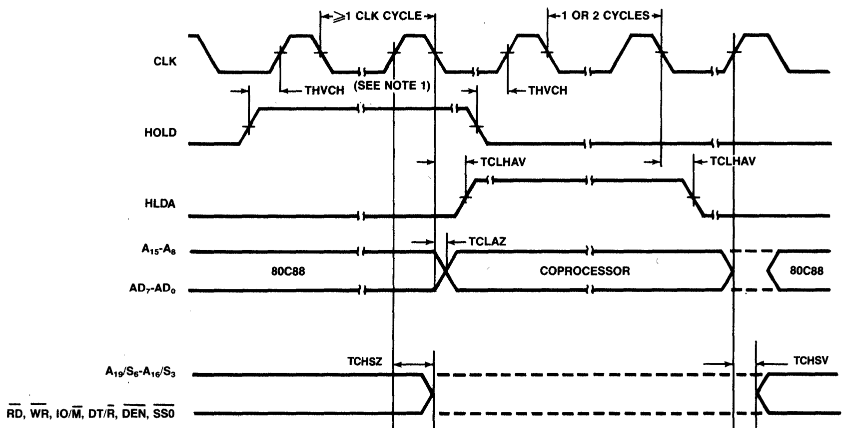
Waveforms

REQUEST/GRANT SEQUENCE TIMING (MAXIMUM MODE ONLY)



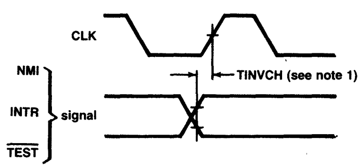
NOTE: 1. THE COPROCESSOR MAY NOT DRIVE THE BUSSES OUTSIDE THE REGION SHOWN WITHOUT RISKING CONTENTION

HOLD/HOLD ACKNOWLEDGE TIMING (MINIMUM MODE ONLY)



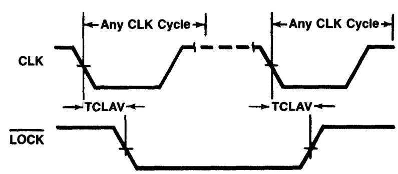
NOTE: 1. SETUP REQUIREMENTS FOR ASYNCHRONOUS SIGNALS ONLY TO GUARANTEE RECOGNITION AT NEXT CLK.

ASYNCHRONOUS SIGNAL RECOGNITION

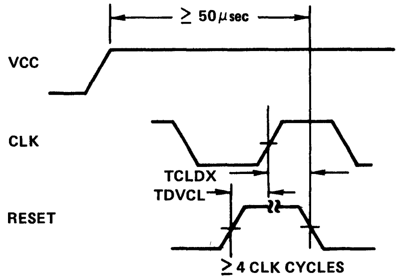


NOTE: 1. SETUP REQUIREMENTS FOR ASYNCHRONOUS SIGNALS ONLY TO GUARANTEE RECOGNITION AT NEXT CLK.

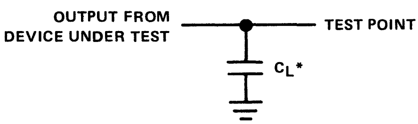
BUS LOCK SIGNAL TIMING (MAXIMUM MODE ONLY)



Reset Timing

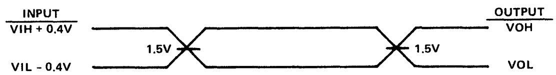


A.C. Test Circuit



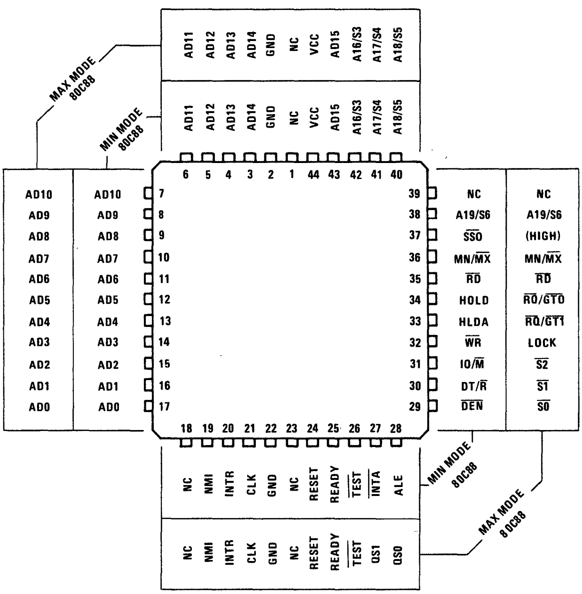
*Includes stray and jig capacitance

A.C. Testing Input, Output Waveforms



A.C. Testing: All input signals (other than CLK) must switch between VIL_{max} -0.4V and VIH_{min} +0.4V. CLK must switch between 0.4V and VCC -0.4V. Input rise and fall times are driven at 1ns/V.

LCC/PLCC Pinout



INSTRUCTION SET SUMMARY

DATA TRANSFER

MOV = **Move**:

	76543210	76543210	76543210	76543210
Register/memory to/from register	1 0 0 0 1 0 d w	mod reg r/m		
Immediate to register/memory	1 1 0 0 0 1 1 w	mod 0 0 0 r/m	data	data if w 1
Immediate to register	1 0 1 1 w reg	data	data if w 1	
Memory to accumulator	1 0 1 0 0 0 0 w	addr-low	addr-high	
Accumulator to memory	1 0 1 0 0 0 1 w	addr-low	addr-high	
Register/memory to segment register	1 0 0 0 1 1 1 0	mod 0 reg r/m		
Segment register to register/memory	1 0 0 0 1 1 0 0	mod 0 reg r/m		

PUSH = **Push**:

Register/memory	1 1 1 1 1 1 1 1	mod 1 1 0 r/m		
Register	0 1 0 1 0 reg			
Segment register	0 0 0 reg 1 1 0			

POP = **Pop**:

Register/memory	1 0 0 0 1 1 1 1	mod 0 0 0 r/m		
Register	0 1 0 1 1 reg			
Segment register	0 0 0 reg 1 1 1			

XCHG = **Exchange**:

Register/memory with register	1 0 0 0 0 1 1 w	mod reg r/m		
Register with accumulator	1 0 0 1 0 reg			

IN = Input from:

Fixed port	1 1 1 0 0 1 0 w	port		
Variable port	1 1 1 0 1 1 0 w			

OUT = Output to:

Fixed port	1 1 1 0 0 1 1 w	port		
Variable port	1 1 1 0 1 1 1 w			
XLAT = Translate byte to AL	1 1 0 1 0 1 1 1			
LEA = Load EA to register	1 0 0 0 1 1 0 1	mod reg r/m		
LDS = Load pointer to DS	1 1 0 0 0 1 0 1	mod reg r/m		
LES = Load pointer to ES	1 1 0 0 0 1 0 0	mod reg r/m		
LAHF = Load AH with flags	1 0 0 1 1 1 1 1			
SAHF = Store AH into flags	1 0 0 1 1 1 1 0			
PUSHF = Push flags	1 0 0 1 1 1 0 0			
POPF = Pop flags	1 0 0 1 1 1 0 1			

ARITHMETIC

ADD = **Add**:

Reg./memory with register to either	0 0 0 0 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 s w	mod 0 0 0 r/m	data	data if s w 01
Immediate to accumulator	0 0 0 0 0 1 0 w	data	data if w 1	

ADC = **Add with carry**:

Reg./memory with register to either	0 0 0 1 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 s w	mod 0 1 0 r/m	data	data if s w 01
Immediate to accumulator	0 0 0 1 0 1 0 w	data	data if w 1	

INC = **Increment**:

Register/memory	1 1 1 1 1 1 1 w	mod 0 0 0 r/m		
Register	0 1 0 0 0 reg			
AAA = ASCII adjust for add	0 0 1 1 0 1 1 1			
DAA = Decimal adjust for add	0 0 1 0 0 1 1 1			

SUB = **Subtract**:

Reg./memory and register to either	0 0 1 0 1 0 d w	mod reg r/m		
Immediate from register/memory	1 0 0 0 0 0 s w	mod 1 0 1 r/m	data	data if s w 01
Immediate from accumulator	0 0 1 0 1 1 0 w	data	data if w 1	

SBB = **Subtract with borrow**

Reg./memory and register to either	0 0 0 1 1 0 d w	mod reg r/m		
Immediate from register/memory	1 0 0 0 0 0 s w	mod 0 1 1 r/m	data	data if s w 01
Immediate from accumulator	0 0 0 1 1 1 0 w	data	data if w 1	

DEC **Decrement**:

	76543210	76543210	76543210	76543210
Register/memory	1 1 1 1 1 1 1 w	mod 0 0 1 r/m		
Register	0 1 0 0 1 reg			
NEG Change sign	1 1 1 1 0 1 1 w	mod 0 1 1 r/m		

CMP **Compare**:

Register/memory and register	0 0 1 1 1 0 d w	mod reg r/m		
Immediate with register/memory	1 0 0 0 0 0 s w	mod 1 1 1 r/m	data	data if s w 01
Immediate with accumulator	0 0 1 1 1 1 0 w	data	data if w 1	
AAS ASCII adjust for subtract	0 0 1 1 1 1 1 1			
DAS Decimal adjust for subtract	0 0 1 0 1 1 1 1			
MUL Multiply (unsigned)	1 1 1 1 0 1 1 w	mod 1 0 0 r/m		
IMUL Integer multiply (signed)	1 1 1 1 0 1 1 w	mod 1 0 1 r/m		
AAM ASCII adjust for multiply	1 1 0 1 0 1 0 0	0 0 0 0 1 0 1 0		
DIV Divide (unsigned)	1 1 1 1 0 1 1 w	mod 1 1 0 r/m		
IDIV Integer divide (signed)	1 1 1 1 0 1 1 w	mod 1 1 1 r/m		
AAD ASCII adjust for divide	1 1 0 1 0 1 0 1	0 0 0 0 1 0 1 0		
CBW Convert byte to word	1 0 0 1 1 0 0 0			
CWD Convert word to double word	1 0 0 1 1 0 0 1			

LOGIC

NOT Invert	1 1 1 1 0 1 1 w	mod 0 1 0 r/m		
SHL/SAL Shift logical/arithmetic left	1 1 0 1 0 0 v w	mod 1 0 0 r/m		
SHR Shift logical right	1 1 0 1 0 0 v w	mod 1 0 1 r/m		
SAR Shift arithmetic right	1 1 0 1 0 0 v w	mod 1 1 1 r/m		
ROL Rotate left	1 1 0 1 0 0 v w	mod 0 0 0 r/m		
ROR Rotate right	1 1 0 1 0 0 v w	mod 0 0 1 r/m		
RCL Rotate through carry flag left	1 1 0 1 0 0 v w	mod 0 1 0 r/m		
RCR Rotate through carry right	1 1 0 1 0 0 v w	mod 0 1 1 r/m		

AND **And**:

Reg./memory and register to either	0 0 1 0 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 0 0 r/m	data	data if w 1
Immediate to accumulator	0 0 1 0 0 1 0 w	data	data if w 1	

TEST **And function to flags, no result**:

Register/memory and register	1 0 0 0 0 1 0 w	mod reg r/m		
Immediate data and register/memory	1 1 1 1 0 1 1 w	mod 0 0 0 r/m	data	data if w 1
Immediate data and accumulator	1 0 1 0 1 0 0 w	data	data if w 1	

OR **Or**:

Reg./memory and register to either	0 0 0 0 1 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 0 0 1 r/m	data	data if w 1
Immediate to accumulator	0 0 0 0 1 1 0 w	data	data if w 1	

XOR **Exclusive or**:

Reg./memory and register to either	0 0 1 1 0 0 d w	mod reg r/m		
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 1 0 r/m	data	data if w 1
Immediate to accumulator	0 0 1 1 0 1 0 w	data	data if w 1	

STRING MANIPULATION

REP = Repeat	1 1 1 1 0 0 1 z			
MOVS = Move byte/word	1 0 1 0 0 1 0 w			
CMPS = Compare byte/word	1 0 1 0 0 1 1 w			
SCAS = Scan byte/word	1 0 1 0 1 1 1 w			
LODS = Load byte/wd to AL/AX	1 0 1 0 1 1 0 w			
STOS = Stor byte/wd from AL/A	1 0 1 0 1 0 1 w			

INSTRUCTION SET SUMMARY

CONTROL TRANSFER

CALL = Call:

	76543210	76543210	76543210
Direct within segment	11101000	disp-low	disp-high
Indirect within segment	11111111	mod 0 1 0 r/m	
Direct intersegment	10011010	offset-low	offset-high
		seg-low	seg-high
Indirect intersegment	11111111	mod 0 1 1 r/m	

JMP = Unconditional Jump:

	76543210	76543210	76543210
Direct within segment	11101001	disp-low	disp-high
Direct within segment-short	11101011	disp	
Indirect within segment	11111111	mod 1 0 0 r/m	
Direct intersegment	11101010	offset-low	offset-high
		seg-low	seg-high
Indirect intersegment	11111111	mod 1 0 1 r/m	

RET = Return from CALL:

	76543210	76543210	76543210
Within segment	11000011		
Within seg adding immed to SP	11000010	data-low	data-high
Intersegment	11001011		
Intersegment adding immediate to SP	11001010	data-low	data-high
JE/JZ = Jump on equal/zero	01110100	disp	
JL/JNGE = Jump on less/not greater or equal	01111100	disp	
JLE/JNG = Jump on less or equal/not greater	01111110	disp	
JB/JNAE = Jump on below/not above or equal	01110010	disp	
JBE/JNA = Jump on below or equal/not above	01110110	disp	
JP/JPE = Jump on parity/parity even	01111010	disp	
JO = Jump on overflow	01110000	disp	
JS = Jump on sign	01111000	disp	
JNE/JNZ = Jump on not equal/not zero	01110101	disp	
JNL/JGE = Jump on not less/greater or equal	01111101	disp	
JNLE/JG = Jump on not less or equal/greater	01111111	disp	

	76543210	76543210
JNB/JAE Jump on not below/above or equal	01110011	disp
JNBE/JA Jump on not below or equal/above	01110111	disp
JNP/JPO Jump on not par/par odd	01111011	disp
JNO Jump on not overflow	01110001	disp
JNS Jump on not sign	01111001	disp
LOOP Loop CX times	11100010	disp
LOOPZ/LOOPE Loop while zero/equal	11100001	disp
LOOPNZ/LOOPNE Loop while not zero/equal	11100000	disp
JCXZ Jump on CX zero	11100011	disp

INT Interrupt

	76543210	76543210
Type specified	11001101	type
Type 3	11001100	
INTO Interrupt on overflow	11001110	
IRET Interrupt return	11001111	

PROCESSOR CONTROL

	76543210	76543210
CLC Clear carry	11111000	
CMC Complement carry	11110101	
STC Set carry	11111001	
CLD Clear direction	11111100	
STD Set direction	11111101	
CLI Clear interrupt	11111010	
STI Set interrupt	11111011	
HLT Halt	11110100	
WAIT Wait	10011011	
ESC Escape (to external device)	11011 x x x	mod x x x r/m
LOCK Bus lock prefix	11110000	

Footnotes:

AL = 8-bit accumulator
AX = 16-bit accumulator
CX = Count register
DS = Data segment
ES = Extra segment
Above/below refers to unsigned value
Greater = more positive;
Less = less positive (more negative) signed values
if d = 1 then "to" reg; if d = 0 then "from" reg
if w = 1 then word instruction; if w = 0 then byte instruction

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low

if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP
DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.

if s:w = 01 then 16 bits of immediate data form the operand.
if s:w = 11 then an immediate data byte is sign extended to form the 16-bit operand.
if v = 0 then "count" = 1; if v = 1 then "count" in (CL)
x = don't care
z is used for string primitives for comparison with ZF FLAG.

SEGMENT OVERRIDE PREFIX

0 0 1 reg 1 1 0

REG is assigned according to the following table.

16-Bit (w = 1)	8-Bit (w = 0)	Segment
000 AX	000 AL	00 ES
001 CX	001 CL	01 CS
010 DX	010 DL	10 SS
011 BX	011 BL	11 DS
100 SP	100 AH	
101 BP	101 CH	
110 SI	110 DH	
111 DI	111 BH	

Instructions which reference the flag register file as a 16-bit object use the symbol FLAGS to represent the file:

FLAGS = X:X:X:X:(OF):(DF):(IF):(TF):(SF):(ZF):X:(AF):X:(PF):X:(CF)

82C37A

CMOS High Performance Programmable DMA Controller

Features

- Compatible with the NMOS 8237A
- Four Independent Maskable Channels with Autoinitialization Capability
- Expandable to any Number of Channels
- Memory-to-memory Transfers
- Static CMOS Design Permits Low Power Operation
  - ▸ ICCOP = 2 mA/MHz Maximum
  - ▸ ICCSB = 10 μA Maximum
- Fully TTL/CMOS Compatible
- High Speed Data Transfers up to 4 MBytes/sec with 8 MHz Clock
- Upgraded Capabilities Allow Software Read of Internal Registers

Description

The 82C37A is an enhanced version of the industry standard 8237A (DMA) Direct Memory Access) controller, fabricated using Harris' advanced SAJI (self aligned junction isolated) CMOS process. Pin compatible with NMOS designs, the 82C37A offers increased functionality, improved performance, and dramatically reduced power consumption. The fully static design permits gated clock operation for even further reduction of power.

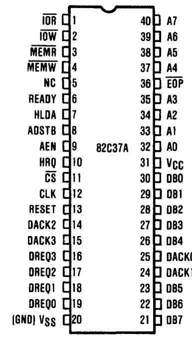
The 82C37A controller can improve system performance by allowing external devices to transfer data directly to or from system memory. Memory-to-memory transfer capability is also provided, along with a memory block initialization feature. DMA requests may be generated by either hardware or software, and each channel is independently programmable with a variety of features for flexible operation.

The 82C37A is designed to be used with an external address latch, such as the 82C82 CMOS to demultiplex the most significant 8 bits. The 82C37A can be used with industry standard microprocessors such as 80C86, 80C88, 8088, 8085, 8086, Z80, NSC800, 80186 and others.

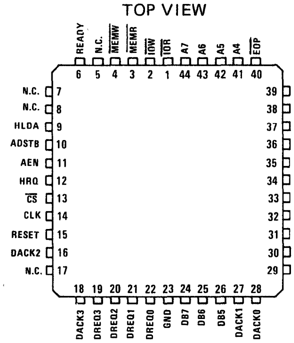
Multimode programmability allows the user to select from three basic types of DMA services, and reconfiguration under program control is possible even with the clock to the controller stopped. Each channel has a full 64K address and word count range, and may be programmed to autoinitialize these registers following DMA termination (end of process).

Pinouts

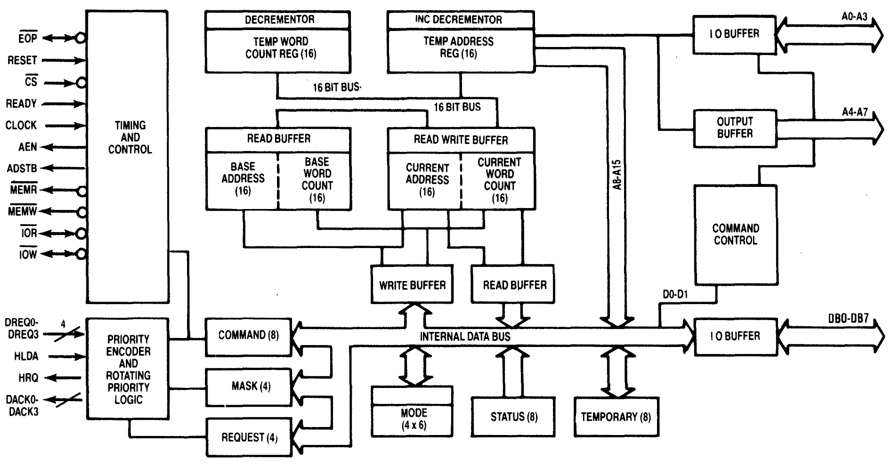
TOP VIEW



LCC/PLCC
TOP VIEW



Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Pin Description

TABLE 1.

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
VCC	31		VCC: is the +5V power supply pin. A 0.1μF capacitor between pins 31 and 20 is recommended for decoupling.
GND	20		Ground
CLK	12	I	CLOCK INPUT: The Clock Input is used to generate the timing signals which control 82C37A operations. This input may be driven from DC to 8MHz for the 82C37A, or from DC to 5 MHz for the 82C37A-5. The Clock may be stopped in either state for standby operation.
$\overline{\text{CS}}$	11	I	CHIP SELECT: Chip Select is an active low input used to enable the controller onto the data bus for CPU communications.
RESET	13	I	RESET: This is an active high input which clears the command, status, request, and temporary registers, the first/last flip-flop, and the mode register counter. The mask register is set to ignore requests. Following a Reset, the controller is in an idle cycle.
READY	6	I	READY: This signal can be used to extend the memory read and write pulses from the 82C37A to accommodate slow memories or I/O devices. Ready must not make transitions during its specified set-up and hold times. Ready is ignored in verify transfer mode.
HLDA	7	I	HOLD ACKNOWLEDGE: The active high Hold Acknowledge from the CPU indicates that it has relinquished control of the system busses.
DREQ0-DREQ3	16-19	I	DMA REQUEST: The DMA Request (DREQ) lines are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service. In Fixed Priority, DREQ0 has the highest priority and DREQ3 has the lowest priority. A request is generated by activating the DREQ line of a channel. DACK will acknowledge the recognition of DREQ signal. Polarity of DREQ is programmable. Reset initializes these lines to active high. DREQ must be maintained until the corresponding DACK goes active. DREQ will not be recognized while the clock is stopped. Unused DREQ inputs should be pulled High or Low (inactive) and the corresponding mask bit set.
DB0-DB7	21-23 26-30	I/O	DATA BUS: The Data Bus lines are bidirectional three-state signals connected to the system data bus. The outputs are enabled in the Program condition during the I/O Read to output the contents of a register to the CPU. The outputs are disabled and the inputs are read during an I/O Write cycle when the CPU is programming the 82C37A control registers. During DMA cycles, the most significant 8 bits of the address are output onto the data bus to be strobed into an external latch by ADSTB. In memory-to-memory operations, data from the memory enters 82C37A on the data bus during the read-from-memory transfer, then during the write-to-memory transfer, the data bus outputs write the data into the new memory location.
$\overline{\text{IOR}}$	1	I/O	I/O READ: I/O Read is a bidirectional active low three-state line. In the Idle cycle, it is an input control signal used by the CPU to read the control registers. In the Active cycle, it is an output control signal used by the 82C37A to access data from a peripheral during a DMA Write transfer.
$\overline{\text{IOW}}$	2	I/O	I/O WRITE: I/O Write is a bidirectional active low three-state line. In the Idle cycle, it is an input control signal used by the CPU to load information into the 82C37A. In the Active cycle, it is an output control signal used by the 82C37A to load data to the peripheral during a DMA Read transfer.

Pin Description

TABLE 1.

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
$\overline{EOP}$	36	I/O	END OF PROCESS: End of Process ($\overline{EOP}$) is an active low bidirectional signal. Information concerning the completion of DMA services is available at the bidirectional $\overline{EOP}$ pin. The 82C37A allows an external signal to terminate an active DMA service by pulling the $\overline{EOP}$ pin low. A pulse is generated by the 82C37A when terminal count (TC) for any channel is reached, except for channel 0 in memory-to-memory mode. During memory-to-memory transfers, $\overline{EOP}$ will be output when the TC for channel 1 occurs. The $\overline{EOP}$ pin is driven by an open drain transistor on-chip, and requires an external pull-up resistor. When an $\overline{EOP}$ pulse occurs, whether internally or externally generated, the 82C37A will terminate the service, and if autoinitialize is enabled, the base registers will be written to the current registers of that channel. The mask bit and TC bit in the status word will be set for the currently active channel by $\overline{EOP}$ unless the channel is programmed for autoinitialize. In that case,the mask bit remains clear.
A0-A3	32-35	I/O	Address: The four least significant address lines are bidirectional three-state signals. In the Idle cycle, they are inputs and are used by the 82C37A to address the control register to be loaded or read. In the Active cycle, they are outputs and provide the lower 4 bits of the output address.
A4-A7	37-40	O	Address: The four most significant address lines are three-state outputs and provide 4 bits of address. These lines are enabled only during the DMA service.
HRQ	10	O	Hold Request: The Hold Request (HRQ) output is used to request control of the system bus. When a DREQ occurs and the corresponding mask bit is clear, or a software DMA request is made, the 82C37A issues HRQ. The HLDA signal then informs the controller when access to the system busses is permitted. For stand-alone operation where the 82C37A always controls the busses, HRQ may be tied to HLDA. This will result in one S0 state before the transfer.
DACK0- DACK 3	14,15 24,25	O	DMA Acknowledge: DMA acknowledge is used to notify the individual peripherals when one has been granted a DMA cycle. The sense of these lines is programmable. Reset initializes them to active low.
AEN	9	O	Address Enable: Address Enable enables the 8-bit latch containing the upper 8 address bits onto the system address bus. AEN can also be used to disable other system bus drivers during DMA transfers. AEN is active HIGH.
ADSTB	8	O	Address Strobe: This is an active high signal used to control latching of the upper address byte. It will drive directly the strobe input of external transparent octal latches, such as the 82C82. During block operations, ADSTB will only be issued when the upper address byte must be updated, thus speeding operation through elimination of S1 states.
$\overline{MEMR}$	3	O	Memory Read: The memory Read signal is an active low three-state output used to access data from the selected memory location during a DMA Read or a memory-to-memory transfer.
$\overline{MEMW}$	4	O	Memory Write: The Memory Write is an active low three-state output used to write data to the selected memory location during a DMA Write or a memory-to-memory transfer.
NC	5		No connect. Pin 5 is open and should not be tested for continuity.

Functional Description

The 82C37A direct memory access controller is designed to improve the data transfer rate in systems which must transfer data from an I/O device to memory, or move a block memory to an I/O device. It will also perform memory-to-memory block moves, or fill a block of memory with data from a single location. Operating modes are provided to handle single byte transfers a well as discontinuous data streams, which allows the 82C37A to control data movement with software transparency.

The DMA controller is a state-driven address and control signal generator, which permits data to be transferred directly from an I/O device to memory or vice versa without ever being stored in a temporary register. This can greatly increase the data transfer rate for sequential operations, compared with processor move or repeated string instructions. Memory-to-memory operations require temporary internal storage of the data byte between generation of the source and destination addresses, so memory-to-memory transfers take place at less than half the rate of I/O operations, but still much faster than with central processor techniques. The maximum data transfer rate obtainable with the 82C37A is approximately 4 Mbytes/second, for an I/O operation using the compressed timing option and 8 MHz clock.

The block diagram of the 82C37A is shown on page 1. The timing and control block, priority block, and internal registers are the main components. Figure 1 lists the name and size of the internal registers. The timing and control block derives internal timing from the clock input, and generates external control signals. The Priority Encoder block resolves priority contention between DMA channels requesting service simultaneously.

NAME	SIZE	NUMBER
Base Address Registers	16 Bits	4
Base Word Count Registers	16 Bits	4
Current Address Registers	16 bits	4
Current Word Count Registers	16 bits	4
Temporary Address Register	16 bits	1
Temporary Word Count Register	16 bits	1
Status Register	8 bits	1
Command Register	8 bits	1
Temporary Register	8 bits	1
Mode Registers	6 bits	4
Mask Registers	4 bits	1
Request Register	4 bits	1

FIGURE 1. 82C37A INTERNAL REGISTERS

DMA Operation

In a system, the 82C37A address and control outputs and data bus pins are basically connected in parallel with the system busses. An external latch is required for the upper address byte. While inactive, the controller's outputs are in a high impedence state. When activated by a DMA request and bus control is relinquished by the host, the 82C37A drives the busses and generates the control signals to perform the data transfer. The operation performed by activating one of the four DMA request inputs has previously been programmed into the controller via the command, mode, address, and word count registers.

For example, if a block of data is to be transferred from RAM to an I/O device, the starting address of the data is loaded into the 82C37A current and base address registers for a particular channel, and the length of the block is loaded into that channel's word count register. The corresponding mode register is programmed for a memory-to-I/O operation (read transfer), and various options are selected by the command register and other mode register bits. The channel's mask bit is cleared to enable recognition of a DMA request (DREQ). The DREQ can either be a hardware signal or a software command.

Once initiated, the block DMA transfer will proceed as the controller outputs the data address, simultaneous $\overline{MEMR}$ and $\overline{IOW}$ pulses, and selects an I/O device via the DMA acknowledge (DACK) outputs. The data byte flows directly from the RAM to the I/O device. After each byte is transferred, the address is automatically incremented (or decremented) and the word count is decremented. The operation is then repeated for the next byte. The controller stops transferring data when the word count register underflows, or an external $\overline{EOP}$ is applied.

To further understand 82C37A operation, the states generated by each clock cycle must be considered. The DMA controller operates in two major cycles, active and idle. After being programmed, the controller is normally idle until a DMA request occurs on an unmasked channel, or a software request is given. The 82C37A will then request control of the system busses and enter the active cycle. The active cycle is composed of several internal states, depending on what options have been selected and what type of operation has been requested.

The 82C37A can assume seven separate states, each composed of one full clock period. State I (SI) is the idle state. It is entered when the 82C37A has no valid DMA requests pending, at the end of a transfer sequence, or when a Reset or Master Clear has occurred. While in SI, the DMA controller is inactive but may be in the Program Condition (being programmed by the processor.)

State 0 (S0) is the first state of a DMA service. The 82C37A has requested a hold but the processor has not yet returned an acknowledge. The 82C37A may still be programmed until it has received HLDA from the CPU. An acknowledge from the CPU will signal that DMA transfers may begin. S1, S2, S3 and S4 are the working states of the DMA service. If more time is needed to complete a transfer than is available with normal timing, wait states (SW) can be inserted between S2 or S3 and S4 by the use of the Ready line on the 82C37A.

Note that the data is transferred directly from the I/O device to memory (or vice versa) with $\overline{IOR}$ and $\overline{MEMW}$ (or $\overline{MEMR}$ and $\overline{IOW}$) being active at the same time. The data is not read into or driven out of the 82C37A in I/O-to-memory or memory-to-I/O DMA transfers.

Memory-to-memory transfers require a read-from and a write-to-memory to complete each transfer. The states, which resemble the normal working states, use two-digit numbers for identification. Eight states are required for a single transfer. The first four states (S11, S12, S13, S14 are used for the read-from-memory half and the last four states (S21, S22, S23, S24) for the write-to-memory half of the transfer.

Idle Cycle

When no channel is requesting service, the 82C37A will enter the Idle cycle and perform "SI" states. In this cycle, the 82C37A will sample the DREQ lines on the falling edge of every clock cycle to determine if any channel is requesting a DMA service.

Note that for standby operation where the clock has been stopped, DMA requests will be ignored. The device will respond to $\overline{CS}$ (chip select), in case of an attempt by the microprocessor to write or read the internal registers of the 82C37A. When $\overline{CS}$ is low and HLDA is low, the 82C37A enters the Program Condition. The CPU can now establish, change or inspect the internal definition of the part by reading from or writing to the internal registers.

The 82C37A may be programmed with the clock stopped, provided that HLDA is low and at least one rising clock edge has occurred after HLDA was driven low, so the controller is in an SI state. Address lines A0-A3 are inputs to the device and select which registers will be read or written. The $\overline{IOR}$ and $\overline{IOW}$ lines are used to select and time the read or write operations. Due to the number and size of the internal registers, an internal flip-flop is used to generate an additional bit of address. The bit is used to determine the upper or lower byte of the 16-bit Address and Word Count registers. The flip-flop is reset by Master Clear or Reset. Separate software commands can also set or reset this flip-flop.

Special software commands can be executed by the 82C37A in the Program Condition. These commands are decoded as sets of addresses with $\overline{CS}$, $\overline{IOR}$, and $\overline{IOW}$. The commands do not make use of the data bus. Instructions include Set and Clear First/Last Flip-Flop, Master Clear, Clear Mode Register Counter, and Clear Mask Register.

Active Cycle

When the 82C37A is in the Idle cycle, and a software request or an unmasked channel requests a DMA service, the device will output an HRQ to the microprocessor and enter the Active cycle. It is in this cycle that the DMA service will take place, in one of four modes:

Single Transfer Mode - In single transfer Mode, the device is programmed to make one transfer only. The word count will be decremented and the address decremented or incremented following each transfer. When the word count "rolls over" from zero to FFFFH, a terminal count bit in the status register is set, an $\overline{EOP}$ pulse is generated, and the channel will autoinitialize if this option has been selected. If not programmed to autoinitialize, the mask bit will be set, along with the TC bit and $\overline{EOP}$ pulse.

DREQ must be held active until DACK becomes active. If DREQ is held active throughout the single transfer, HRQ will go inactive and release the bus to the system. It will again go active and, upon receipt of a new HLDA, another single transfer will be performed, unless a higher priority channel takes over. In 8080A, 8085A, 80C88, or 80C86 systems, this will ensure one full machine cycle execution between DMA transfers. Details of timing between the 82C37A and other bus control protocols will depend upon the characteristics of the microprocessor involved.

Block Transfer Mode — In Block Transfer mode, the device is activated by DREQ or software request and continues making transfers during the service until a TC, caused by word count going to FFFFH, or an external End of Process ($\overline{EOP}$) is encountered. DREQ need only be held active until DACK becomes active. Again, an Autoinitialization will occur at the end of the service if the channel has been programmed for that option.

Demand Transfer Mode — In Demand Transfer mode the device continues making transfers until a TC or external $\overline{EOP}$ is encountered, or until DREQ goes inactive. Thus, transfers may continue until the I/O device has exhausted its data capacity. After the I/O device has had a chance to catch up, the DMA service is reestablished by means of a DREQ. During the time between services when the microprocessor is allowed to operate, the intermediate values of address and word count are stored in the 82C37A Current Address and Current Word Count registers. Higher priority channels may intervene in the demand process, once DREQ has gone inactive. Only an $\overline{EOP}$ can cause an Autoinitialization at the end of the service. $\overline{EOP}$ is generated either by TC or by an external signal.

Cascade Mode — This mode is used to cascade more than one 82C37A for simple system expansion. The HRQ and HLDA signals from the additional 82C37A are connected to the DREQ and DACK signals respectively of a channel for the initial 82C37A. This allows the DMA requests of the additional device to propagate through the priority network circuitry of the preceding device. The priority chain is preserved and the new device must wait for its turn to acknowledge requests. Since the cascade channel of the initial 82C37A is used only for prioritizing the additional device, it does not output an address or control signals of its own. These could conflict with the outputs of the active channel in the added device. The 82C37A will respond to DREQ and generate DACK but all other outputs except HRQ will be disabled. An external $\overline{EOP}$ will be ignored by the initial device, but will have the usual effect on the added device.

Figure 2 shows two additional devices cascaded with an initial device using two of the previous channels. This forms a two-level DMA system. More 82C37As could be added at the second level by using the remaining channels of the first level. Additional devices can also be added by cascading into the channels of the second level devices, forming a third level.

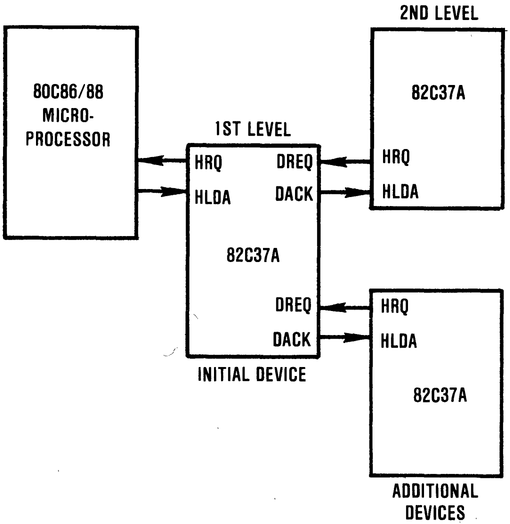


FIGURE 2. CASCADED 82C37As

When programming cascaded controllers, start with the first level (closest to the microprocessor). After RESET, the DACK outputs are programmed to be active low and are held in the high state. If they are used to drive HLDA directly, the second level device(s) cannot be programmed until DACK polarity is selected as active high on the initial device. Also, the initial device's mask bits function normally on cascaded channels, so they may be used to inhibit second-level services.

Transfer Types

Each of the three active transfer modes can perform three different types of transfers. These are Read, Write and Verify. Write transfers move data from an I/O device to the memory by activating $\overline{MEMW}$ and $\overline{IOR}$. Read transfers move data from memory to an I/O device by activating $\overline{MEMR}$ and $\overline{IOW}$.

Verify transfers are pseudo-transfers. The 82C37A operates as in Read or Write transfers generating addresses and responding to $\overline{EOP}$, etc., however the memory and I/O control lines all remain inactive. Verify mode is not permitted for memory-to-memory operation. Ready is ignored during verify transfers.

Autoinitialize — By programming a bit in the mode register, a channel may be set up as an Autoinitialize channel. During Autoinitialization, the original values of the Current Address and Current Word Count registers are automatically restored from the Base Address and Base Word count registers of that channel following $\overline{EOP}$. The base registers are loaded simultaneously with the current registers by the microprocessor and remain unchanged throughout the DMA service. The mask bit is not set when the channel is in Autoinitialize. Following Autoinitialization, the channel is ready to perform another DMA service, without CPU intervention, as soon as a valid DREQ is detected, or software request is made.

Memory-to-Memory — To perform block moves of data from one memory address space to another with minimum of program effort and time, the 82C37A includes a memory-to-memory transfer feature. Programming a bit in the Command register selects channels 0 and 1 to operate as memory-to-memory transfer channels.

The transfer is initiated by setting the software or hardware DREQ for channel 0. The 82C37A requests a DMA service in the normal manner. After HLDA is true, the device, using four-state transfers in Block Transfer mode, reads data from the memory. The channel 0 Current Address register is the source for the address used and is decremented or incremented in the normal manner. The data byte read from the memory is stored in the 82C37A internal Temporary register. Another four-state transfer moves the data to memory using the address in channel one's Current Address register and incrementing or decrementing it in the normal manner. The channel 1 Current Word Count is decremented.

When the word count of channel 1 goes to FFFFH, a TC is generated causing an $\overline{EOP}$ output terminating the service. Channel 0 word count decrementing to FFFFH will not set the channel 0 TC bit in the status register or generate an $\overline{EOP}$ in this mode. It will cause an autoinitialization of channel 0, if that option has been selected.

If full Autoinitialization for a memory-to-memory operation is desired, the channel 0 and channel 1 word counts must be set equal before the transfer begins. Otherwise, if channel 0 underflows before channel 1, it will autoinitialize and set the data source address back to the beginning of the block. If the channel 1 word count underflows before channel 0, the memory-to-memory DMA service will terminate, and channel 1 will autoinitialize but channel 0 will not.

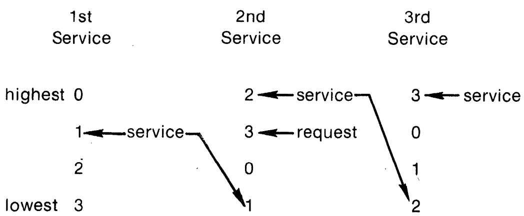
In memory-to-memory mode, Channel 0 may be programmed to retain the same address for all transfers. This allows a single byte to be written to a block of memory. This channel 0 address hold feature is selected by bit 1 in the command register.

The 82C37A will respond to external $\overline{EOP}$ signals during memory-to-memory transfers, but will only relinquish the system busses after the transfer is complete (i.e., after an S24 state). Data comparators in block search schemes may use this input to terminate the service when a match is found. The timing of memory-to-memory transfers is found in Figure 9. Memory-to-memory operations can be detected as an active AEN with no DACK outputs.

Priority — The 82C37A has two types of priority encoding available as software selectable options. The first is Fixed Priority which fixes the channels in priority order based upon the descending value of their numbers. The channel with the lowest priority is 3 followed by 2, 1 and the highest priority channel, 0. After the recognition of any one channel for service, the other channels are prevented from interferring with the service until it is completed.

The second scheme is Rotating Priority. The last channel to get service becomes the lowest priority channel with the others rotating accordingly. The next lower channel from the channel serviced has highest priority on the following request: Priority rotates every time control of the system busses is returned to the processor.

Rotating Priority



With Rotating Priority in a single chip DMA system, any device requesting service is guaranteed to be recognized after no more than three higher priority services have occurred. This prevents any one channel from monopolizing the system.

Regardless of which priority scheme is chosen, priority is evaluated every time a HLDA is returned to the 82C37A.

Compressed Timing — In order to achieve even greater throughput where system characteristics permit, the 82C37A can compress the transfer time to two clock cycles. From Figure 8 it can be seen that state S3 is used to extend the access time of the read pulse. By removing state S3, the read pulse width is made equal to the write pulse width and a transfer consists only of state S2 to change the address and state S4 to perform the read/write. S1 states will still occur when A8-A15 need updating (see Address Generation). Timing for compressed transfers is found in Figure 11. $\overline{\text{EOP}}$ will be output in S2 if compressed timing is selected. Compressed timing is not allowed for memory-to-memory transfers.

Address Generation — In order to reduce pin count, the 82C37A multiplexes the eight higher order address bits on the data lines. State S1 is used to output the higher order address bits to an external latch from which they may be placed on the address bus. The falling edge of Address Strobe (ADSTB) is used to load these bits from the data lines to the latch. Address Enable (AEN) is used to enable the bits onto the address bus through a three-state enable. The lower order address bits are output by the 82C37A directly. Lines A0-A7 should be connected to the address bus. Figure 8 shows the time relationships between CLK, AEN, ADSTB, DB0-DB7 and A0-A7.

During Block and Demand Transfer mode service, which include multiple transfers, the addresses generated will be sequential. For many transfers the data held in the external address latch will remain the same. This data need only change when a carry or borrow from A7 to A8 takes place in the normal sequence of addresses. To save time and speed transfers, the 82C37A executes S1 states only when updating of A8-A15 in the latch is necessary. This means for long services, S1 states and Address Strobes may ocur only once every 256 transfers, a savings of 255 clock cycles for each 256 transfers.

Programming

The 82C37A will accept programming from the host processor anytime that HLDA is inactive, and at least one rising clock edge has occurred after HLDA went low. It is the responsibility of the host processor to assure that programming and HLDA are mutually exclusive.

Note that a problem can occur if a DMA request occurs on an unmasked channel while the 82C37A is being programmed. For instance, the CPU may be starting to reprogram the two byte address register of channel 1 when channel 1 receives a DMA request. If the 82C37A is enabled (bit 2 in the command register is 0), and channel 1 is unmasked, a DMA service will occur after only one byte of the Address register has been reprogrammed. This condition can be avoided by disabling the controller (setting bit 2 in the command register) or masking the channel before programming any of its registers. Once the programming is complete, the controller can be enabled/unmasked.

After power-up it is suggested that all internal locations be loaded with some known value, even if some channels are unused. This will aid in debugging.

Register Description

Current Address Register — Each channel has a 16-bit Current Address register. This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented after each transfer and the values of the address are stored in the Current Address register during the transfer. This register is written or read by the microprocessor in successive 8-bit bytes. It may also be reinitialized by an Autoinitialize back to its original value. Autoinitialize takes place only after an $\overline{\text{EOP}}$. In memory-to-memory mode, the channel 0 current address register can be prevented from incrementing or decrementing by setting the address hold bit in the command register.

Current Word Register — Each channel has a 16-Bit Current Word Count register. This register determines the number of transfers to be performed. The actual number of transfers will be one more than the number programmed in the Current Word Count register (i.e., programming a count of 100 will result in 101 transfers). The word count is decremented after each transfer. When the value in the register goes from zero to FFFFH, a TC will be generated. This register is loaded or read in successive 8-bit bytes by the microprocessor in the Program Condition. Following the end of a DMA service it may also be reinitialized by an Autinitialization back to its original value. Autoinitialization can occur only when an $\overline{EOP}$ occurs. If it is not Autoinitialized, this register will have a count of FFFFH after TC.

Base Address and Base Word Count Registers — Each channel has a pair of Base Address and Base Word Count registers. These 16-bit registers store the original value of their associated current registers. During Autoinitialize these values are used to restore the current registers to their original values. The base registers are written simultaneously with their corresponding current register in 8-bit bytes in the Program Condition by the microprocessor. These registers cannot be read by the microprocessor.

Command Register — This 8-bit register controls the operation of the 82C37A. It is programmed by the microprocessor and is cleared by Reset or a Master Clear instruction. The following table lists the function of the command bits. See Figure 3 for Read and Write addresses.

Command Register

Bit Number: 7 6 5 4 3 2 1 0

0	0	Memory-to-memory disable
	1	Memory-to-memory enable
1	0	Channel 0 address hold disable
	1	Channel 0 address hold enable
	X	If bit 0 = 0
2	0	Controller enable
	1	Controller disable
3	0	Normal timing
	1	Compressed timing
	X	If bit 0 = 1
4	0	Fixed priority
	1	Rotating priority
5	0	Late write selection
	1	Extended write selection
	X	If bit 3 = 1
6	0	DREQ sense active high
	1	DREQ sense active low
7	0	DACK sense active low
	1	DACK sense active high

Mode Register — Each channel has a 6-bit mode register associated with it. When the register is being written to by the microprocessor in the Program Condition, bits 0 and 1 determine which channel Mode register is to be written. When the processor reads a mode register, bits 0 and 1 will both be ones. See the following table and Figure 3 for mode register functions and addresses.

Mode Register

Bit Number: 7 6 5 4 3 2 1 0

1, 0	00	Channel 0 select
	01	Channel 1 select
	10	Channel 2 select
	11	Channel 3 select
	XX	Readback
3, 2	00	Verify transfer
	01	Write transfer
	10	Read transfer
	11	Illegal
	XX	If bits 6 and 7 = 11
4	0	Autoinitialization disable
	1	Autoinitialization enable
5	0	Address increment select
	1	Address decrement select
7, 6	00	Demand mode select
	01	Single mode select
	10	Block mode select
	11	Cascade mode select

Request Register — The 82C37A can respond to requests for DMA service which are initiated by software as well as by a DREQ. Each channel has a request bit associated with it in the 4-bit Request register. These are non-maskable and subject to prioritization by the priority Encoder network. Each register bit is set or reset separately under software control. The entire register is cleared by a Reset. To set or reset a bit, the software loads the proper form of the data word. See Figure 3 for register address coding, and the following table for request register format. A software request for DMA operation can be made in block or single modes. For memory-to-memory transfers, the software request for channel 0 should be set. When reading the request register, bits 4-7 will always read as ones, and bits 0-3 will display the request bits of channels 0-3 respectively.

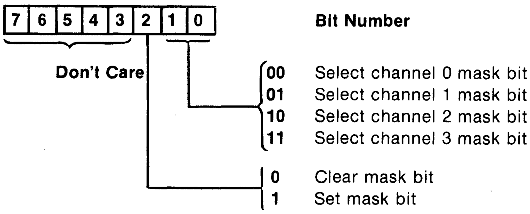
Request Register

Bit Number: 7 6 5 4 3 2 1 0

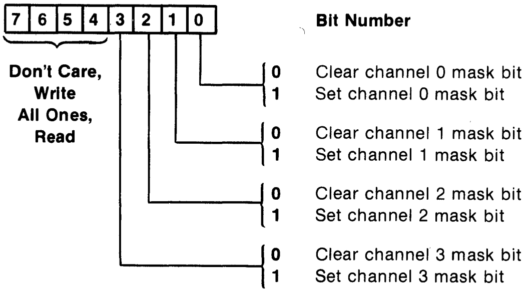
7–4		Don't Care, Write; Bits 4-7 All Ones, Read
1, 0	00	Select channel 0
	01	Select channel 1
	10	Select channel 2
	11	Select channel 3
2	0	Reset request bit
	1	Set request bit

Mask Register — Each channel has associated with it a mask bit which can be set to disable an incoming DREQ. Each mask bit is set when its associated channel produces an $\overline{EOP}$ if the channel is not programmed to Autoinitialize. Each bit of the 4-bit Mask register may also be set or cleared separately or simultaneously under software control. The entire register is also set by a Reset or Master Clear. This disables all hardware DMA requests until a clear Mask register instruction allows them to occur. The instruction to separately set or clear the mask bits is similar in form to that used with the Request register. Refer to the following table and Figure 3 for details. When reading the mask register, bits 4-7 will always read as logical ones, and bits 0-3 will display the mask bits of channel 0-3, respectively. The 4 bits of the mask register may be cleared simultaneously by using the Clear Mask Register command (see software commands section).

Mask Register

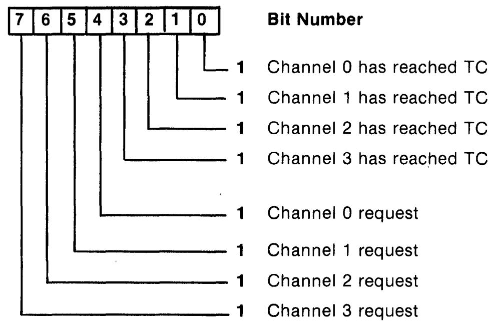


All four bits of the Mask register may also be written with a single command.



Status Register — The Status register is available to be read out of the 82C37A by the microprocessor. It contains information about the status of the devices at this point. This information includes which channels have reached a terminal count and which channels have pending DMA requests. Bits 0-3 are set every time a TC is reached by that channel or an external $\overline{EOP}$ is applied. These bits are cleared upon Reset, Master Clear, and on each Status Read. Bits 4-7 are set whenever their corresponding channel is requesting service, regardless of the mask bit state. If the mask bits are set, software can poll the status register to determine which channels have DREQs, and selectively clear a mask bit, thus allowing user defined service priority. Status bits 4-7 are updated while the clock is high, and latched on the falling edge. Status Bits 4-7 are cleared upon Reset or Master Clear.

Status Register



Temporary Register — The Temporary register is used to hold data during memory-to-memory transfers. Following the completion of the transfers, the last word moved can be read by the microprocessor. The Temporary register always contains the last byte transferred in the previous memory-to-memory operation, unless cleared by a Reset or Master Clear.

OPERATION	A3	A2	A1	A0	$\overline{IOR}$	$\overline{IOW}$
Read Status Register	1	0	0	0	0	1
Write Command Register	1	0	0	0	1	0
Read Request Register	1	0	0	1	0	1
Write Request Register	1	0	0	1	1	0
Read Command Register	1	0	1	0	0	1
Write Single Mask Bit	1	0	1	0	1	0
Read Mode Register	1	0	1	1	0	1
Write Mode Register	1	0	1	1	1	0
Set Byte Pointer F/F	1	1	0	0	0	1
Clear Byte Pointer F/F	1	1	0	0	1	0
Read Temporary Register	1	1	0	1	0	1
Master Clear	1	1	0	1	1	0
Clear Mode Reg. Counter	1	1	1	0	0	1
Clear Mask Register	1	1	1	0	1	0
Read All Mask Bits	1	1	1	1	0	1
Write All Mask Bits	1	1	1	1	1	0

FIGURE 3. SOFTWARE COMMAND CODES AND REGISTER CODES

Software Commands

There are special software commands which can be executed by reading or writing to the 82C37A. These commands do not depend on the specific data pattern on the data bus, but are activated by the I/O operation itself. On read type commands, the data value is not guaranteed. These commands are:

Clear First/Last Flip-Flop: This command is executed prior to writing or reading new address or word count information to the 82C37A. This initializes the flip-flop to a known state so that subsequent accesses to register contents by the microprocessor will address upper and lower bytes in the correct sequence.

Set First/Last Flip-Flop: This command will set the flip-flop to select the high byte first on read and write operations to address and word count registers.

Master Clear: This software instruction has the same effect as the hardware Reset. The Command, Status, Request, and Temporary registers, and Internal First/Last Flip-Flop and mode register counter are cleared and the Mask register is set. The 82C37A will enter the Idle cycle.

Clear Mask Register: This command clears the mask bits of all four channels, enabling them to accept DMA requests.

Clear Mode Register Counter: Since only one address location is available for reading the mode registers, an internal two-bit counter has been included to select mode registers during read operations. To read the mode registers, first execute the clear mode register counter command, then do consecutive reads until the desired channel is read. Read order is channel 0 first, channel 3 last. The lower two bits on all mode registers will read as ones.

External $\overline{EOP}$ Operation

The $\overline{EOP}$ pin is a bidirectional, open drain pin which may be driven by external signals to terminate DMA operation. Because $\overline{EOP}$ is an open drain pin an external pull-up resistor is required. The value of the external pull-up resistor used should guarantee a rise time of less than 125ns. It is important to note that the 82C37A will not accept external $\overline{EOP}$ signals when it is in an SI (Idle) state. The controller must be active to latch EXT $\overline{EOP}$. Once latched, the EXT $\overline{EOP}$ will be acted upon during the next S2 state, unless the 82C37A enters an idle state first. In the latter

Channel	Register	Operation	Signals $\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A3	A2	A1	A0	Internal Flip-Flop	Data Bus DB0-DB7
0	Base and Current Address	Write	0	1	0	0	0	0	0	0	A0-A7
			0	1	0	0	0	0	0	1	A8-A15
	Current Address	Read	0	0	1	0	0	0	0	0	A0-A7
			0	0	1	0	0	0	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	0	0	1	0	W0-W7
			0	1	0	0	0	0	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	0	0	1	0	W0-W7
			0	0	1	0	0	0	1	1	W8-W15
1	Base and Current Address	Write	0	1	0	0	0	1	0	0	A0-A7
			0	1	0	0	0	1	0	1	A8-A15
	Current Address	Read	0	0	1	0	0	1	0	0	A0-A7
			0	0	1	0	0	1	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	0	1	1	0	W0-W7
			0	1	0	0	0	1	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	0	1	1	0	W0-W7
			0	0	1	0	0	1	1	1	W8-W15
2	Base and Current Address	Write	0	1	0	0	1	0	0	0	A0-A7
			0	1	0	0	1	0	0	1	A8-A15
	Current Address	Read	0	0	1	0	1	0	0	0	A0-A7
			0	0	1	0	1	0	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	1	0	1	0	W0-W7
			0	1	0	0	1	0	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	1	0	1	0	W0-W7
			0	0	1	0	1	0	1	1	W8-W15
3	Base and Current Address	Write	0	1	0	0	1	1	0	0	A0-A7
			0	1	0	0	1	1	0	1	A8-A15
	Current Address	Read	0	0	1	0	1	1	0	0	A0-A7
			0	0	1	0	1	1	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	1	1	1	0	W0-W7
			0	1	0	0	1	1	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	1	1	1	0	W0-W7
			0	0	1	0	1	1	1	1	W8-W15

FIGURE 4. WORD COUNT AND ADDRESS REGISTER COMMAND CODES.

case, the latched $\overline{EOP}$ is cleared. External $\overline{EOP}$ pulses occurring between active DMA transfers in demand mode will not be recognized, since the 82C37A is in an SI state.

Application Information

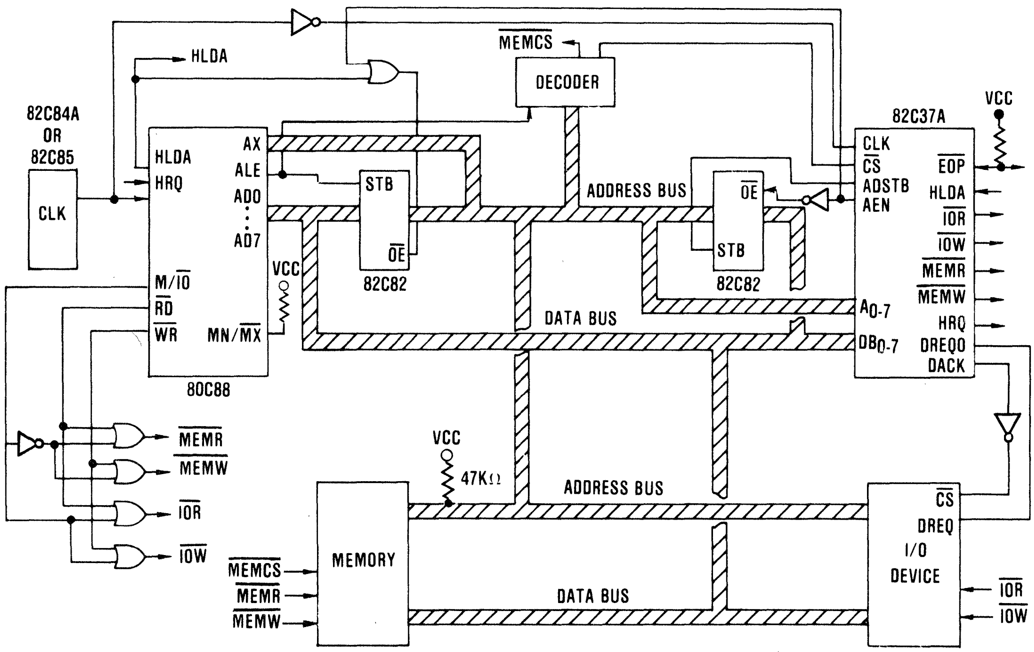
Figure 5 shows an application for a DMA system utilizing the 82C37A DMA controller and the 80C88 Microprocessor. In this application, the 82C37A DMA controller is used to improve system performance by allowing an I/O device to transfer data directly to or from system memory.

Components

The system clock is generated by the 82C84A clock driver and is inverted to meet the clock high and low times required by the 82C37A DMA controller. The four OR gates are used to support the 80C88 Microprocessor in minimum mode by producing the control signals used by the processor to access memory or I/O. A decoder is used to generate chip select for the DMA controller and memory. The most significant bits of the address are output on the address/data bus. Therefore, the 82C82 octal latch is used to demultiplex the address. Hold Acknowledge (HLDA) and Address Enable (AEN) are "ORed" together to insure that the DMA controller does not have bus contention with the microprocessor.

Operation

A DMA request (DREQ) is generated by the I/O device. After receiving the DMA request, the DMA controller will issue a Hold request (HRQ) to the processor. The system busses are not released to the DMA controller until a Hold Acknowledge signal is returned to the DMA controller from the 80C88 processor. After the Hold Acknowledge has been received, addresses and control signals are generated by the DMA controller to accomplish the DMA transfers. Data is transferred directly from the I/O device to memory (or vice versa) with $\overline{IOR}$ and $\overline{MEMW}$ (or $\overline{MEMR}$ and $\overline{IOW}$) being active. Note that data is not read into or driven out of the DMA controller in I/O-to-memory or memory-to-I/O data transfers.



NOTE: The address lines need pull-up resistors

FIGURE 5. APPLICATION FOR DMA SYSTEM

Absolute Maximum Ratings

Supply Voltage	+8.0 Volts
Input, Output or I/O Voltage Applied	GND -0.5V to VCC +0.5V
Storage Temperature Range	-65°C to +150°C
Maximum Package Power Dissipation	1 Watt
θ_{jc}	16°C/W (Cerdip Package), 21°C/W (LCC Package)
θ_{ja}	43°C/W (Cerdip Package), 48°C/W (LCC Package)
Gate Count	2,325 Gates
Junction Temperature	+150°C
Lead Temperature (Soldering, Ten Seconds)	+260°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range	+4.5 to +5.5V
Operating Temperature Ranges	
C82C37A	0°C to +70°C
I82C37A	-40°C to +85°C
M82C37A	-55°C to +125°C

D.C. Electrical Specifications

VCC = 5.0V ±10%, TA = 0°C to +70°C (C82C37A)
TA = -40°C to +85°C (I82C37A), TA = -55°C to +125°C (M82C37A)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	Logical One Input Voltage	2.0 2.2		V V	C82C37A I82C37A, M82C37A
VIL	Logical Zero Input Voltage		0.8	V	
VOH	Output High Voltage	3.0 VCC -0.4		V V	IOH = -2.5mA IOH = -100μA
VOL	Output Low Voltage		0.4	V	IOL = +2.5mA
II	Input Leakage Current	-1.0	+1.0	μA	VIN = GND or VCC pins 11, 12, 13, 6, 7, 16-19
IO	I/O and Output	-10.0	+10.0	μA	VO = GND or VCC pins 21-23, 26-30, 1, 2, 36, 32-35, 37-40, 3, 4
ICCSB	Standby Power Supply Current		10	μA	VCC = 5.5V VIN = VCC or GND Outputs Open
ICCOP	Operating Power Supply Current		2	mA/mHz	VCC = 5.5V CLK FREQ = 5MHz VIN = VCC or GND Outputs Open

Capacitance

TA = 25°C; VCC = GND = OV; VIN = +5V or GND

SYMBOL	PARAMETER	TYP	UNITS	TEST CONDITIONS
CIN*	Input Capacitance	5	pF	FREQ = 1MHz Unmeasured pins returned to GND
COUT*	Output Capacitance	15	pF	
CI/O*	I/O Capacitance	20	pF	

* Guaranteed and sampled, but not 100% tested.

A.C. Electrical Specifications

VCC = +5V ±10%, GND = 0V
TA = 0°C to +70°C (C82C37A) (C82C37A-5)
TA = -40°C to +85°C (I82C37A) (I82C37A-5)
TA = -55°C to +125°C (M82C37A) (M82C37A-5)

DMA (Master) Mode

SYMBOL	PARAMETER	82C37A-5		82C37A		UNITS
		MIN	MAX	MIN	MAX	
TAEL	AEN HIGH from CLK LOW (S1) Delay Time		175		105	ns
TAET	AEN LOW from CLK HIGH (SI) Delay Time		130		80	ns
TAFAB	ADR Active to Float Delay from CLK HIGH		90		55	ns
TAFC	$\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ Float Delay from CLK HIGH		120		75	ns
TAFDB	DB Active to Float Delay from CLK HIGH		170		135	ns
TAHR	ADR from $\overline{\text{READ}}$ HIGH Hold Time	TCY-100		TCY-75		ns
TAHS	DB from ADSTB LOW Hold Time	TCL-18		TCL-18		ns
TAHW	ADR from $\overline{\text{WRITE}}$ HIGH Hold Time	TCY-50		TCY-50		ns
TAK	DACK Valid from CLK LOW Delay Time		170		105	ns
	$\overline{\text{EOP}}$ HIGH from CLK HIGH Delay Time		170		105	ns
	$\overline{\text{EOP}}$ LOW to CLK HIGH Delay Time		100		60	ns
TASM	ADR Stable from CLK HIGH		110		60	ns
TASS	DB to ADSTB LOW Setup Time	TCH+10		TCH+10		ns
TCH	Clock High Time (Transitions 10ns)	70		55		ns
TCL	Clock LOW Time (Transitions 10ns)	50		43		ns
TCY	CLK Cycle Time	200		125		ns
TDCL	CLK HIGH to $\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ LOW Delay		190		120	ns
TDCTR	$\overline{\text{READ}}$ HIGH from CLK HIGH (S4) Delay Time		190		115	ns
TDCTW	WRITE HIGH from CLK HIGH (S4) Delay Time		130		80	ns
TDQ1	HRQ Valid from CLK HIGH Delay Time		120		75	ns
TDQ2			120		75	ns
TEPS	$\overline{\text{EOP}}$ LOW from CLK LOW Setup Time	40		25		ns
TEPW	$\overline{\text{EOP}}$ Pulse Width	220		135		ns
TFAAB	ADR Float to Active Delay from CLK HIGH		110		60	ns
TFAC	$\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ Active from CLK HIGH		150		90	ns
TFADB	DB Float to Active Delay from CLK HIGH		110		60	ns
THS	HLDA Valid to CLK HIGH Setup Time	75		45		ns
TIDH	Input Data from $\overline{\text{MEMR}}$ HIGH Hold Time	0		0		ns
TIDS	Input Data to $\overline{\text{MEMR}}$ HIGH Setup Time	155		90		ns
TODH	Output Data from $\overline{\text{MEMW}}$ HIGH Hold Time	15		15		ns
TODV	Output Data Valid to $\overline{\text{MEMW}}$ HIGH	TCY-35		TCY-35		ns
TQS	DREQ to CLK LOW (SI, S4) Setup Time	0		0		ns
TRH	CLK to READY LOW Hold Time	20		20		ns
TRS	READY to CLK LOW Setup Time	60		35		ns
TCLSH	ADSTB HIGH from CLK LOW Delay Time		80		50	ns
TCLSL	ADSTB LOW from CLK LOW Delay Time		120		120	ns

A.C. Electrical Specifications

DMA Master Mode

		82C37A-5		82C37A		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
TWRRD	READ HIGH Delay from WRITE HIGH	0		0		ns
TRLRH	READ Pulse Width, Normal Timing	2TCY-50		2TCY-50		ns
TSHSL	ADSTB Pulse Width	TCY-80		TCY-50		ns
TWLWHA	Extended WRITE Pulse Width	2TCY-100		2TCY-75		ns
TWLWH	WRITE Pulse Width	TCY-100		TCY-75		ns
TRLRHC	READ Pulse Width, Compressed	TCY-50		TCY-50		ns
Peripheral (Slave) Mode						
TAR	ADR Valid or CS LOW to READ LOW	10		10		ns
TAWL	ADR Valid to WRITE LOW Setup Time	0		0		ns
TCWL	CS LOW to WRITE LOW Setup Time	0		0		ns
TDW	Data Valid to WRITE HIGH Setup Time	150		100		ns
TRA	ADR or CS Hold from READ HIGH	0		0		ns
TRDE	Data Access from READ		140		120	ns
TRDF	DB Float Delay from READ HIGH	10	85	10	85	ns
TRSTD	Power Supply HIGH to RESET LOW Setup Time	500		500		ns
TRSTS	RESET to First IOWR	2TCY		2TCY		ns
TRSTW	RESET Pulse Width	300		300		ns
TRW	READ Width	200		155		ns
TWA	ADR from WRITE HIGH Hold Time	0		0		ns
TWC	CS HIGH from WRITE HIGH Hold Time	0		0		ns
TWD	Data from WRITE HIGH Hold Time	10		10		ns
TWWS	WRITE Width	150		100		ns

Waveforms

Slave Mode Write Timing

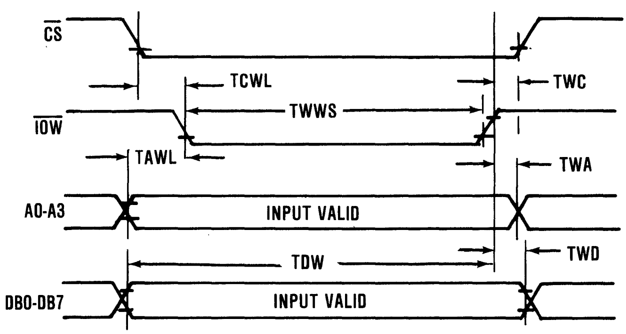


FIGURE 6. SLAVE MODE TIMING

NOTE: Successive WRITE accesses to the 82C37A must allow at least TCY as recovery time between accesses.

Waveforms

Slave Mode Read Timing

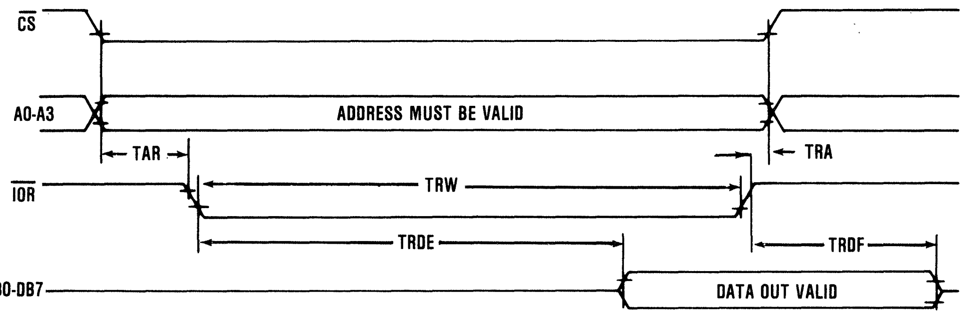


FIGURE 7. SLAVE MODE READ

NOTE: Successive READ accesses to the 82C37A must allow at least TCY as recovery time between accesses.

DMA Transfer Timing

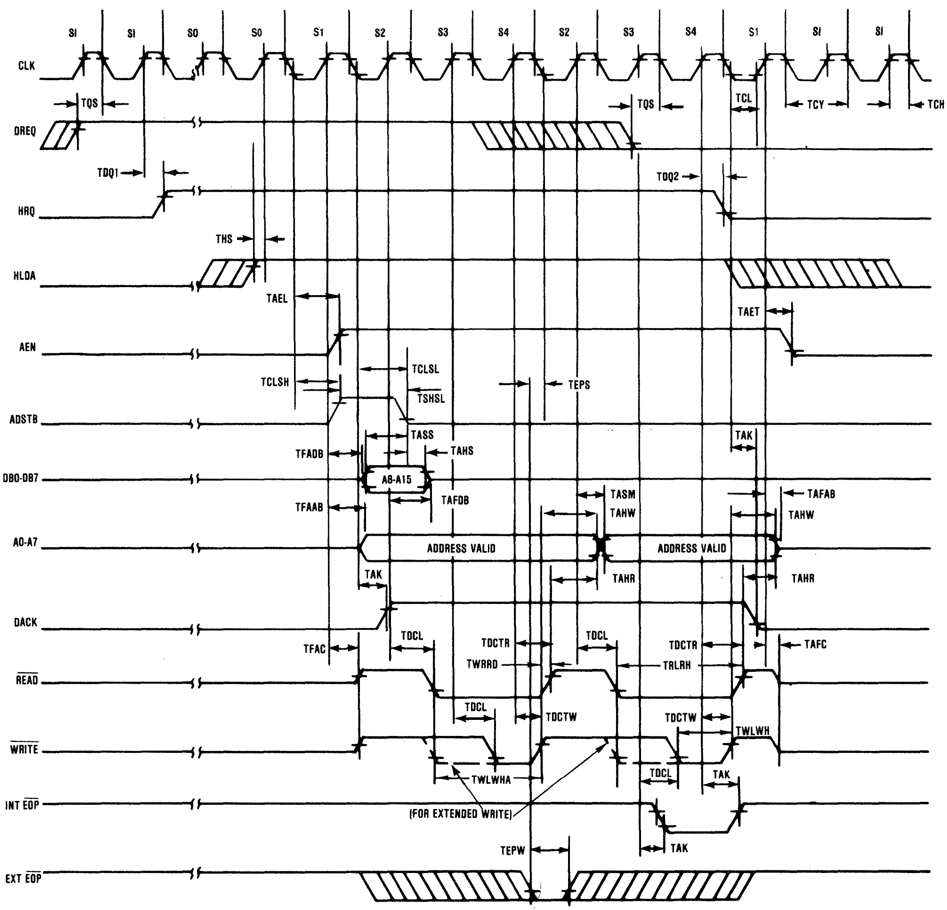


FIGURE 8. DMA TRANSFER

Waveforms

Memory-to-Memory Transfer Timing

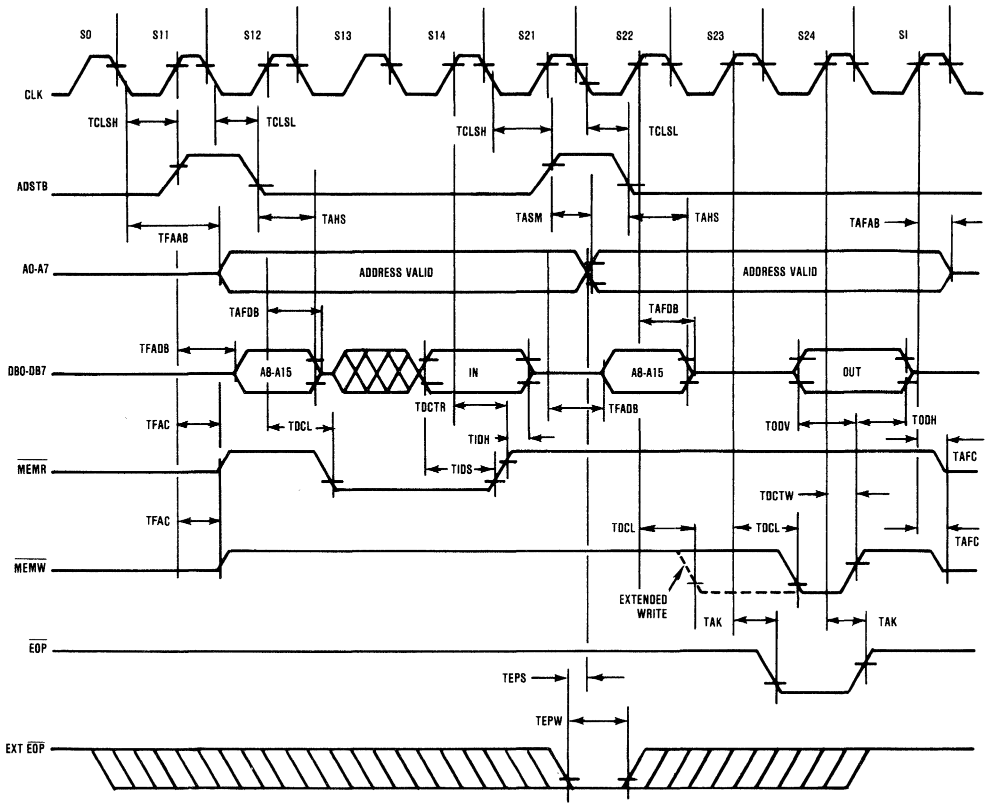


FIGURE 9. MEMORY-TO-MEMORY TRANSFER

Ready Timing

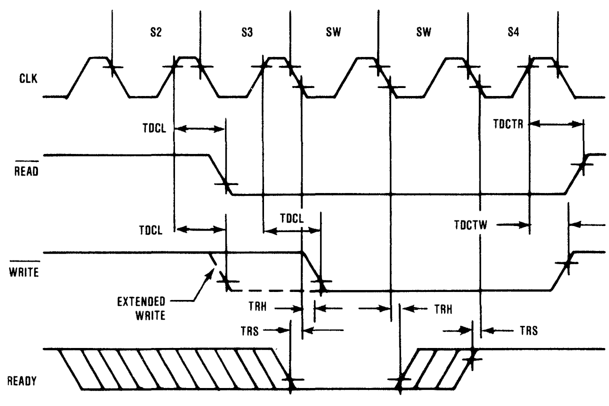


FIGURE 10. READY

Waveforms

Compressed Transfer Timing

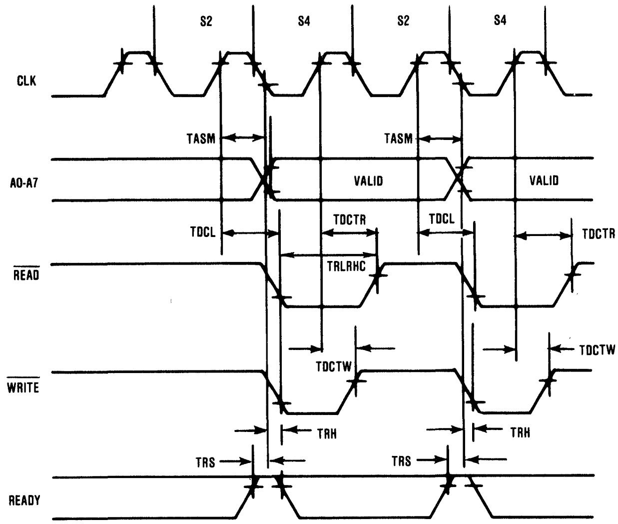


FIGURE 11. COMPRESSED TRANSFER

Reset Timing

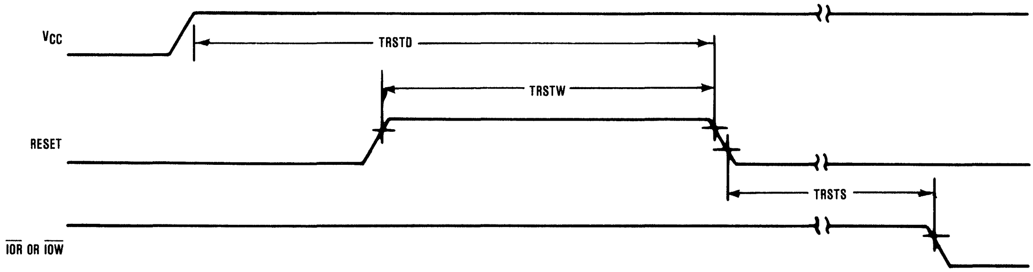
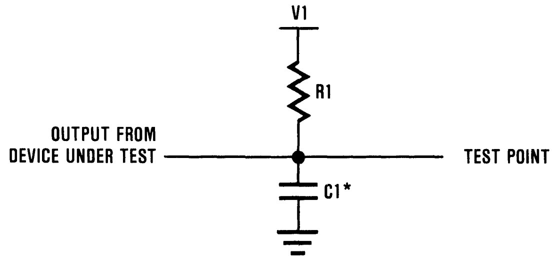


FIGURE 12. RESET

A. C. Test Circuits

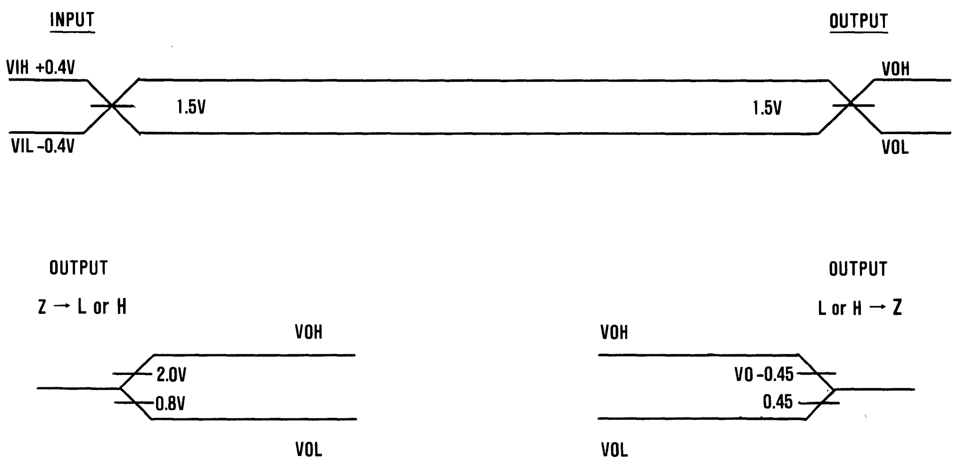


* Includes STRAY and JIG Capacitance

TEST CONDITION DEFINITION TABLE

PINS	V1	R1	C1
All Outputs Except $\overline{EOP}$	1.7V	520Ω	100pF
$\overline{EOP}$	VCC	1.6KΩ	50pF

A. C. Testing Input, Output Waveforms



A. C. Testing: All A. C. Parameters tested as per test circuits. Input RISE and FALL times are driven at Ins/V.

HARRIS

82C50A

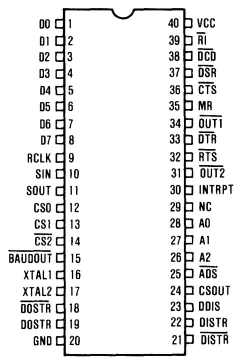
CMOS Asynchronous Communications Element

Features

- Single Chip UART/BRG
- DC to 10 MHz Operation, (DC to 625K Baud)
- Crystal or External Clock Input
- On Chip Baud Rate Generator 1 to 65535 Divisor Generates 16X Clock
- Prioritized Interrupt Mode
- Fully TTL/CMOS Compatible
- Microprocessor Bus Oriented Interface
- 80C86/80C88 Compatible
- Scaled SAJI IV CMOS Process
- Low Power - 1 mA/MHz Typical
- Modem Interface
- Line Break Generation and Detection
- Loopback and Echo Modes
- Doubled Buffered Transmitter and Receiver
- Single 5V Supply

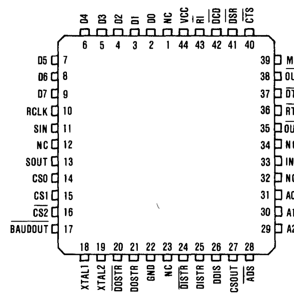
Pinouts

TOP VIEW



LCC/PLCC

TOP VIEW



Description

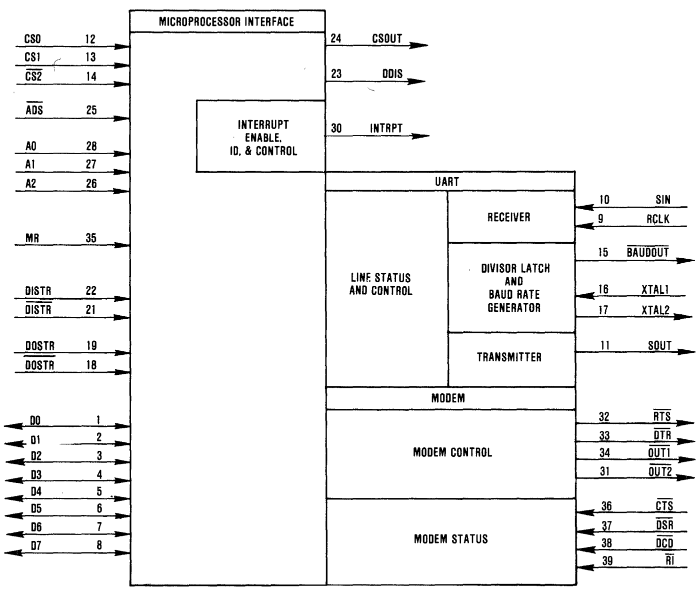
The 82C50A Asynchronous Communication Element (ACE) is a high performance programmable Universal Asynchronous Receiver/Transmitter (UART) and Baud Rate Generator (BRG) on a single chip. Using Harris Semiconductor's advanced Scaled SAJI IV CMOS Process, the ACE will support data rates from DC to 625K baud (0-10 MHz clock).

The ACE's receiver circuitry converts start, data, stop, and parity bits into a parallel data word. The transmitter circuitry converts a parallel data word into serial form and appends the start, parity, and stop bits. The word length is programmable to 5, 6, 7, or 8 data bits. Stop bit selection provides a choice of 1, 1.5, or 2 stop bits.

The Baud Rate Generator divides the clock by a divisor programmable from 1 to 2^{16}-1 to provide standard RS-232C baud rates when using any one of three industry standard baud rate crystals (1.8432 MHz, 2.4576 MHz, or 3.072 MHz). A programmable buffered clock output (BAUDOUT) provides either a buffered oscillator or 16X (16 times the data rate) baud rate clock for general purpose system use.

To meet the system requirements of a CPU interfacing to an asynchronous channel, the modem control signals RTS, CTS, DSR, DTR, RI, DCD are provided. Inputs and outputs have been designed with full TTL/CMOS compatability in order to facilitate mixed TTL/NMOS/CMOS system design.

Functional Diagram



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Pin Description

SYMBOL	PIN NUMBER	TYPE	ACTIVE LEVEL	DESCRIPTION
DISTR, $\overline{\text{DISTR}}$	22 21	I I	H L	DATA IN STROBE, $\overline{\text{DATA IN STROBE}}$: DISTR, $\overline{\text{DISTR}}$ are read inputs which cause the 82C50A to output data to the data bus (D0-D7). The data output depends upon the register selected by the address inputs A0, A1, A2. The chip select inputs CS0, CS1, $\overline{\text{CS2}}$ enable the DISTR, $\overline{\text{DISTR}}$ inputs. Only an active DISTR or $\overline{\text{DISTR}}$, not both, is used to receive data from the 82C50A during a read operation. If DISTR is used as the read input, $\overline{\text{DISTR}}$ should be tied high. If $\overline{\text{DISTR}}$ is used as the active read input, DISTR should be tied low.
DOSTR, $\overline{\text{DOSTR}}$	19 18	I I	H L	DATA OUT STROBE, $\overline{\text{DATA OUT STROBE}}$: DOSTR, $\overline{\text{DOSTR}}$ are write inputs which cause data from the data bus (D0-D7) to be input to the 82C50A. The data input depends upon the register selected by the address inputs A0, A1, A2. The chip select inputs CS0, CS1, $\overline{\text{CS2}}$ enable the DOSTR, $\overline{\text{DOSTR}}$ inputs. Only an active DOSTR or $\overline{\text{DOSTR}}$, not both, is used to transmit data to the 82C50A during a write operation. If DOSTR is used as the write input, $\overline{\text{DOSTR}}$ should be tied high. If $\overline{\text{DOSTR}}$ is used as the write input, DOSTR should be tied low.
D0-D7	1-8	I/O		DATA BITS 0-7: The Data Bus provides eight, 3-state input/output lines for the transfer of data, control and status information between the 82C50A and the CPU. For character formats of less than 8 bits, D7, D6 and D5 are "don't cares" for data write operations and 0 for data read operations. These lines are normally in a high impedance state except during read operations. D0 is the Least Significant Bit (LSB) and is the first serial data bit to be received or transmitted.
A0, A1, A2	28, 27, 26	I I	H	REGISTER SELECT: The address lines select the internal registers during CPU bus operations. See Table 1.
XTAL1, XTAL2	16 17	I O		CRYSTAL/CLOCK: Crystal connections for the internal Baud Rate Generator. XTAL1 can also be used as an external clock input, in which case XTAL2 should be left open.
SOUT	11	O		SERIAL DATA OUTPUT: Serial data output from the 82C50A transmitter circuitry. A Mark (1) is a logic one (high) and Space (0) is a logic zero (low). SOUT is held in the Mark condition when the transmitter is disabled, MR is true, the Transmitter Register is empty, or when in the Loop Mode. SOUT is not affected by the $\overline{\text{CTS}}$ input.
GND	20		L	GROUND: Power supply ground connection (VSS).
$\overline{\text{CTS}}$	36	I	L	$\overline{\text{CLEAR TO SEND}}$: The logical state of the $\overline{\text{CTS}}$ pin is reflected in the CTS bit of the (MSR) Modem Status Register (CTS is bit 4 of the MSR, written MSR(4)). A change of state in the $\overline{\text{CTS}}$ pin since the previous reading of the MSR causes the setting of DCTS (MSR(0)) of the Modem Status Register. When $\overline{\text{CTS}}$ pin is ACTIVE (low), the modem is indicating that data on SOUT can be transmitted on the communications link. If $\overline{\text{CTS}}$ pin goes INACTIVE (high), the 82C50A should not be allowed to transmit data out of SOUT. $\overline{\text{CTS}}$ pin does not affect Loop Mode operation.
$\overline{\text{DSR}}$	37	I	L	$\overline{\text{DATA SET READY}}$: The logical state of the $\overline{\text{DSR}}$ pin is reflected in MSR(5) of the Modem Status Register. DDSR (MSR(1)) indicates whether the $\overline{\text{DSR}}$ pin has changed state since the previous reading of the MSR. When the $\overline{\text{DSR}}$ pin is ACTIVE (low), the modem is indicating that it is ready to exchange data with the 82C50A, while the $\overline{\text{DSR}}$ Pin INACTIVE (high) indicates that the modem is not ready for data exchange. The ACTIVE condition indicates only the condition of the local Data Communications Equipment (DCE), and does not imply that a data circuit as been established with remote equipment.

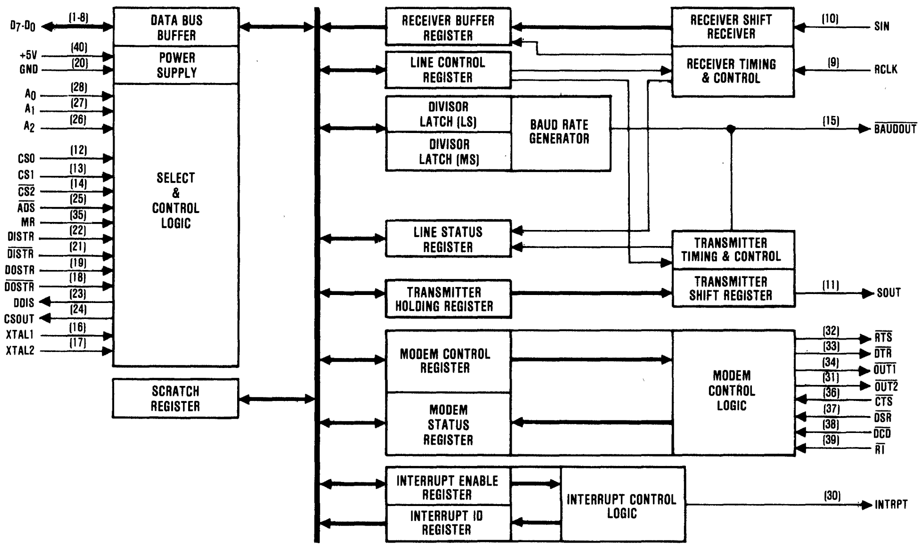
Pin Description

SYMBOL	PIN NUMBER	TYPE	ACTIVE LEVEL	DESCRIPTION
$\overline{DTR}$	33	O	L	DATA TERMINAL READY: The $\overline{DTR}$ pin can be set (low) by writing a logic 1 to MCR(0), Modem Control Register bit 0. This signal is cleared (high) by writing a logic 0 to the DTR bit (MCR(0)) or whenever a MR ACTIVE (high) is applied to the 82C50A. When ACTIVE (low), $\overline{DTR}$ pin indicates to the DCE that the 82C50A is ready to receive data. In some instances, $\overline{DTR}$ pin is used as a power on indicator. The INACTIVE (high) state causes the DCE to disconnect the modem from the telecommunications circuit.
$\overline{RTS}$	32	O	L	REQUEST TO SEND: The $\overline{RTS}$ signal is an output used to enable the modem. The $\overline{RTS}$ pin is set low by writing a logic 1 to MCR(1) bit 1 of the Modem Control Register. The $\overline{RTS}$ pin is reset high by Master Reset. When ACTIVE, the $\overline{RTS}$ pin indicates to the DCE that the 82C50A has data ready to transmit. In half duplex operations, $\overline{RTS}$ is used to control the direction of the line.
$\overline{BAUDOUT}$	15	O		BAUDOUT: This output is a 16X clock out used for the transmitter section (16X = 16 times the data rate). The $\overline{BAUDOUT}$ clock rate is equal to the reference oscillator frequency divided by the specified divisor in the Baud Rate Generator Divisor Latches DLL and DLM. $\overline{BAUDOUT}$ may be used by the Receiver section by tying this output to RCLK.
$\overline{OUT1}$	34	O	L	OUTPUT 1: This is a general purpose output that can be programmed ACTIVE (low) by setting MCR(2) (OUT1) of the Modem Control Register to a high level. The $\overline{OUT1}$ pin is set high by Master Reset. The $\overline{OUT1}$ pin is INACTIVE (high) during loop mode operation.
$\overline{OUT2}$	31	O	L	OUTPUT 2: This is a general purpose output that can be programmed ACTIVE (low) by setting MCR(3) (OUT2) of the Modem Control Register to a high level. The $\overline{OUT2}$ pin is set high by Master Reset. The $\overline{OUT2}$ signal is INACTIVE (high) during loop mode operation.
$\overline{RI}$	39	I	L	RING INDICATOR: When low, $\overline{RI}$ indicates that a telephone ringing signal has been received by the modem or data set. The $\overline{RI}$ signal is a modem control input whose condition is tested by reading MSR(6) (RI). The Modem Status Register output TERI (MSR(2)) indicates whether the $\overline{RI}$ input has changed from a High to Low since the previous reading of the MSR. If the interrupt is enabled (IER(3)=1) and $\overline{RI}$ changes from a high to low, an interrupt is generated. The ACTIVE (low) state of $\overline{RI}$ indicates that the DCE is receiving a ringing signal. $\overline{RI}$ will appear ACTIVE for approximately the same length of time as the ACTIVE segment of the ringing cycle. The INACTIVE state of $\overline{RI}$ will occur during the INACTIVE segments of the ringing cycle, or when ringing is not detected by the DCE. This circuit is not disabled by the INACTIVE condition of $\overline{DTR}$.
$\overline{DCD}$	38	I	L	DATA CARRIER DETECT: When ACTIVE (low), $\overline{DCD}$ indicates that the data carrier has been detected by the modem or data set. $\overline{DCD}$ is a modem input whose condition can be tested by the CPU by reading MSR(7) (DCD) of the Modem Status Register. MSR(3) (DDCD) of the Modem Status Register indicates whether the $\overline{DCD}$ input has changed since the previous reading of the MSR. $\overline{DCD}$ has no effect on the receiver. If the $\overline{DCD}$ changes state with the modem status interrupt enabled, an interrupt is generated. When $\overline{DCD}$ is ACTIVE (low), the received line signal from the remote terminal is within the limits specified by the DCE manufacturer. The INACTIVE (high) signal indicates that the signal is not within the specified limits, or is not present.

Pin Description

SYMBOL	PIN NUMBER	TYPE	ACTIVE LEVEL	DESCRIPTION
MR	35	I	H	MASTER RESET: The MR input forces the 82C50A into an idle mode in which all serial data activities are suspended. The Modem Control Register (MCR) along with its associated outputs are cleared. The Line Status Register (LSR) is cleared except for the THRE and TEMT bits, which are set. The 82C50A remains in an idle state until programmed to resume serial data activities. The MR input is a Schmitt trigger input. See the D. C. Electrical Characteristics for Schmitt trigger logic input voltage levels. See Table 7 for a summary of Master Reset's effect on 82C50A operation.
INTRPT	30	O	H	INTERRUPT REQUEST: The INTRPT output goes ACTIVE (high) when one of the following interrupts has an ACTIVE (high) condition and is enabled by the Interrupt Enable Register: Receiver Error flag, Received Data Available, Transmitter Holding Register Empty, and Modem Status. The INTRPT is reset low upon appropriate service or a MR operation. See Figure 1. Interrupt Control Structure.
SIN	10	I	H	SERIAL DATA INPUT: The SIN input is the serial data input from the communication line or modem to the 82C50A receiver circuits. A mark (1) is high, and a space (0) is low. Data inputs on SIN are disabled when operating in the loop mode.
VCC	40		H	VCC: +5 volt positive power supply pin. A 0.1μA decoupling capacitor from VCC (pin 40) to GND (pin 20) is recommended.
CS0, CS1 $\overline{CS2}$	12, 13, 14	I I	H, H L	CHIP SELECT: The Chip Select inputs acts as enable signals for the write (DOSTR, $\overline{DOSTR}$) and read (DISTR, $\overline{DISTR}$) input signals. The Chip Select inputs are latched by the $\overline{ADS}$ input.
NC	29			Do Not Connect
CSOUT	24	O	H	CHIP SELECT OUT: When ACTIVE (high), this pin indicates that the chip has been selected by active CS0, CS1, and $\overline{CS2}$ inputs. No data transfer can be initiated until CSOUT is a logic 1, ACTIVE (high).
DDIS	23	O	H	DRIVER DISABLE: This output is INACTIVE (low) when the CPU is reading data from the 82C50A. An ACTIVE (high) DDIS output can be used to disable an external transceiver when the CPU is reading data.
$\overline{ADS}$	25	I	L	$\overline{\text{ADDRESS STROBE}}$: When ACTIVE (low), $\overline{ADS}$ latches the Register Select (A0,A1,A2) and Chip Select (CS0, CS1, $\overline{CS2}$) inputs. An active $\overline{ADS}$ is required when the Register Select pins are not stable for the duration of the read or write operation, multiplexed mode. If not required, the $\overline{ADS}$ input should be tied low, non-multiplexed mode.
RCLK	9	I		This input is the 16X Baud Rate Clock for the receiver section of the 82C50A. This input may be provided from the $\overline{BAUDOUT}$ output or an external clock.

Block Diagram



Accessible Registers

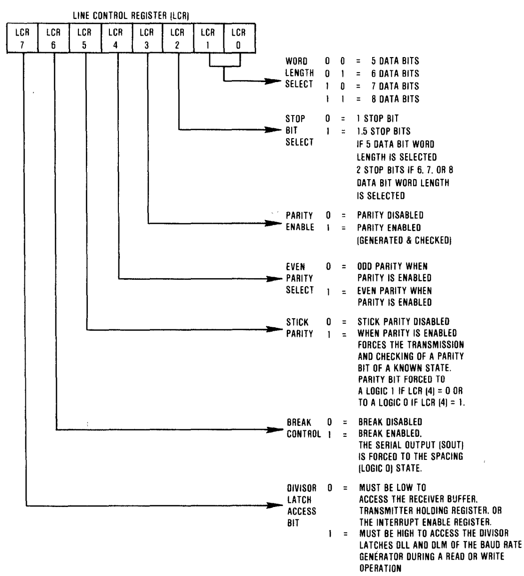
The three types of internal registers in the 82C50A used in the operation of the device are control, status, and data registers. The control registers are the Bit Rate Select Register DLL and DLM, Line Control Register, Interrupt Enable Register and the Modem Control registers, while the status registers are the Line Status Registers and the Modem Status Register. The data registers are the Receiver Buffer Register and Transmitter Holding Register. **The Address, Read, and Write inputs are used in conjunction with the Divisor Latch Access Bit in the Line Control Register (LCR(7)) to select the register to be written or read** (see Table 1.). Individual bits within these registers are referred to by the register mnemonic and the bit number in parenthesis. An example, LCR(7) refers to Line Control Register Bit 7.

TABLE 1. ACCESSING 82C50A INTERNAL REGISTERS

DLAB	A2	A1	A0	MNEMONIC	REGISTER
0	0	0	0	RBR	Receiver Buffer Register (read only)
0	0	0	0	THR	Transmitter Holding Register (write only)
0	0	0	1	IER	Interrupt Enable Register
X	0	1	0	IIR	Interrupt Identification Register (read only)
X	0	1	1	LCR	Line Control Register
X	1	0	0	MCR	Modem Control Register
X	1	0	1	LSR	Line Status Register
X	1	1	0	MSR	Modem Status Register
X	1	1	1	SCR	Scratch Register
1	0	0	0	DLL	Divisor Latch (LSB)
1	0	0	1	DLM	Divisor Latch (MSB)

X = "Don't Care" O = Logic Low 1 = Logic High

The Transmitter Buffer Register and Receiver Buffer Register are data registers holding from 5-8 data bits. If less than eight data bits are transmitted, data is right justified to the LSB. Bit 0 of a data word is always the first serial data bit received and transmitted. The 82C50A data registers are double buffered so that read and write operations can be performed at the same time the UART is performing the parallel to serial and serial to parallel conversion. This provides the microprocessor with increased flexibility in its read and write timing.



Line Control Register (LCR)

The format of the data character is controlled by the Line Control Register. The contents of the LCR may be read, eliminating the need for separate storage of the line characteristics in system memory. The contents of the LCR are described below.

LCR Bits 0 thru 7

LCR (0) Word Length Select Bit 0 (WLS0)
LCR (1) Word Length Select Bit 1 (WLS1)
LCR (2) Stop Bit Select (STB)
LCR (3) Parity Enable (PEN)
LCR (4) Even Parity Select (EPS)
LCR (5) Stick Parity
LCR (6) Set Break
LCR (7) Divisor Latch Access Bit (DLAB)

LCR(0) and LCR(1) word length select bit 0, word length select bit 1: The number of bits in each transmitted or received serial character is programmed as follows

LCR(1)	LCR(0)	WORD LENGTH
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

LCR(2) Stop Bit Select: LCR(2) specifies the number of stop bits in each transmitted character. If LCR(2) is a logic 0, one stop bit is generated in the transmitted data. If LCR(2) is a logic 1 when a 5 bit word length is selected, 1.5 stop bits are generated. If LCR(2) is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two stop bits are generated. The receiver checks for two stop bits if programmed.

LCR(3): Parity Enable: When LCR(3) is high, a parity bit between the last data word bit and stop bit is generated and checked.

LCR(4) Even Parity Select: When parity is enabled (LCR(3)=1), LCR(4)=0 selects odd parity, and LCR(4)=1 selects even parity.

LCR(5) Stick Parity: When parity is enabled (LCR(3)=1), LCR(5)=1 causes the transmission and reception of a parity bit to be in the opposite state from that indicated by LCR(4). This allows the user to force parity to a known state and for the receiver to check the parity bit in a known state.

LCR(6) Break Control: When LCR(6) is set to logic-1, the serial output (SOUT) is forced to the spacing (logic 0) state. The break is disabled by setting LCR(6) to a logic-0. The Break Control bit acts only on SOUT and has no effect on the transmitter logic. Break Control enables the CPU to alert a terminal in a computer communications system. If the following sequence is used, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all 0s pad character in response to THRE.
2. Set break in response to the next THRE.
3. Wait for the transmitter to be idle, (TEMT=1), and clear break when normal transmission has to be restored.

During the break, the transmitter can be used as a character timer to accurately establish the break duration.

LCR(7) Divisor Latch Access Bit (DLAB): LCR(7) must be set high (logic 1) to access the Divisor Latches DLL and DLM of the Baud Rate Generator during a read or write operation. LCR(7) must be input low to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

Line Status Register (LSR)

The LSR is a single register that provides status indications. The LSR is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of the 82C50A.

Three error flags OE, FE, and PE provide the status of any error conditions detected in the receiver circuitry. During reception of the stop bits, the error flags are set high by an error condition. The error flags are not reset by the absence of an error condition in the next received character. The flags reflect the last character only if no overrun occured. The Overrun Error (OE) indicates that a character in the Receiver Buffer Register has been overwritten by a character from the Receiver Shift Register before being read by the CPU. The character is lost. Framing Error (FE) indicates that the last character received contained incorrect (low) stop bits. This is caused by the absence of the required stop bit or by a stop bit too short to be detected. Parity Error (PE) indicates that the last character received contained a parity error based on the programmed and calculated parity of the received character.

The Break Interrupt (BI) status bit indicates that the last character received was a break character. A break character is an invalid data character, with the entire character, including parity and stop bits, logic zero.

The Transmitter Holding Register Empty (THRE) bit indicates that the THR register is empty and ready to receive another character. The Transmission Shift Register Empty (TEMT) bit indicates that the Transmitter Shift Register is empty, and the 82C50A has completed transmission of the last character. If the interrupt is enabled (IER(1)), an active THRE causes an interrupt (INTRPT).

The Data Ready (DR) bit indicates that the RBR has been loaded with a received character (including Break) and that the CPU may access this data.

Reading the LSR clears LSR(1)-LSR(4). (OE, PE, FE & BI)

LSR Bits 0 Thru 7

	LOGIC 1	LOGIC 0
LSR (0) Data Ready (DR)	Ready	Not Ready
LSR (1) Overrun Error (OE)	Error	No Error
LSR (2) Parity Error (PE)	Error	No Error
LSR (3) Framing Error (FE)	Error	No Error
LSR (4) Break Interrupt (BI)	Break	No Break
LSR (5) Transmitter Holding Register Empty (THRE)	Empty	Not Empty
LSR (6) Transmitter Empty (TEMT)	Empty	Not Empty
LSR (7) Not Used		

The contents of the Line Status Register are indicated in the above table and are described below.

LSR(0) Data Ready (DR): Data Ready is set high when an incoming character has been received and transferred into the Receiver Buffer Register. LSR(0) is reset low by a CPU read of the data in the Receiver Buffer Register.

LSR(1) Overrun Error (OE): Overrun Error indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, overwriting the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

LSR(2) Parity Error (PE): Parity Error indicates that the received data character does not have the correct even or odd parity, as selected by the Even Parity Select bit (LCR(4)). The PE bit is set high upon detection of a parity error, and is reset low when the CPU reads the contents of the LSR.

LSR(3) Framing Error (FE): Framing Error indicates that the received character did not have a valid stop bit. LSR(3) is set high when the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). The FE indicator is reset low when the CPU reads the contents of the LSR.

LSR(4) Break Interrupt (BI): Break Interrupt is set high when the received data input is held in the spacing (logic 0) state for longer than a full word transmission time (start bit + data bits + parity + stop bits). The BI indicator is reset when the CPU reads the contents of the Line Status Register.

LSR(1) - LSR(4) are the error conditions that produce a Receiver Line Status interrupt (priority 1 interrupt in the Interrupt Identification Register (IIR)) when any of the conditions are detected. This interrupt is enabled by setting IER(2)=1 in the Interrupt Enable Register.

LSR(5) Transmitter Holding Register Empty (THRE): THRE indicates that the 82C50A is ready to accept a new character for transmission. The THRE bit is set high when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. LSR(5) is reset low by the loading of the Transmitter Holding Register by the CPU. LSR(5) is not reset by a CPU read of the LSR.

When the THRE interrupt is enabled (IER(1)=1), THRE causes a priority 3 interrupt in the IIR. If THRE is the interrupt source indicated in IIR, INTRPT is cleared by a read of the IIR.

LSR(6) Transmitter Empty (TEMT): TEMT is set high when the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. LSR(6) is reset low when a character is loaded into the THR and remains low until the character is transferred out of SOUT. TEMT is not reset low by a CPU read of the LSR.

LSR(7): This bit is permanently set to logic 0.

Modem Control Register (MCR)

The MCR controls the interface with the modem or data set as described below. The MCR can be written and read. The $\overline{RTS}$, $\overline{DTR}$, $\overline{OUT1}$, and $\overline{OUT2}$ outputs are directly controlled by their control bits in this register. **A high input asserts a low (true) at the output pins.**

MCR Bits 0 thru 7

	MCR BIT LOGIC 1	MCR BIT LOGIC 0
MCR (0) Data Terminal Ready (DTR)	$\overline{DTR}$ Output Low	$\overline{DTR}$ Output High
MCR (1) Request to Send (RTS)	$\overline{RTS}$ Output Low	$\overline{RTS}$ Output High
MCR (2) OUT1	$\overline{OUT1}$ Output Low	$\overline{OUT1}$ Output High
MCR (3) OUT2	$\overline{OUT2}$ Output Low	$\overline{OUT2}$ Output High
MCR (4) LOOP	LOOP Enabled	LOOP Disabled
MCR (5) 0		
MCR (6) 0		
MCR (7) 0		

MCR(0): When MCR(0) is set high, the $\overline{DTR}$ output is forced low. When MCR(0) is reset low, the $\overline{DTR}$ output is forced high. The $\overline{DTR}$ output of the 82C50A may be input into an EIA inverting line driver as the 1488 to obtain the proper polarity input at the modem or data set.

MCR(1): When MCR(1) is set high, the $\overline{RTS}$ output is forced low. When MCR(1) is reset low, the $\overline{RTS}$ output is forced high. The $\overline{RTS}$ output of the 82C50A may be input into an EIA inverting line driver as the 1488 to obtain the proper polarity input at the modem or data set.

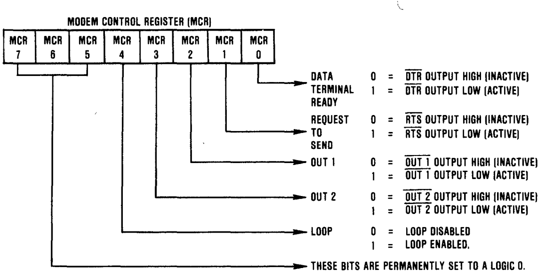
MCR(2): When MCR(2) is set high, the $\overline{\text{OUT1}}$ output is forced low. When MCR(2) is reset low, the $\overline{\text{OUT1}}$ output is forced high. $\overline{\text{OUT1}}$ is an user designated output.

MCR(3): When MCR(3) is set high, the $\overline{\text{OUT2}}$ output is forced low. When MCR(3) is reset low, the $\overline{\text{OUT2}}$ output is forced high. $\overline{\text{OUT2}}$ is an user designated output.

MCR(4): MCR(4) provides a local loopback feature for diagnostic testing of the 82C50A. When MCR(4) is set high, Serial Output (SOUT) is set to the marking (logic 1) state, and the receiver data input Serial Input (SIN) is disconnected. The output of the Transmitter Shift Register is looped back into the Receiver Shift Register input. The four modem control inputs ($\overline{\text{CTS}}$, $\overline{\text{DSR}}$, DC, and $\overline{\text{RI}}$) are disconnected. The four modem control outputs ($\overline{\text{DTR}}$, RTS, $\overline{\text{OUT1}}$ and $\overline{\text{OUT2}}$) are internally connected to the four modem control inputs. The modem control output pins are forced to their inactive state (high). In the diagnostic mode, data transmitted is immediately received. This allows the processor to verify the transmit and receive data paths of the 82C50A.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational, but the interrupt sources are now the lower four bits of the MCR instead of the four modem control inputs. The interrupts are still controlled by the Interrupt Enable Register.

MCR(5) - MCR(7): These bits are permanently set to logic 0.



Modem Status Register (MSR)

The MSR provides the CPU with status of the modem input lines from the modem or peripheral device. The MSR allows the CPU to read the modem signal inputs by accessing the data bus interface of the 82C50A. In addition to the current status information, four bits of the MSR indicate whether the modem inputs have changed since the last reading of the MSR. The delta status bits are set high when a control input from the modem changes state, and reset low when the CPU reads the MSR.

The modem input lines are $\overline{\text{CTS}}$ (pin 36), $\overline{\text{DSR}}$ (pin 37), $\overline{\text{RI}}$ (pin 39), and $\overline{\text{DCD}}$ (pin 38). MSR(4) - MSR(7) are status indications of these lines. The status indications follow the status of the input lines. If the modem status interrupt in the Interrupt Enable Register is enabled (IER(3)), a change of state in a modem input signals will be reflected by the modem status bits in the IIR register, and an interrupt (INTRPT) is generated. The MSR is a priority 4 interrupt. The contents of the Modem Status Register are described below:

Note that the state (high or low) of the status bits are inverted versions of the actual input pins.

MSR Bits 0 thru 7

MSR BIT	MNEMONIC	DESCRIPTION
MSR (1)	DDSR	Delta Data Set Ready
MSR (2)	TERI	Trailing Edge of Ring Indicator
MSR (0)	DCTS	Delta Clear To Send
MSR (3)	DDCD	Delta Data Carrier Detect
MSR (4)	CTS	Clear To Send
MSR (5)	DSR	Data Set Ready
MSR (6)	RI	Ring Indicator
MSR (7)	DCD	Data Carrier Detect

MSR(0) Delta Clear to Send (DCTS): DCTS indicates that the $\overline{\text{CTS}}$ input (Pin-36) to the 82C50A has changed state since the last time it was read by the CPU.

MSR(1) Delta Data Set Ready (DDSR): DDSR indicates that the $\overline{\text{DSR}}$ input (Pin-37) to the 82C50A has changed state since the last time it was read by the CPU.

MSR(2) Trailing Edge of Ring Indicator (TERI): TERI indicates that the $\overline{\text{RI}}$ input (Pin-39) to the 82C50A has changed state from high to low since the last time it was read by the CPU. Low to high transitions on $\overline{\text{RI}}$ do not activate TERI.

MSR(3) Delta Data Carrier Detect (DDCD): DDCD indicates that the $\overline{\text{DCD}}$ input (Pin-38) to the 82C50A has changed state since the last time it was read by the CPU.

MSR(4) Clear to Send (CTS): Clear to Send (CTS) is the status of the $\overline{\text{CTS}}$ input (Pin-36) from the modem indicating to the 82C50A that the modem is ready to receive data from the 82C50A transmitter output (SOUT). If the 82C50A is in the loop mode (MCR(4)=1), MSR(4) is equivalent to RTS in the MCR.

MSR(5) Data Set Ready (DSR): Data Set Ready (DSR) is a status of the $\overline{\text{DSR}}$ input (Pin-37) from the modem to the 82C50A which indicates that the modem is ready to provide received data to the 82C50A receiver circuitry. If the 82C50A is in the loop mode (MCR(4)=1), MSR(5) is equivalent to DTR in the MCR.

MSR(6) Ring Indicator MSR(6): Indicates the status of the RI input (Pin-39). If the 82C50A is in the loop mode (MCR(4)=1), MSR(6) is equivalent to OUT1 in the MCR.

MSR(7) Data Carrier Detect (MSR(7)): Data Carrier Detect indicates the status of the Data Carrier Detect (DCD) input (Pin-38). If the 82C50A is in the loop mode (MCR(4)=1), MSR(4) is equivalent to OUT2 of the MCR.

The modem status inputs (RI, DCD, DSR and CTS) reflect the modem input lines with any change of status. **Reading the MSR register will clear the delta modem status indications but has no effect on the status bits.** The status bits reflect the state of the input pins regardless of the mask control signals. If a DCTS, DDSR, TERI, or DDCD are true and a state change occurs during a read operation (DISTR, $\overline{DISTR}$), the state change is not indicated in the MSR. If DCTS, DDSR, TERI, or DDCD are false and a state change occurs during a read operation, the state change is indicated after the read operation.

For LSR and MSR, the setting of status bits is inhibited during status register read (DISTR, $\overline{DISTR}$) operations. If a status condition is generated during a read (DISTR, $\overline{DISTR}$) operation, the status bit is not set until the trailing edge of the read (DISTR, $\overline{DISTR}$).

If a status bit is set during a read (DISTR, $\overline{DISTR}$) operation, and the same status condition occurs, that status bit will be cleared at the trailing edge of the read (DISTR, $\overline{DISTR}$) instead of being set again.

Baud Rate Select Register (BRSR)

The 82C50A contains a programmable Baud Rate Generator (BRG) that divides the clock (DC to 10 MHz) by any divisor from 1 to 2^{16}-1 (see also BRG description). The output frequency of the Baud Generator is 16X the data rate [divisor # = frequency input ÷ (baud rate x 16)]. **Two 8-bit divisor latch registers store the divisor in a 16 bit binary format.** These Divisor Latch registers must be loaded during initialization. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Sample Divisor Number Calculation:

Given: Desired Baud Rate 1200 Baud

Frequency Input 1.8432 MHz

Formula: Divisor # = Frequency Input ÷ (Baud Rate x 16)

Divisor # = 1843200 ÷ (1200 x 16)

Answer: Divisor # = 96 = 60_{HEX} ➔ DLL = 01100000
DLM = 00000000

Check: The Divisor # 96 will divide the input frequency 1.8432 MHz down to 19200 which is 16 times the desired baud rate.

Divisor Latch Least Significant BYTE

DLL (0)	Bit 0
DLL (1)	Bit 1
DLL (2)	Bit 2
DLL (3)	Bit 3
DLL (4)	Bit 4
DLL (5)	Bit 5
DLL (6)	Bit 6
DLL (7)	Bit 7

Divisor Latch Most Significant BYTE

DLM (0)	Bit 8
DLM (1)	Bit 9
DLM (2)	Bit 10
DLM (3)	Bit 11
DLM (4)	Bit 12
DLM (5)	Bit 13
DLM (6)	Bit 14
DLM (7)	Bit 15

Receiver Buffer Register (RBR)

The receiver circuitry in the 82C50A is programmable for 5, 6, 7 or 8 data bits per character. For words of less than 8 bits, the data is right justified to the least significant bit (LSB = Data Bit 0 (RBR (0)). Data Bit 0 of a data word (RBR (0)) is the first data bit received. The unused bits in a character less than 8 bits are output low to the parallel output by the 82C50A.

Received data at the SIN input pin is shifted into the Receiver Shift Register by the 16X clock provided at the RCLK input. This clock is synchronized to the incoming data based on the position of the start bit. When a complete character is shifted into the Receiver Shift Register, the assembled data bits are parallel loaded into the Receiver Buffer Register. The DR flag in the LSR register is set.

Double buffering of the received data permits continuous reception of data without losing received data. While the Receiver Shift Register is shifting a new character into the 82C50A, the Receiver Buffer Register is holding a previously received character for the CPU to read. Failure to read the data in the RBR before complete reception of the next character result in the loss of the data in the Receiver Register. The OE flag in the LSR register indicates the overrun condition.

RBR Bits 0 thru 7

RBR (0)	Data Bit 0
RBR (1)	Data Bit 1
RBR (2)	Data Bit 2
RBR (3)	Data Bit 3
RBR (4)	Data Bit 4
RBR (5)	Data Bit 5
RBR (6)	Data Bit 6
RBR (7)	Data Bit 7

Transmitter Holding Register (THR)

The Transmitter Holding Register (THR) holds parallel data from the data bus (D0-D7) until the Transmitter Shift Register is empty and ready to accept a new character for transmission. The transmitter and receiver word length and number of stop bits are the same. If the character is less than eight bits, unused bits at the microprocessor data bus are ignored by the transmitter.

Data Bit 0 (THR (0)) is the first serial data bit transmitted. The THRE flag (LSR (5)) reflect the status of the THR. The TEMT flag (LSR (5)) indicates if both the THR and TSR are empty.

THR Bits 0 thru 7

THR (0)	Data Bit 0
THR (1)	Data Bit 1
THR (2)	Data Bit 2
THR (3)	Data Bit 3
THR (4)	Data Bit 4
THR (5)	Data Bit 5
THR (6)	Data Bit 6
THR (7)	Data Bit 7

Scratchpad Register (SCR)

This 8-bit Read/Write register has no effect on the 82C50A. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

SCR Bits 0 thru 7

SCR (0)	Data Bit 0
SCR (1)	Data Bit 1
SCR (2)	Data Bit 2
SCR (3)	Data Bit 3
SCR (4)	Data Bit 4
SCR (5)	Data Bit 5
SCR (6)	Data Bit 6
SCR (7)	Data Bit 7

Interrupt Structure

Interrupt Identification Register (IIR)

The 82C50A has interrupt capability for interfacing to current microprocessors. In order to minimize software overhead during data character transfers, the 82C50A prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows:

1. Receiver Line Status (priority 1)
2. Received Data Ready (priority 2)
3. Transmitter Holding Register Empty (priority 3)
4. Modem Status (priority 4).

Information indicating that a prioritized interrupt is pending and the type of interrupt is stored in the Interrupt Identification Register (IIR). When addressed during chip select time, the IIR indicates the highest priority interrupt pending. No other interrupts are acknowledged until the interrupt is serviced by the CPU. The contents of the IIR are indicated in Table 2 and are described below.

IIR(0): IIR(0) can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When IIR(0) is low, an interrupt is pending, and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When IIR(0) is high, no interrupt is pending.

IIR(1) and IIR(2): IIR(1) and IIR(2) are used to identify the highest priority interrupt pending as indicated in Table 2.

IIR(3) - IIR(7): These five bits of the IIR are logic 0.

Interrupt Enable Register (IER)

The Interrupt Enable Register (IER) is a Write register used to independently enable the four 82C50A interrupts which activate the interrupt (INTRPT) output. All interrupts are disabled by resetting IER(0) - IER(3) of

TABLE 2. INTERRUPT IDENTIFICATION REGISTER

INTERRUPT IDENTIFICATION				INTERRUPT SET AND RESET FUNCTIONS		
BIT 2	**BIT 1**	**BIT 0**	**PRIORITY LEVEL**	**INTERRUPT FLAG**	**INTERRUPT SOURCE**	**INTERRUPT RESET CONTROL**
X	X	1		None	None	
1	1	0	First	Receiver Line Status	OE, PE, FE, or BI	LSR Read
1	0	0	Second	Received Data Available	Receiver Data Available	RBR Read
0	1	0	Third	THRE	THRE	IIR Read if THRE is the interrupt source or THR Write
0	0	0	Fourth	Modem Status	$\overline{CTS}$, $\overline{DSR}$ $\overline{RI}$, $\overline{DCD}$	MSR Read

X = Not Defined, May Be 0 or 1

the Interrupt Enable Register. Interrupts are enabled by setting the appropriate bits of the IER high. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers. The contents of the Interrupt Enable Register are indicated in Table 3 and are described below.

IER(0): When programmed high (IER(0)=Logic 1), IER(0) enables Received Data Available interrupt.

IER(1): When programmed high (IER(1)=Logic 1), IER(1) enables the Transmitter Holding Register Empty interrupt.

IER(2): When programmed high (IER(2)=Logic 1), IER(2) enables the Receiver Line Status interrupt.

IER(3): When programmed high (IER(3)=Logic 1), IER (3) enables the Modem Status interrupt.

IER(4) - IER(7): These four bits of the IER are logic 0.

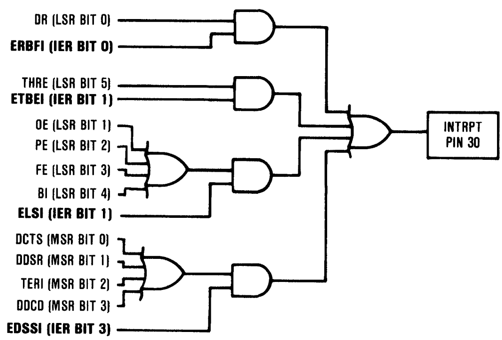


FIGURE 1. 82C50A INTERRUPT CONTROL STRUCTURE

TABLE 3. 82C50A ACCESSIBLE REGISTER SUMMARY

(NOTE: See Table 1 for how to access these registers).

REGISTER MNEMONIC	REGISTER BIT NUMBER							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RBR (Read Only)	Data Bit 7 (MSB)	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)*
THR (Write Only)	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
IER	0	0	0	0	(EDSSI) Enable Modem Status Interrupt	(ELSI) Enable Receiver Line Status Interrupt	(ETBEI) Enable Transmitter Holding Register Empty Interrupt	(ERBFI) Enable Received Data Available Interrupt
IIR (Read Only)	0	0	0	0	0	Interrupt ID Bit (1)	Interrupt ID Bit (0)	"0" 1F Interrupt Pending
LCR	(DLAB) Divisor Latch Access Bit	Set Break	Stick Parity	(EPS) Even Parity Select	(PEN) Parity Enable	(STB) Number of Stop Bits	(WLSB1) Word Length Select Bit 1	(WLSB0) Word Length Select Bit 0
MCR	0	0	0	Loop	Out 2	Out 1	(RTS) Request To Send	(DTR) Data Terminal Ready
LSR	0	(TEMT) Transmitter Empty	(THRE) Transmitter Holding Register Empty	(BI) Break Interrupt	(FE) Framing Error	(PE) Parity Error	(OE) Overrun Error	(DR) Data Ready
MSR	(DCD) Data Carrier Detect	(RI) Ring Indicator	(DSR) Data Set Ready	(CTS) Clear to Send	(DDCD) Delta Data Carrier Detect	(TERI) Trailing Edge Ring Indicator	(DDSR) Delta Data Set Ready	(DCTS) Delta Clear to Send
SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

* LSB, Data Bit 0 is the first bit transmitted or received.

Transmitter

The serial transmitter section consists of a Transmitter Holding Register (THR), Transmitter Shift Register (TSR), and associated control logic. The Transmitter Holding Register Empty (THRE) and Transmitter Shift Register Empty (TEMT) are two bits in the Line Status Register which indicate the status of THR and TSR. To transmit a 5-8 bit word, the word is written through D0-D7 to the THR. The microprocessor should perform a write operation only if THRE is high. The THRE is set high when the word is automatically transferred from the THR to the TSR during the transmission of the start bit.

When the transmitter is idle, both THRE and TEMT are high. The first word written causes THRE to be reset to 0. After completion of the transfer, THRE returns high. TEMT remains low for at least the duration of the transmission of the data word. If a second character is transmitted to the THR, the THRE is reset low. Since the data word cannot be transferred from the THR to the TSR until the TSR is empty, THRE remains low until the TSR has completed transmission of the word. When the last word has been transmitted out of the TSR, TEMT is set high. THRE is set high one THR to TSR transfer time later.

Receiver

Serial asynchronous data is input into the SIN pin. The idle state of the line providing the input into SIN is high. A start bit detect circuit continually searches for a high to low transition from the idle state. When the transition is detected, a counter is reset, and counts the 16X clock to 7 1/2, which is the center of the start bit. The start bit is valid if the SIN is still low at the mid bit sample of the start bit. Verifying the start bit prevents the receiver from assembling an incorrect data character due to a low going noise spike on the SIN input.

The Line Control Register determines the number of data bits in a character (LCR(0), LCR(1)), number of stop bits LCR(2), if parity is used LCR(3), and the polarity of parity LCR(4). Status information for the receiver is provided in the Line Status Register. When a character is transferred from the Receiver Shift Register to the Receiver Buffer Register, the Data Received indication in LSR(0) is set high. The CPU reads the Reciver Buffer Register through D0-D7. This read resets LSR(0). If D0-D7 are not read prior to a new character transfer from the RSR to the RBR, the overrun error status indication is set in LSR(1). The parity check tests for even or odd parity on the parity bit, which precedes the first stop bit. If there is a parity error, the parity error is set in LSR(2). There is circuitry which tests whether the stop bit is high. If it is not, a framing error indication is generated in LSR(3).

The center of the start bit is defined as clock count 7 1/2. If the data into SIN is a symmetrical square wave, the center of the data cells will occur within ± 3.125% of the actual center, providing an error margin of 46.875%. The start bit can begin as much as one 16X clock cycle prior to being detected.

Baud Rate Generator (BRG)

The BRG generates the clocking for the UART function, providing standard ANSI/CCITT bit rates. The oscillator driving the BRG may be provided either with the addition of an external crystal to the XTAL1 and XTAL2 inputs, or an external clock into XTAL1. In either case, a buffered clock output, $\overline{\text{BAUDOUT}}$, is provided for other system clocking. If two 82C50As are used on the same board, one can use a crystal, and the buffered clock output can be routed directly into the XTAL1 of the second 82C50A.

The data rate is determined by the Divisor Latch registers DLL and DLM and the external frequency or crystal input, with the $\overline{\text{BAUDOUT}}$ providing an output 16X the data rate. The bit rate is selected by programming the two divisor latches, Divisor Latch Most Significant Byte and Divisor Latch Least Significant Byte. Setting DLL=1 and DLM=0 selects the divisor to divide by 1 (divide by 1 gives maximum baud rate for a given input frequency at XTAL 1). The on-chip oscillator is optimized for a 10 MHz crystal. Usually, higher frequency are less expensive than lower frequency crystals.

The BRG can use any of three different popular crystals to provide standard baud rates. The frequency of these three common crystals on the market are l.8432 MHz, 2.4576 MHz, and 3.072 MHz. With these standard crystals, standard bit rates from 50 to 38.5 kbps are available. The following tables illustrate the divisors needed to obtain standard rates using these three crystal frequencies.

TABLE 4. BAUD RATES USING 1.8432 MHz CRYSTAL

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 x CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED & ACTUAL
50	2304	-
75	1536	-
110	1047	0.026
134.5	857	0.058
150	768	-
300	384	-
600	192	-
1200	96	-
1800	64	-
2000	58	0.69
2400	48	-
3600	32	-
4800	24	-
7200	16	-
9600	12	-
19200	6	-
38400	3	-
56000	2	2.86

TABLE 5. BAUD RATES USING 2.4576 MHz CRYSTAL

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 x CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED & ACTUAL
50	3072	-
75	2048	-
110	1396	0.026
134.5	1142	0.0007
150	1024	-
300	512	-
600	256	-
1200	128	-
1800	85	0.392
2000	77	0.260
2400	64	-
3600	43	0.775
4800	32	-
7200	21	1.587
9600	16	-
19200	8	-
38400	4	-

TABLE 6. BAUD RATES USING 3.072 MHz Crystal

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 x CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED & ACTUAL
50	3840	-
75	2560	-
110	1745	0.026
134.5	1428	0.034
150	1280	-
300	640	-
600	320	-
1200	160	-
1800	107	0.312
2000	96	-
2400	80	-
3600	53	0.628
4800	40	-
7200	27	1.23
9600	20	-
19200	10	-
38400	5	-

Reset

After powerup, the 82C50A Master Reset schmitt trigger input (MR) should be held high for TMRW ns to reset the 82C50A circuits to an idle mode until initialization. A high on MR causes the following:

1. Initializes the transmitter and receiver internal clock counters.

2. Clears the Line Status Register (LSR), except for Transmitter Shift Register Empty (TEMT) and Transmit Holding Register Empty (THRE), which are set. The Modem Control Register (MCR) is also cleared. All of the discrete lines, memory elements and miscellaneous logic associated with these register bits are also cleared or turned off. The Line Control Register (LCR), Divisor Latches, Receiver Buffer Register, Transmitter Buffer Register are not effected.

Following removal of the reset condition (MR low), the 82C50A remains in the idle mode until programmed.

A hardware reset of the 82C50A sets the THRE and TEMT status bit in the LSR. When interrupts are subsequently enabled, an interrupt occurs due to THRE.

A summary of the effect of a Master Reset on the 82C50A is given in Table 7.

TABLE 7. 82C50A RESET OPERATIONS

REGISTER/SIGNAL	RESET CONTROL	RESET
Interrupt Enable Register	Master Reset	All Bits Low (0-3 forced and 4-7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High, Bits 1 and 2 Low Bits 3-7 are Permanently Low
Line Control Register	Master Reset	All Bits Low
MODEM Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	All Bits Low, Except Bits 5 and 6 are High
MODEM Status Register	Master Reset	Bit 0-3 Low Bits 4-7 Input Signal
SOUT	Master Reset	High
Intrpt (RCVR Errs)	Read LSR/MR	Low
Intrpt (RCVR Data Ready)	Read RBR/MR	Low
Intrpt (THRE)	Read IIR/Write THR/MR	Low
Intrpt (Modem Status Changes)	Read MSR/MR	Low
$\overline{\text{Out2}}$	Master Reset	High
$\overline{\text{RTS}}$	Master Reset	High
$\overline{\text{DTR}}$	Master Reset	High
$\overline{\text{Out1}}$	Master Reset	High

Programming

The 82C50A is programmed by the control registers LCR, IER, DLL and DLM, and MCR. These control words define the character length, number of stop bits, parity, baud rate, and modem interface.

While the control registers can be written in any order, the IER should be written to last because it controls the interrupt enables. Once the 82C50A is programmed and operational, these registers can be updated any time the 82C50A is not transmitting or receiving data.

The control signals required to access 82C50A internal registers are shown below.

Software Reset

A software reset of the 82C50A is a useful method for returning to a completely known state without a system reset. Such a reset consists of writing to the LCR, Divisor Latches, and MCR registers. The LSR and RBR registers should be read prior to enabling interrupts in order to clear out any residual data or status bits which may be invalid for subsequent operation.

Crystal Operation

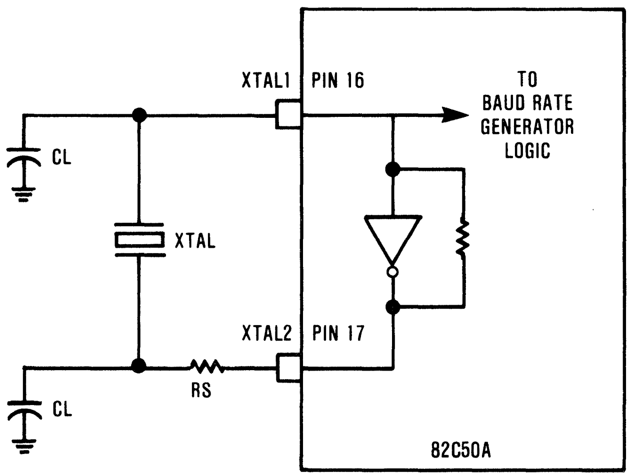
The 82C50A crystal oscillator circuitry is designed to operate with a fundamental mode, parallel resonant crystal. Table 8 shows the required crystal parameters and crystal circuit configuration, respectively.

When using an external clock source, the XTAL1 input is driven and the XTAL2 output is left open. Power consumption when using an external clock is typically 50% of that required when using a crystal. This is due to the sinusoidal nature of the drive circuitry when using a crystal.

The maximum frequency of the the 82C50A is 10 MHz with an external clock or a crystal attached to XTAL1 and XTAL2. Using the external clock or crystal, and a divide by one divisor, the maximum $\overline{\text{BAUDOUT}}$ is 10 MHz, and the maximum data rate is 625 Kbps.

TABLE 8. TYPICAL CRYSTAL OSCILLATOR CIRCUIT

PARAMETER	
Frequency	1.0 to 10 MHz
Type of Operation	Parallel resonant, Fundamental mode
Load Capacitance(CL)	20 or 32 pF (typ)
R_{series} (Max)	100 ohms (f=10 MHz, CL=32 pF)
	200 ohms (f=10 MHz, CL=20 pF)



Absolute Maximum Ratings

Supply Voltage .... +8.0 Volts
Input, Output or I/O Voltage Applied .... GND -0.5V to VCC +0.5V
Storage Temperature Range .... -65°C to +150°C
Maximum Package Power Dissipation .... 1 Watt
θ_{jc} .... 12°C/W (CERDIP Package), 17°C/W (LCC Package)
θ_{ja} .... 36°C/W (CERDIP Package), 41°C/W (LCC Package)
Gate Count .... 1788 Gates
Junction Temperature .... +150°C
Lead Temperature (Soldering, Ten Seconds) .... +260°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +4.5V to +5.5V
Operating Temperature Range
C82C50A .... 0°C to +70°C
I82C50A .... -40°C to +85°C
M82C50A .... -55°C to +125°C

D.C. Electrical Specifications

VCC = 5.0V ± 10%
T_A = 0°C to +70°C (C82C50A), T_A = -40°C to +85°C (I82C50A)
T_A = -55°C to +125°C (M82C50A)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	Logical One Input Voltage	2.0 2.2		V V	I82C50A, C82C50A M82C50A
VIL	Logical Zero Input Voltage		0.8	V	
VTH	Schmitt Trigger Logic One Input Voltage	2.0 2.2		V V	MR Input I82C50A, C82C50A M82C50A
VTL	Schmitt Trigger Logic Zero Input Voltage		0.8	V	MR Input
VIH(CLK)	Logical One Clock Voltage	VCC-0.8		V	External Clock
VIL(CLK)	Logical Zero Clock Voltage		0.8	V	External Clock
VOH	Output High Voltage	3.0 VCC-0.4		V V	IOH = -2.5mA IOH = -100μA
VOL	Output Low Voltage		0.4	V	IOL = +2.5mA,
II	Input Leakage Current	-1.0	+1.0	μA	VIN = GND or VCC, DIP Pins 9, 10, 12, 13, 14, 18, 19, 21, 22, 25-28, 35-39
IO	Input/Output Leakage Current	-10.0	+10.0	μA	VO = GND or VCC, DIP Pins 1-8
ICCOP	Operating Power Supply Current		6	mA	External Clock F = 2.4576MHz, VCC = 5.5V, VIN = VCC or GND, Outputs Open
ICCSB	Standby Supply Current		100	μA	VCC = 5.5V, VIN = VCC or GND, Outputs Open

Capacitance

T_A = 25°C; VCC = GND = 0V; VIN = +5V or GND

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
CIN	Input Capacitance	15	pF	FREQ = 1MHz, Unmeasured pins returned to GND
COUT	Output Capacitance	15	pF	
CI/O	I/O Capacitance	20	pF	

A.C. Specifications

VCC = 5.0V ± 10%
T_A = 0°C to +70°C (C82C50A)
T_A = -40°C to +85°C (I82C50A)
T_A = -55°C to +125°C (M82C50A)

Timing Requirements

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
T_{AW}	Address Strobe Width	50		ns	
T_{AS}	Address Setup Time	60		ns	Note 1
T_{AH}	Address Hold Time	0		ns	
T_{CS}	Chip Select Setup Time	60		ns	Note 1
T_{CH}	Chip Select Hold Time	0		ns	
T_{DIW}	DISTR $\overline{DISTR}$ Strobe Width	150		ns	
T_{RC}	Read Cycle Delay	270		ns	Note 1
R_C	Read Cycle = TAR +TDIW +TRC	500		ns	
T_{DD}	DISTR $\overline{DISTR}$ to Driver Disable Delay		75	ns	
T_{DDD}	Delay From DISTR $\overline{DISTR}$ to Data		120	ns	
T_{HZ}	DISTR $\overline{DISTR}$ to Floating Data Delay	10	75	ns	
T_{DOW}	DOSTR $\overline{DOSTR}$ Strobe Width	150		ns	
T_{WC}	Write Cycle Delay	270		ns	Note 1
W_C	Write Cycle = TAW+TDOW+TWC	500		ns	
T_{DS}	Data Setup Time	90		ns	
T_{DH}	Data Hold Time	60		ns	

NOTE 1: "When using the 82C50A in the multiplexed mode ($\overline{ADS}$ operational), it will operate in 80C86/88 systems with a maximum 3 MHz operating frequency."

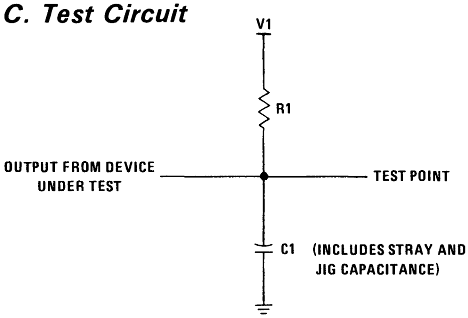
A.C. Specifications

Timing

VCC = 5.0V ± 10%
T_A = 0°C to +70°C (C82C50A)
T_A = -40°C to +85°C (I82C50A)
T_A = -55°C to +125°C (M82C50A)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
DEMULTIPLEXED OPERATION					
T_{CSC}	Chip Select Output Delay from Select		125	ns	
T_{RA}	Address Hold Time from DISTR $\overline{DISTR}$	20		ns	
T_{RCS}	Chip Select Hold Time from DISTR $\overline{DISTR}$	20		ns	
T_{AR}	DISTR $\overline{DISTR}$ Delay from Address	80		ns	
T_{CSR}	DISTR $\overline{DISTR}$ Delay from Chip Select	80		ns	
T_{WA}	Address Hold Time from DOSTR $\overline{DOSTR}$	20		ns	
T_{WCS}	Chip Select Hold Time from DOSTR $\overline{DOSTR}$	20		ns	
T_{AW}	DOSTR $\overline{DOSTR}$ Delay from Address	80		ns	
T_{CSW}	DOSTR $\overline{DOSTR}$ Delay from Select	80		ns	
T_{MRW}	Master Reset Pulse Width	500		ns	
T_{XH}	Duration of Clock High Pulse	40			
T_{XL}	Duration of Clock Low Pulse	40		ns	
BAUD GENERATOR					
N	Baud Divisor	1	$2^{16}-1$		
T_{BLD}	Baud Output Negative Edge Delay		250	ns	
T_{BHD}	Baud Output Positive Edge Delay		250	ns	
T_{LW}	Baud Output Down Time	40		ns	
T_{HW}	Baud Output Up Time	40		ns	
RECEIVER					
T_{SCD}	Delay from RCLK to Sample Time		250	ns	
T_{SINT}	Delay from Stop to Set Interrupt	1	1	$\overline{BAUDOUT}$ Cycles	
T_{RINT}	Delay from DISTR $\overline{DISTR}$ (RD RBR) to Reset Interrupt		250	ns	
TRANSMITTER					
T_{HR}	Delay from DOSTR $\overline{DOSTR}$ to Reset Interrupt		250	ns	
T_{IRS}	Delay from Initial INTR Reset to Transmit Start	8	24	$\overline{BAUDOUT}$ Cycles	
T_{SI}	Delay from Initial Write to Interrupt	16	32	$\overline{BAUDOUT}$ Cycles	
T_{STI}	Delay from Stop to Interrupt (THRE)	8	24	$\overline{BAUDOUT}$ Cycles	
T_{IR}	Delay from DISTR $\overline{DISTR}$ (RD IIR) to Reset Interrupt (THRE)		250	ns	
MODEM CONTROL					
T_{MDO}	Delay from DOSTR $\overline{DOSTR}$ to Output		500	ns	
T_{SIM}	Delay to Set Interrupt from Modem Input		500	ns	
T_{RIM}	Delay to Reset Interrupt from DISTR $\overline{DISTR}$ (RD MSR)		500	ns	

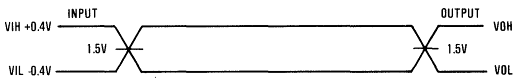
A. C. Test Circuit



IOH	IOL	V1	R1	C1
-2.5mA	+2.5mA	1.7V	520Ω	100 pF

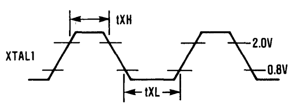
TEST CONDITION DEFINITION TABLE

A.C. Testing Input, Output Waveforms

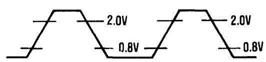


A.C. Testing: All input signals must switch between VIL -0.4V and VIH +0.4V. Input rise and fall times are driven at 1nsec per volt.

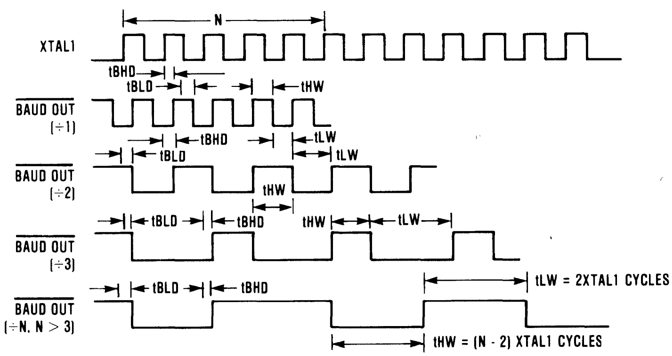
Timing Waveforms



EXTERNAL CLOCK INPUT

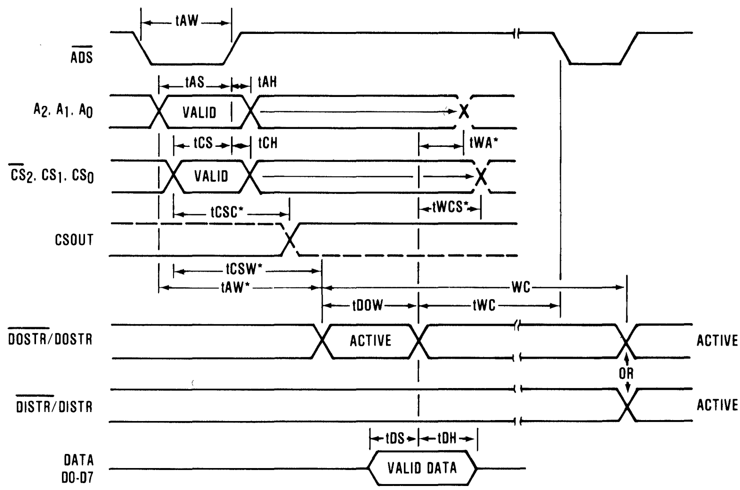


AC TEST POINTS



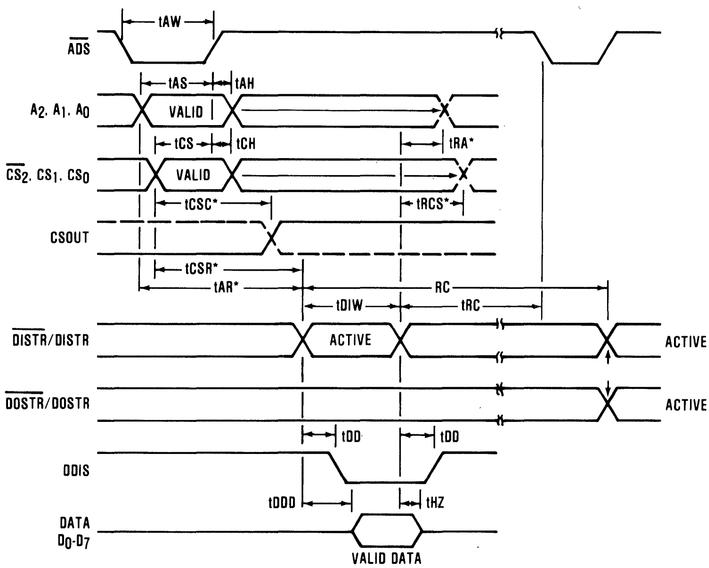
BAUDOUT TIMING

Timing Waveforms



*Applicable only when ADS is low.

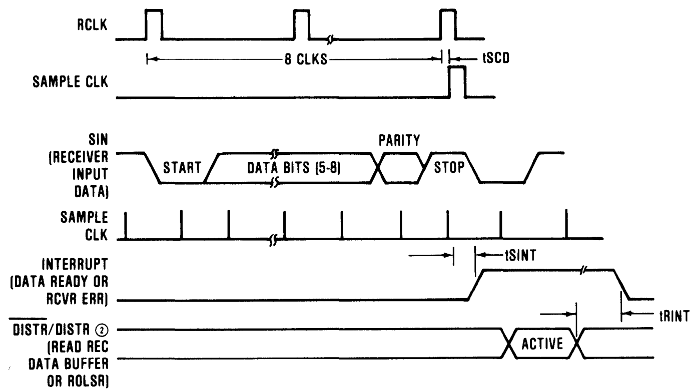
WRITE CYCLE



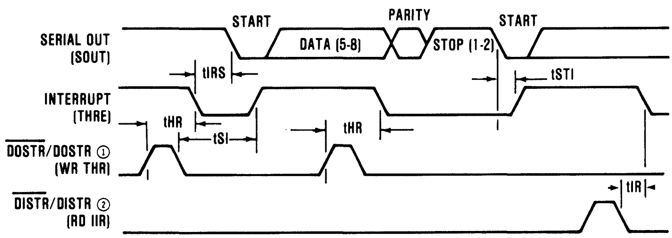
*Applicable only when ADS is low.

READ CYCLE

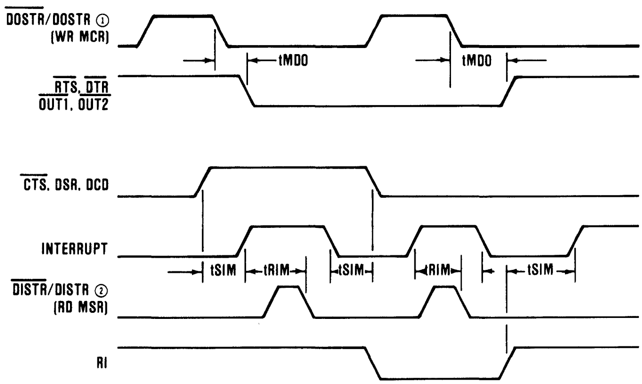
Timing Waveforms



RECEIVER TIMING



TRANSMITTER TIMING



NOTE 1: See Write Cycle Timing
NOTE 2: See Read Cycle Timing

MODEM CONTROLS TIMING

HARRIS

82C52

CMOS Serial Controller Interface

REFERENCE PAGE 4-56 FOR
APPLICATION NOTE 108

Features

- SINGLE CHIP UART/BRG
- DC TO 16MHz OPERATION
- CRYSTAL OR EXTERNAL CLOCK INPUT
- ON CHIP BAUD RATE GENERATOR . . . 72 SELECTABLE BAUD RATES
- INTERRUPT MODE WITH MASK CAPABILITY
- MICROPROCESSOR BUS ORIENTED INTERFACE
- 80C86 COMPATIBLE
- SCALED SAJI IV CMOS PROCESS
- SINGLE 5V POWER SUPPLY
- LOW POWER – 1mA/MHz TYPICAL
- MODEM INTERFACE
- LINE BREAK GENERATION AND DETECTION
- LOOPBACK AND ECHO MODES

Description

The 82C52 is a high performance programmable Universal Asynchronous Receiver/Transmitter (UART) and Baud Rate Generator (BRG) on a single chip. Utilizing the Harris advanced Scaled SAJI IV CMOS process, the 82C52 will support data rates from D.C. to 1M baud asynchronously with a 16X clock (0-16 MHz clock frequency).

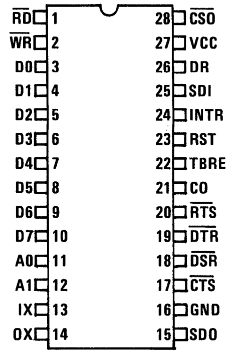
The on-chip Baud Rate Generator can be programmed for any one of 72 different baud rates using a single industry standard crystal or external frequency source. A unique pre-scale divide circuit has been designed to provide standard RS-232-C baud rates when using any one of three industry standard baud rate crystals (1.8432 MHz, 2.4576 MHz, or 3.072 MHz).

A programmable buffered clock output (CO) is available and can be programmed to provide either a buffered oscillator or 16X baud rate clock for general purpose system usage.

Inputs and outputs have been designed with full TTL/CMOS compatibility in order to facilitate mixed TTL/NMOS/CMOS system design.

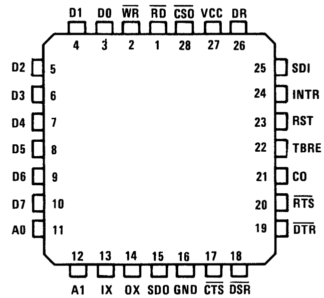
Pinouts

TOP VIEW

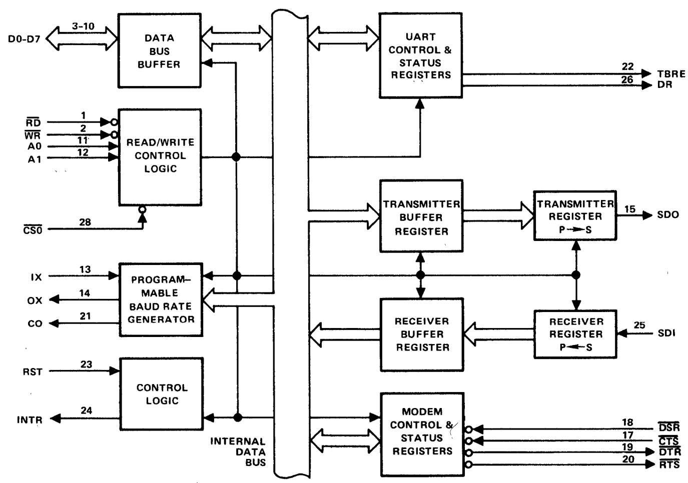


LCC/PLCC

TOP VIEW



Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Pin Description

SYMBOL	PIN NO.	TYPE	ACTIVE LEVEL	DESCRIPTION
$\overline{RD}$	1	I	Low	READ: The $\overline{RD}$ input causes the 82C52 to output data to the data bus (D0-D7). The data output depends upon the state of the address inputs (A0, A1). $\overline{CS0}$ enables the $\overline{RD}$ input.
$\overline{WR}$	2	I	Low	WRITE: The $\overline{WR}$ input causes data from the data bus (D0-D7) to be input to the 82C52. Addressing and chip select action is the same as for read operations.
D0-D7	3-10	I/O	High	DATA BITS 0-7: The Data Bus provides eight, 3-state input/output lines for the transfer of data, control and status information between the 82C52 and the CPU. For character formats of less than 8 bits, the corresponding D7, D6 and D5 are considered "don't cares" for data WRITE operations and are 0 for data READ operations. These lines are normally in a high impedance state except during read operations. D0 is the Least Significant Bit (LSB) and is the first serial data bit to be received or transmitted.
A0, A1	11, 12	I	High	ADDRESS INPUTS: The address lines select the various internal registers during CPU bus operations.
IX, OX	13, 14	I, O		CRYSTAL/CLOCK: Crystal connections for the internal Baud Rate Generator. IX can also be used as an external clock input in which case OX should be left open.
SDO	15	O	High	SERIAL DATA OUTPUT: Serial data output from the 82C52 transmitter circuitry. A Mark (1) is a logic one (high) and Space (0) is a logic zero (low). SD0 is held in the Mark condition when the transmitter is disabled when $\overline{CTS}$ is false, RST is true, when the Transmitter Register is empty, or when in the Loop Mode.
GND	16		Low	GROUND: Power supply ground connection.
$\overline{CTS}$	17	I	Low	CLEAR TO SEND: The logical state of the $\overline{CTS}$ line is reflected in the CTS bit of the Modem Status Register. Any change of state in $\overline{CTS}$ causes INTR to be set true when INTEN and MIEN are true. A false level on $\overline{CTS}$ will inhibit transmission of data on the SD0 output and will hold SD0 in the Mark (high) state. If CTS goes false during transmission, the current character being transmitted will be completed. $\overline{CTS}$ does not affect Loop Mode operation.
$\overline{DSR}$	18	I	Low	DATA SET READY: The logical state of the $\overline{DSR}$ line is reflected in the Modem Status Register. Any change of state of $\overline{DSR}$ will cause INTR to be set if INTEN and MIEN are true. The state of this signal does not affect any other circuitry within the 82C52.
$\overline{DTR}$	19	O	Low	DATA TERMINAL READY: The $\overline{DTR}$ signal can be set (low) by writing a logic 1 to the appropriate bit in the Modem Control Register (MCR). This signal is cleared (high) by writing a logic 0 to the $\overline{DTR}$ bit in the MCR or whenever a RST (high) is applied to the 82C52.
$\overline{RTS}$	20	O	Low	REQUEST TO SEND: The $\overline{RTS}$ signal can be set (low) by writing a logic 1 to the appropriate bit in the MCR. This signal is cleared (high) by writing a logic 0 to the $\overline{RTS}$ bit in the MCR or whenever a reset (RST = high) is applied to the 82C52.
CO	21	O		CLOCK OUT: This output is user programmable to provide either a buffered IX output or a buffered Baud Rate Generator (16x) clock output. The buffered IX (Crystal or external clock source) output is provided when the Baud Rate Select Register (BRSR) bit 7 is set to a zero. Writing a logic one to BRSR bit 7 causes the CO output to provide a buffered version of the internal Baud Rate Generator clock which operates at sixteen times the programmed baud rate.
TBRE	22	O	High	TRANSMITTER BUFFER REGISTER EMPTY: The TBRE output is set (high) whenever the Transmitter Buffer Register (TBR) has transferred its data to the Transmit Register. Application of a reset (RST) to the 82C52 will also set the TBRE output. TBRE is cleared (low) whenever data is written to the TBR.
RST	23	I	High	RESET: The RST input forces the 82C52 into an "Idle" mode in which all serial data activities are suspended. The Modem Control Register (MCR) along with its associated outputs are cleared. The UART Status Register (USR) is cleared except for the TBRE and TC bits, which are set. The 82C52 remains in an "Idle" state until programmed to resume serial data activities. The RST input is a Schmitt trigger input.
INTR	24	O	High	INTERRUPT REQUEST: The INTR output is enabled by the INTEN bit in the Modem Control Register (MCR). The MIEN bit selectively enables modem status changes to provide an input to the INTR logic. Figure 9 shows the overall relationship of these interrupt control signals.
SDI	25	I	High	SERIAL DATA INPUT: Serial data input to the 82C52 receiver circuits. A Mark (1) is high, and a Space (0) is low. Data inputs on SDI are disabled when operating in the loop mode or when RST is true.

Pin Description

SYMBOL	PIN NO.	TYPE	ACTIVE LEVEL	DESCRIPTION
DR	26	O	High	DATA READY: A true level indicates that a character has been received, transferred to the RBR and is ready for transfer to the CPU. DR is reset on a data READ of the Receiver Buffer Register (RBR) or when RST is true.
VCC	27		High	VCC: +5V positive power supply pin. A 0.1μA decoupling capacitor from VCC (Pin 27) to GND (Pin 16) is recommended.
$\overline{CS0}$	28	I	Low	CHIP SELECT: The chip select input acts as an enable signals for the $\overline{RD}$ and $\overline{WR}$ input signals.

RESET

During and after power-up, the 82C52 Reset input (RST) must be held high for at least two IX clock cycles in order to initialize and drive the 82C52 circuits to an idle mode until proper programming can be done. A high on RST causes the following events to occur:

- Resets the internal Baud Rate Generator (BRG) circuits clock counters and bit counters. The Baud Rate Select Register (BRSR) is not affected (except for bit 7 which is reset to 0).
- Clears the UART Status Register (USR) except for Transmission Complete (TC) and Transmit Buffer Register Empty (TBRE) which are set. The Modem Control Register (MCR) is also cleared. All of the discrete lines, memory elements and miscellaneous logic associated with these register bits are also cleared or turned off. Note that the UART Control Register (UCR) is not affected.

Following removal of the reset condition (RST = low), the 82C52 remains in the idle mode until programmed to its desired system configuration.

PROGRAMMING THE 82C52

The complete functional definition of the 82C52 is programmed by the systems software. A set of control words (UCR, BRSR and MCR) must be sent out by the CPU to initialize the 82C52 to support the desired communication format. These control words will program the character length, number of stop bits, even/odd/no parity, baud rate, etc. Once programmed, the 82C52 is ready to perform its communication functions.

The control registers can be written to in any order. However, the MCR should be written to last because it controls the interrupt enables, modem control outputs and the receiver enable bit. Once the 82C52 is programmed and operational, these registers can be updated any time the 82C52 is not immediately transmitting or receiving data.

Table 1 shows the control signals required to access 82C52 internal registers.

TABLE 1.

$\overline{CS0}$	A1	A0	$\overline{WR}$	$\overline{RD}$	OPERATION
0	0	0	0	1	Data Bus → Transmitter Buffer Register (TBR)
0	0	0	1	0	Receiver Buffer Register (RBR) → Data Bus
0	0	1	0	1	Data Bus → UART Control Register (UCR)
0	0	1	1	0	UART Status Register (USR) → Data Bus
0	1	0	0	1	Data Bus → Modem Control Register (MCR)
0	1	0	1	0	MCR → Data Bus
0	1	1	0	1	Data Bus → Bit Rate Select Register (BRSR)
0	1	1	1	0	Modem Status Register (MSR) → Data Bus

UART CONTROL REGISTER (UCR)

The UCR is a write only register which configures the UART transmitter and receiver circuits. Data bits D7 and D6 are not used but should always be set to a logic zero (0) in order to insure software compatibility with future product upgrades. During the Echo Mode, the transmitter always repeats the received word and parity, even when the UCR is programmed with different or no parity.

UCR

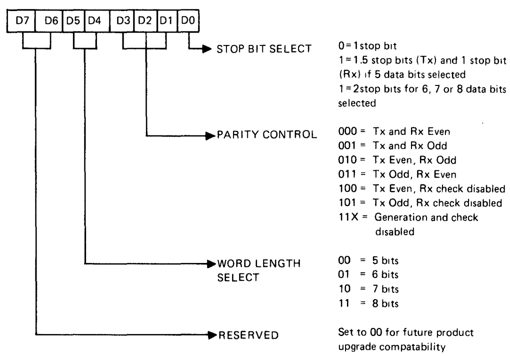


FIGURE 1.

BAUD RATE SELECT REGISTER (BRSR)

The 82C52 is designed to operate with a single crystal or external clock driving the IX input pin. The Baud Rate Select Register is used to select the divide ratio (one of 72) for the internal Baud Rate Generator circuitry. The internal circuitry is separated into two separate counters, a Prescaler and a Divisor Select. The Prescaler can be set to any one of four division rates, ÷1, ÷3, ÷4 or ÷5.

The Prescaler design has been optimized to provide standard baud rates using any one of three popular crystal frequencies. By using one of these common system clock frequencies, 1.8432 MHz, 2.4576 MHz or 3.072 MHz and Prescaler divide ratios of ÷3, ÷4, or ÷5 respectively, the Prescaler output will provide a constant 614.4 KHz. When this frequency is further divided by the Divisor Select counter, any of the standard baud rates from 50 Baud to 38.4 KBaud can be selected (see Table 2). Non-standard baud rates up to 1 Mbaud can be selected by using different input frequencies (crystal or an external frequency input up to 16 MHz) and/or different Prescaler and Divisor Select ratios.

Regardless of the baud rate, the baud rate generator provides a clock which is 16 times the desired baud rate. For example, in order to operate at a 1 Mbaud data rate, a 16 MHz crystal, a Prescale rate of ÷1, and a Divisor Select rate of "external" would be used. This would provide a 16 MHz clock as the output of the Baud Rate Generator to the Transmitter and Receiver circuits.

The CO select bit in the BRSR selects whether a buffered version of the external frequency input (IX input) or the Baud Rate Generator output (16x baud rate clock) will be output on the CO output (pin 21). The Baud Rate Generator output will always be a 50% nominal duty cycle except when "external" is selected and the Prescaler is set to ÷3 or ÷5.

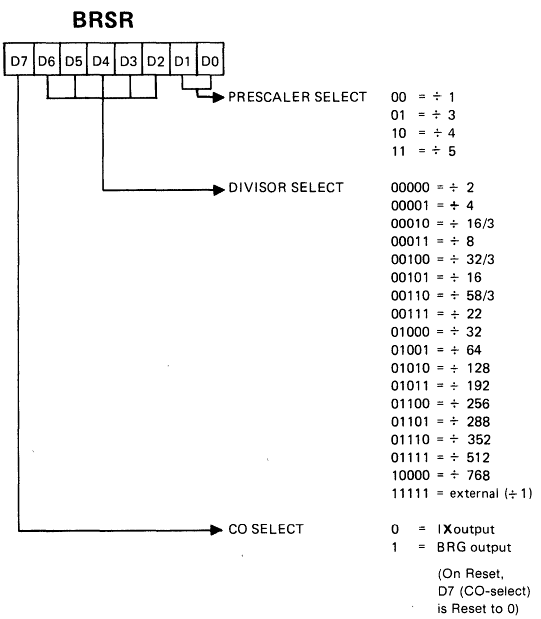


FIGURE 2.

TABLE 2.

BAUD RATE	DIVISOR
38.4K	external
19.2K	2
9600	4
7200	16/3
4800	8
3600	32/3
2400	16
2000*	58/3
1800	21
1200	32
600	64
300	128
200	192
150	256
134.5*	288
110*	352
75	512
50	768

Note: These baud rates are based upon the following input frequency/Prescale divisor combinations.
1.8432 MHz and Prescale = ÷3
2.4576 MHz and Prescale = ÷4
3.072 MHz and Prescale = ÷5

*All baud rates are exact except for:

BAUD RATE	ACTUAL	PERCENT ERROR
1800	1828.3	1.59%
2000	1986.2	0.69%
134.5	133.33	0.87%
110	109.71	0.26%

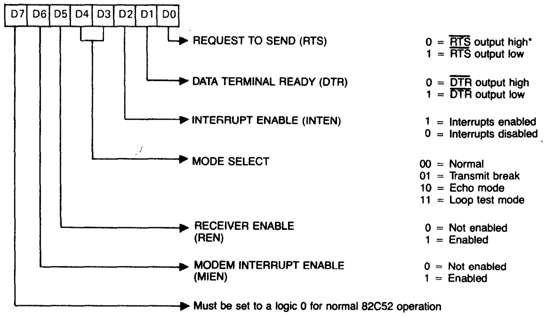
MODEM CONTROL REGISTER

The MCR is a general purpose control register which can be written to and read from. The $\overline{RTS}$ and $\overline{DTR}$ outputs are directly controlled by their associated bits in this register. Note that a logic one asserts a true logic level (low) at these output pins. The Interrupt Enable (INTEN) bit is the overall control for the INTR output pin. When INTEN is false, INTR is held false (low).

The Operating Mode bits configure the 82C52 into one of four possible modes. "Normal" configures the 82C52 for normal full or half duplex communications. "Transmit Break" enables the transmitter to only transmit break characters (Start, Data and Stop bits all are logic zero). The Echo Mode causes any data that is received on the SDI input pin to be re-transmitted on the SDO output pin. Note that this output is a buffered version of the data seen on the SDI input and is not a resynchronized output. Also note that normal UART transmission via the Transmitter Register is disabled when operating in the Echo mode (see Figure 4). The Loop Test Mode internally routes transmitted data to the receiver circuitry for the purpose of self test. The transmit data is disabled from the SDO output pin. The Receiver Enable bit gates off the input to the receiver circuitry when in the false state.

Modem Interrupt Enable will permit any change in modem status line inputs ($\overline{CTS}$, $\overline{DSR}$) to cause an interrupt when this bit is enabled. Bit D7 must always be written to with a logic zero to insure correct 82C52 operation.

MCR



*See Modem Status Register description (p5) for a description of register flag images with respect to output pins.

FIGURE 3.

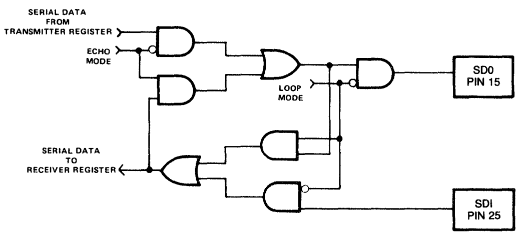


FIGURE 4. LOOP AND ECHO MODE FUNCTIONALITY

UART STATUS REGISTER (USR)

The USR provides a single register that the controlling system can examine to determine if errors have occurred or if other status changes in the 82C52 require attention. For this reason, the USR is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of the 82C52.

Three error flags OE, FE and PE report the status of any error conditions detected in the receiver circuitry. These error flags are updated with every character received during reception of the stop bits. The Overrun Error (OE) indicates that a character in the Receiver Register has been received and cannot be transferred to the Receiver Buffer Register (RBR) because the RBR was not read by the CPU. Framing Error (FE) indicates that the last character received in the RBR contained improper stop bits. This could be caused by the absence of the required stop bit(s) or by a stop bit(s) that was too short to be properly detected. Parity Error (PE) indicates that the last character received in the RBR contained a parity error based on the programmed parity of the receiver and the calculated parity of the received character data and parity bits.

The Received Break (RBRK) status bit indicates that the last character received was a break character. A break character would be considered to be an invalid data character in that the entire character including parity and stop bits are a logic zero.

The Modem Status bit is set whenever a transition is detected on any of the Modem input lines ($\overline{CTS}$ or $\overline{DSR}$). A subsequent read of the Modem Status Register will show the state of these two signals. Assertion of this bit will cause an interrupt (INTR) to be generated if the MIEN and INTEN bits in the MCR register are enabled.

The Transmission Complete (TC) bit indicates that both the TBR and Transmitter Registers are empty and the 82C52 has completed transmission of the last character it was commanded to transmit. The assertion of this bit will cause an interrupt (INTR) if the INTEN bit in the MCR register is true.

The Transmitter Buffer Register Empty (TBRE) bit indicates that the TBR register is empty and ready to receive another character.

The Data Ready (DR) bit indicates that the RBR has been loaded with a received character (including Break) and that the CPU may access this data.

Assertion of the TBRE or DR bits do not affect the INTR logic and associated INTR output pin since the 82C52 has been designed to provide separate requests via the DR and TBRE output pins. If a single interrupt for any status change in the 82C52 is desired this can be accomplished by using an 82C59A Interrupt controller with DR, TBRE, and INTR as inputs. (See Figure 11).

Reading the USR clears all of the status bits in the USR register, but does not affect associated output pins.

USR

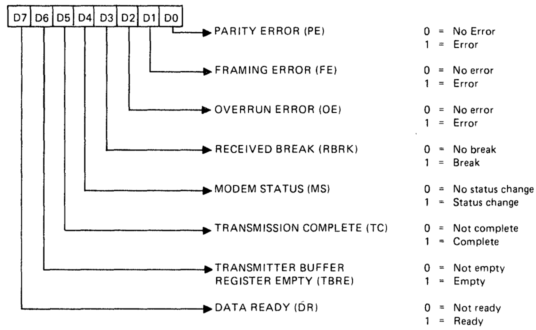


FIGURE 5.

MODEM STATUS REGISTER (MSR)

The MSR allows the CPU to read the modem signal inputs by accessing the data bus interface of the 82C52. Like all of the register images of external pins in the 82C52, true logic levels are represented by a high (1) signal level. By following this consistent definition, the system software need not be concerned with whether external signals are high or low true. In particular, the modem signal inputs are low true, thus a 0 (true assertion) at a modem input pin is represented by a 1 (true) in the MSR.

Any change of state in any modem input signals will set the Modem Status (MS) bit in the USR register. When this happens, an interrupt (INTR) will be generated if the MIEN and INTEN bits of the MCR are enabled.

The Data Set Ready ($\overline{DSR}$) input is a status indicator from the modem to the 82C52 which indicates that the modem is ready to provide received data to the 82C52 receiver circuitry.

Clear to Send ($\overline{CTS}$) is both a status and control signal from the modem that tells the 82C52 that the modem is ready to receive transmit data from the 82C52 transmitter output (SDO). A high (false) level on this input will inhibit the 82C52 from beginning transmission and if asserted in the middle of a transmission will only permit the 82C52 to finish transmission of the current character.

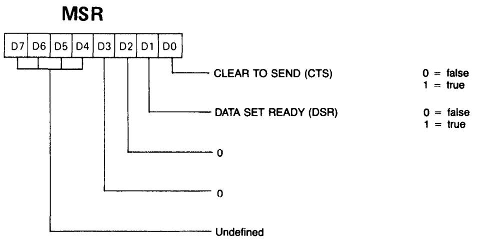


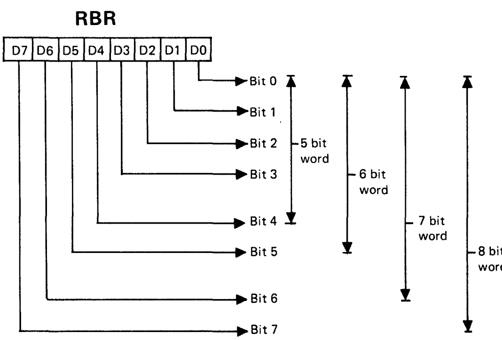
FIGURE 6.

RECEIVER BUFFER REGISTER (RBR)

The receiver circuitry in the 82C52 is programmable for 5, 6, 7 or 8 data bits per character. For words of less than 8 bits, the data is right justified to the Least Significant Bit (LSB = D0). Bit D0 of a data word is always the first data bit received. The unused bits in a less than 8 bit word, at the parallel interface, are set to a logic zero (0) by the 82C52.

Received data at the SDI input pin is shifted into the Receiver Register by an internal 1x clock which has been synchronized to the incoming data based on the position of the start bit. When a complete character has been shifted into the Receiver Register, the assembled data bits are parallel loaded into the Receiver Buffer Register. Both the DR output pin and DR flag in the USR register are set. This double buffering of the received data permits continuous reception of data without losing any of the received data.

While the Receiver Register is shifting a new character into the 82C52, the Receiver Buffer Register is holding a previously received character for the system CPU to read. Failure to read the data in the RBR before complete reception of the next character can result in the loss of the data in the Receiver Register. The OE flag in the USR register indicates the overrun condition.



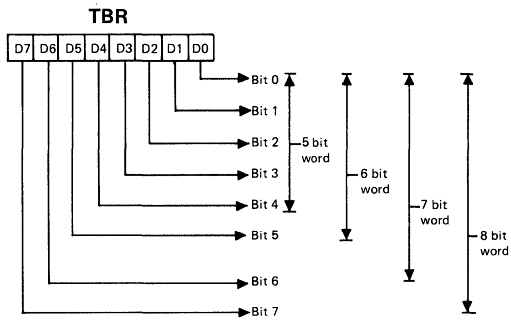
Note: The LSB, Bit 0 is the first serial data bit received.

FIGURE 7.

TRANSMITTER BUFFER REGISTER (TBR)

The Transmitter Buffer Register (TBR) accepts parallel data from the data bus (D0-D7) and holds it until the Transmitter Register is empty and ready to accept a new character for transmission. The transmitter always has the same word length and number of stop bits as the receiver. For words of less than 8 bits the unused bits at the microprocessor data bus are ignored by the transmitter.

Bit 0, which corresponds to D0 at the data bus, is always the first serial data bit transmitted. Provision is made for the transmitter parity to be the same or different from the receiver. The TBRE output pin and flag (USR register) reflect the status of the TBR. The TC flag (USR register) indicates when both the TBR and TR are empty.



Note: The LSB, Bit 0 is the first serial data bit transmitted.

FIGURE 8.

82C52 INTERRUPT STRUCTURE

The 82C52 has provisions for software masking of interrupts generated for the INTR output pin. Two control bits in the MCR register, MIEN and INTEN, control modem status interrupts and overall 82C52 interrupts respectively. Figure 9 illustrates the logical control function provided by these signals.

The modem status inputs ($\overline{DSR}$ and $\overline{CTS}$) will trigger the edge detection circuitry with any change of status. Reading the MSR register will clear the detect circuit but has no effect on the status bits themselves. These status bits always reflect the state of the input pins regardless of the mask control signals. Note that the state (high or low) of the status bits are inverted versions of the actual input pins.

The edge detection circuits for the USR register signals will trigger only for a positive edge (true assertion) of these status bits. Reading the USR register not only clears the edge detect circuit but also clears (sets to 0) all of the status bits. The output pins associated with these status bits are not affected by reading the USR register.

A hardware reset of the 82C52 sets the TC status bit in the USR. When interrupts are subsequently enabled an interrupt can occur due to the fact that the positive edge detection circuitry in the interrupt logic has detected the setting of the TC bit. If this interrupt is not desired the USR should be read prior to enabling interrupts. This action resets the positive edge detection circuitry in the interrupt control logic (Figure 9).

NOTE: For USR and MSR, the setting of status bits is inhibited during status register READ operations. If a status condition is generated during a READ operation, the status bit is not set until the trailing edge of the $\overline{RD}$ pulse.

If the bit was already set at the time of the READ operation, and the same status condition occurs, that status bit will be cleared at the trailing edge of the $\overline{RD}$ pulse instead of being set again.

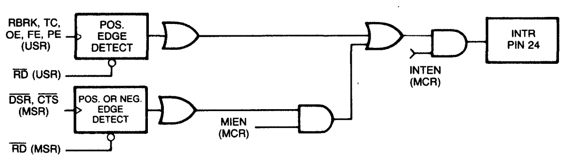


FIGURE 9. 82C52 INTERRUPT STRUCTURE

SOFTWARE RESET

A software reset of the 82C52 is a useful method for returning to a completely known state without exercising a complete system reset. Such a reset would consist of writing to the UCR, BRSR and MCR registers. The USR and RBR registers should be read prior to enabling interrupts in order to clear out any residual data or status bits which may be invalid for subsequent operation.

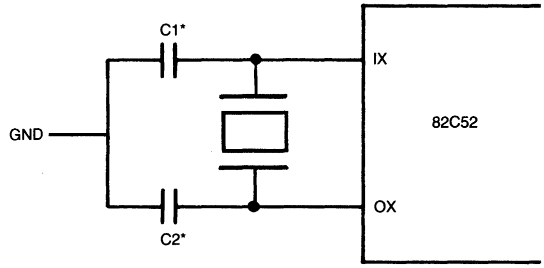
CRYSTAL OPERATION

The 82C52 crystal oscillator circuitry is designed to operate with a fundamental mode, parallel resonant crystal. This circuit is the same one used in the Harris 82C84A clock generator/driver and the general oscillator operation information which is contained in Tech Brief TB-47 will be pertinent to the 82C52. To summarize, Table 3 and Figure 10 show the required crystal parameters and crystal circuit configuration respectively.

When using an external clock source, the IX input is driven and the OX output is left open. Power consumption when using an external clock is typically 50% of that required when using a crystal. This is due to the sinusoidal nature of the drive circuitry when using a crystal.

TABLE 3.

PARAMETER	TYPICAL CRYSTAL SPECIFICATION
Frequency	1.0 to 16MHz
Type of Operation	Parallel resonant, Fundamental mode
Load Capacitance (CL)	20 or 32 pf. (typ.)
R_{series}(Max.)	100 ohms (f=16 MHz, CL = 32pf.) 200 ohms (f=16 MHz, CL = 20pf.)



*C1 = C2 = 20 pf for CL=20 pf
*C1 = C2 = 47 pf for CL=32 pf

FIGURE 10.

82C52 - 80C86 INTERFACING

The following example (Figure 11) shows the interface for an 82C52 in an 80C86 system.

Use of the Harris CMOS Interrupt Controller (82C59A) is optional and necessary only if an interrupt driven system is desired.

By using the Harris CMOS 82C84A clock generator, the system can be built with a single crystal providing both the processor clock and the clock for the 82C52. The 82C52 has special divider circuitry which is designed to supply industry standard baud rates with a 2.4576 MHz input frequency. Using a 15 MHz crystal as shown, results in less than a 2% frequency error which is adequate for many applications. For more precise baud rate requirements, a 14.7456 MHz crystal will drive the 80C86 at 4.9 MHz and provide the 82C52 with the standard baud rate input frequency of 2.4576 MHz. If baud rates above 156 Kbaud are desired, the OSC output can be used instead of the PCLK (÷6) output for asynchronous baud rates up to 1 Mbaud.

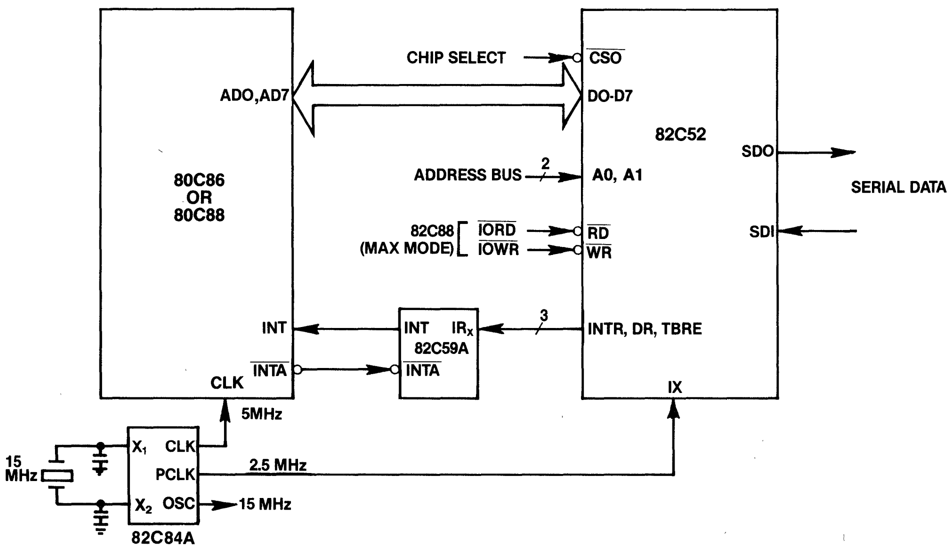


FIGURE 11. 80C86/82C52 INTERFACE

Absolute Maximum Ratings

Supply Voltage .... +8.0 Volts
Input, Output or I/O Voltage Applied .... GND -0.5V to VCC +0.5V
Storage Temperature Range .... -65°C to +150°C
Maximum Package Power Dissipation .... 1 Watt
θ_{jc} .... 18°C/W (CERDIP Package), 23°C/W (LCC Package)
θ_{ja} .... 56°C/W (CERDIP Package), 61°C/W (LCC Package)
Gate Count .... 1500 Gates
Junction Temperature .... +150°C
Lead Temperature (Soldering, Ten Seconds) .... +260°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +4.5V to +5.5V
Operating Temperature Range
C82C52 .... 0°C to +70°C
I82C52 .... -40°C to +85°C
M82C52 .... -55°C to +125°C

D.C. Electrical Specifications

VCC = 5.0V ± 10%;
T_A = 0°C to +70°C (C82C52)
T_A = -40°C to +85°C (I82C52)
T_A = -55°C to +125°C (M82C52)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	Logical One Input Voltage	2.0 2.2		V	I82C52, C82C52 M82C52
VIL	Logical Zero Input Voltage		0.8	V	
VTH	Schmitt Trigger Logical One Input Voltage	VCC-0.5		V	Reset Input
VTL	Schmitt Trigger Logical Zero Input Voltage		GND +0.5	V	Reset Input
VIH (CLK)	Logical One Clock Input Voltage	VCC-0.5		V	External Clock
VIL (CLK)	Logical Zero Clock Input Voltage		GND +0.5	V	External Clock
VOH	Output High Voltage	3.0 VCC-0.4		V V	IOH = -2.5mA IOH = -100μA
VOL	Output Low Voltage		0.4	V	IOL = +2.5mA
II	Input Leakage Current	-1.0	+1.0	μA	VIN = GND or VCC, DIP Pins 1, 2, 11, 12, 17, 18, 23, 25, 28
IO	Input/Output Leakage Current	-10.0	+10.0	μA	VO = GND or VCC, DIP Pins 3-10
ICCOP*	Operating Power Supply Current		3	mA	External Clock F = 2.4576MHz, VCC = 5.5V, VIN = VCC or GND, Outputs Open

*Guaranteed and sampled, but not 100% tested. ICCOP is typically ≤ 1mA/MHz.

Capacitance

T_A = 25°C; VCC = GND = 0V; VIN = +5V or GND

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_{IN}	Input Capacitance	10	pF	FREQ = 1MHz, Unmeasured pins returned to GND
C_{OUT}	Output Capacitance	15	pF	
C_{IO}	I/O Capacitance	20	pF	

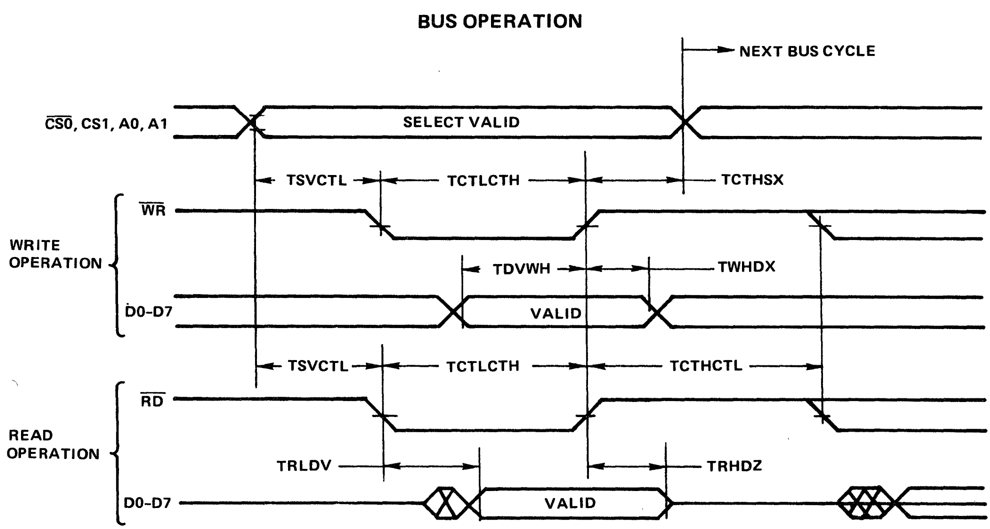
A.C. Electrical Specifications

VCC = 5.0V ± 10%;
TA = 0°C to +70°C (C82C52)
TA = -40°C to +85°C (I82C52)
TA = -55°C to +125°C (M82C52)

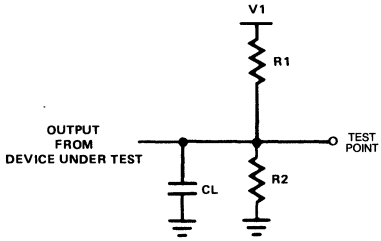
Timing Requirements and Responses

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
TSVCTL	Select Setup to Control Leading Edge	30		ns	
TCTHSX	Select Hold From Control Trailing Edge	50		ns	
TCTLCTH	Control Pulse Width	150		ns	Control Consists of $\overline{RD}$ or $\overline{WR}$
TCTHCTL	Control Disable to Control Enable	100		ns	
TRLDV	Read Low to Data Valid		120	ns	1
TRHDZ	Read Disable	0	60	ns	2
TDVWH	Data Setup Time	50		ns	
TWHDX	Data Hold Time	20		ns	
FC	Clock Frequency	0	16	MHz	TCHCL + TCLCH must be ≥62.5 ns
TCHCL	Clock High Time	25		ns	
TCLCH	Clock Low Time	25		ns	
TR/TF	IX Input Rise/Fall Time (External Clock)		tx	ns	$tx \leq \frac{1}{6FC}$ or 50ns whichever is smaller
TFCO	Clock Output Fall Time		15	ns	CL = 50 pf
TRCO	Clock Output Rise Time		15	ns	CL = 50 pf

Timing Diagram

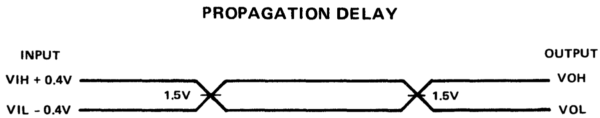


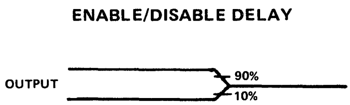
A.C. Test Circuit



	TEST CONDITION	V1	R1	R2	CL
1	Propagation Delay	1.7V	520	∞	100pF
2	Disable Delay	VCC	5K	5K	50pF

A.C. Testing Input, Output Waveforms





A.C. Testing: All input signals must switch between VIL -0.4V and VIH +0.4V. Input rise and fall times are driven at 1nsec per volt.

HARRIS

82C54

CMOS Programmable Interval Timer

Features

- **Compatible with NMOS 8254**
  - **Enhanced Version of NMOS 8253**
- **8MHz Clock Input Frequency**
- **Three Independent 16 Bit Counters**
- **Six Programmable Counter Modes**
- **Status Read Back Command**
- **Binary or BCD Counting**
- **Fully TTL Compatible**
- **Scaled SAJI IV CMOS Process**
- **Low Power**
  - **ICCSB = 10μA**
  - **ICCOP = 10mA**
- **Single 5V Power Supply**
- **Wide Operating Temperature Ranges:**
  - **C82C54 .... 0°C to 70°C**
  - **I82C54 .... -40°C to +85°C**
  - **M82C54 .... -55°C to +125°C**

Description

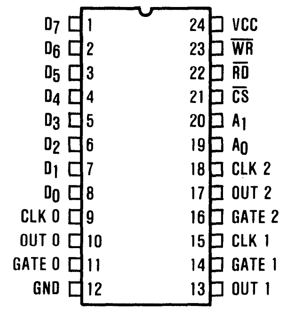
The Harris 82C54 is a high performance CMOS Programmable Interval Timer manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). The 82C54 has three independently programmable and functional 16 bit counters, each capable of handling clock input frequencies of up to 8MHz. The high speed and industry standard configuration of the 82C54 make it compatible with the Harris 80C86 and 80C88 CMOS microprocessors along with many other industry standard processors.

Six programmable timer modes allow the 82C54 to be used as an event counter, elapsed time indicator, programmable one-shot along with many other applications.

Static CMOS circuit design insures low operation power Harris advanced SAJI process results in a significant reduction in power with performance equal to or greater than existing equivalent products.

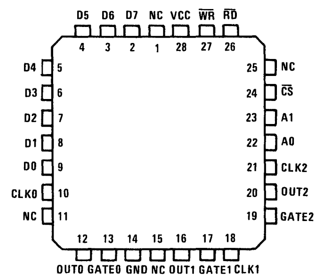
Pinouts

TOP VIEW

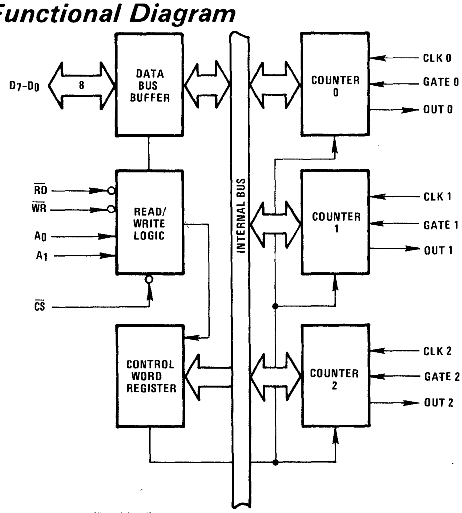


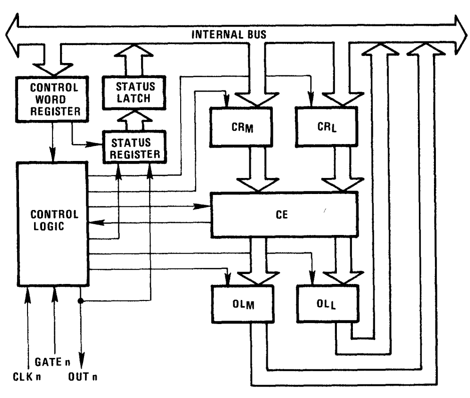
LCC/PLCC

TOP VIEW



Functional Diagram





COUNTER INTERNAL BLOCK DIAGRAM

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Pin Description

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
D_7-D_0	1-8	I/O	DATA: Bi-directional three state data bus lines, connected to system data bus.
CLK 0	9	I	CLOCK 0: Clock input of Counter 0.
OUT 0	10	O	OUT 0: Output of Counter 0.
GATE 0	11	I	GATE 0: Gate input of Counter 0.
GND	12		GROUND: Power supply connection.
OUT 1	13	O	OUT 1: Output of Counter 1.
GATE 1	14	I	GATE 1: Gate input of Counter 1.
CLK 1	15	I	CLOCK 1: Clock input of Counter 1.
GATE 2	16	I	GATE 2: Gate input of Counter 2.
OUT 2	17	O	OUT 2: Output of Counter 2.
CLK 2	18	I	CLOCK 2: Clock input of Counter 2.
A0, A1	19-20	I	ADDRESS: Select inputs for one of the three counters or Control Word Register for read/write operations. Normally connected to the system address bus. A_1 A_0 Selects 0 0 Counter 0 0 1 Counter 1 1 0 Counter 2 1 1 Control Word Register
$\overline{CS}$	21	I	CHIP SELECT: A low on this input enables the 82C54 to respond to $\overline{RD}$ and $\overline{WR}$ signals. $\overline{RD}$ and $\overline{WR}$ are ignored otherwise.
$\overline{RD}$	22	I	READ: This input is low during CPU read operations.
$\overline{WR}$	23	I	WRITE: This input is low during CPU write operations.
VCC	24		VCC: The +5V power supply Pin. A 0.1μF capacitor between pins 12 and 24 is recommended for decoupling.

Functional Description

General

The 82C54 is a programmable interval timner/counter designed for use with microcomputer systems. It is a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software.

The 82C54 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in software, the programmer configures the 82C54 to match his requirements and programs one of the counters for the desired delay. After the desired delay, the 82C54 will interrupt the CPU. Software overhead is minimal and variable length delays can easily be accommodated.

Some of the other computer/timer functions common to microcomputers which can be implemented with the 82C54 are:

- Real time clock
- Event counter
- Digital one-shot
- Programmable rate generator
- Square wave generator
- Binary rate multiplier
- Complex waveform generator
- Complex motor controller

Data Bus Buffer

This three-state, bi-directional, 8-bit buffer is used to interface the 82C54 to the system bus (see Figure 1).

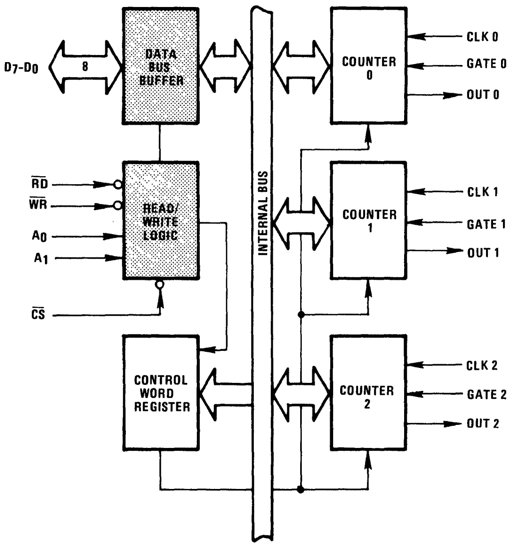


FIGURE 1. DATA BUS BUFFER AND READ/WRITE LOGIC FUNCTION

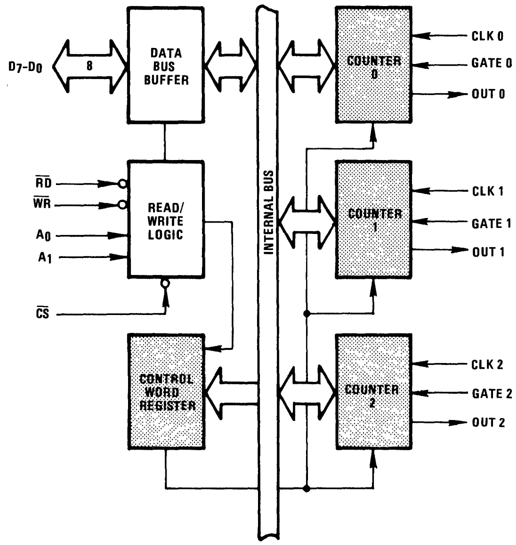


FIGURE 2. CONTROL WORD REGISTER AND COUNTER FUNCTIONS

Read/Write Logic

The Read/Write Logic accepts inputs from the system bus and generates control signals for the other functional blocks of the 82C54. A_1 and A_0 select one of the three counters or the Control Word Register to be read from/written into. A "low" on the $\overline{RD}$ input tells the 82C54 that the CPU is reading one of the counters. A "low" on the $\overline{WR}$ input tells the 82C54 that the CPU is writing either a Control Word or an initial count. Both $\overline{RD}$ and $\overline{WR}$ are qualified by $\overline{CS}$; $\overline{RD}$ and $\overline{WR}$ are ignored unless the 82C54 has been selected by holding $\overline{CS}$ low.

Control Word Register

The Control Word Register (Figure 2) is selected by the Read/Write Logic when $A_1, A_0 = 11$. If the CPU then does a write operation to the 82C54, the data is stored in the Control Word Register and is interpreted as a Control Word used to define the Counter operation.

The Control Word Register can only be written to; status information is available with the Read-Back Command.

Counter 0, Counter 1, Counter 2

These three functional clocks are identical in operation, so only a single Counter will be described. The internal block diagram of a single counter is shown in Figure 3. The counters are fully independent. Each Counter may operate in a different Mode.

The Control Word Register is shown in the figure; it is not part of the Counter itself, but its contents determine how the Counter operates.

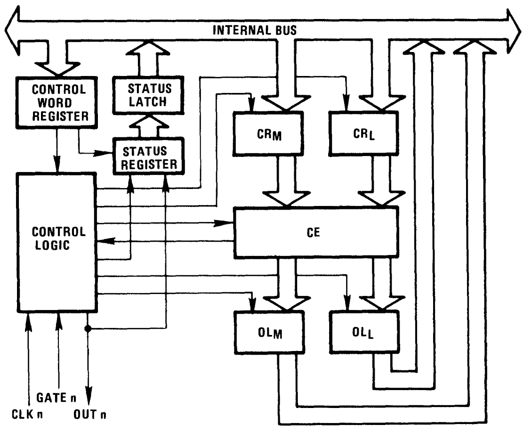


FIGURE 3. COUNTER INTERNAL BLOCK DIAGRAM

The status register, shown in the figure, when latched, contains the current contents of the Control Word Register and status of the output and null count flag. (See detailed explanation of the Read-Back command.)

The actual counter is labeled CE (for Counting Element). It is a 16 bit presettable synchronous down counter.

OL_M and OL_L are two 8-bit latches. OL stands for "Output Latch"; the subscripts M and L for "Most significant byte" and "Least significant byte", respectively. Both are normally referred to as one unit and called just OL. These latches normally "follow" the CE, but if a suitable Counter Latch Command is sent to the 82C54, the latches "latch" the present count until read by the CPU and then return to "following" the CE. One latch at a time is enabled by the counter's Control Logic to drive the internal bus. This is how the 16-bit Counter communicates over the 8-bit internal bus. Note that the CE itself cannot be read; whenever you read the count, it is the OL that is being read.

Similarly, there are two 8-bit registers called CR_M and CR_L (for "Count Register"). Both are normally referred to as one unit and called just CR. When a new count is written to the Counter, the count is stored in the CR and later transferred to the CE. The Control Logic allows one register at a time to be loaded from the internal bus. Both bytes are transferred to the CE simultaneously. CR_M and CR_L are cleared when the Counter is programmed for one byte counts (either most significant byte only or least significant byte only) the other byte will be zero. Note that the CE cannot be written into; whenever a count is written, it is written into the CR.

The Control Logic is also shown in the diagram. CLK n, GATE n, and OUT n are all connected to the outside world through the Control Logic.

82C54 System Interface

The 82C54 is treated by the system software as an array of peripheral I/O ports; three are counters and the fourth is a control register for MODE programming.

Basically, the select inputs A_0, A_1 connect to the A_0, A_1 address bus signals of the CPU. The CS can be derived directly from the address bus using a linear select method or it can be connected to the output of a decoder, such as a Harris HD-6440 for larger systems.

Operational Description

General

After power-up, the state of the 82C54 is undefined. The Mode, count value, and output of all Counters are undefined.

How each Counter operates is determined when it is programmed. Each Counter must be programmed before it can be used. Unused counters need not be programmed.

Programming The 82C54

Counters are programmed by writing a Control Word and then an initial count.

All Control Words are written into the Control Word Register, which is selected when $A_1, A_0 = 11$. The Control Word specifies which Counter is being programmed.

By contrast, initial counts are written into the Counters, not the Control Word Register. The A_1, A_0 inputs are used to select the Counter to be written into. The format of the initial count is determined by the Control Word used.

Write Operations

The programming procedure for the 82C54 is very flexible. Only two conventions need to be remembered:

1. For each Counter, the Control Word must be written before the initial count is written.
2. The initial count must follow the count format specified in the Control Word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

Since the Control Word Register and the three Counters have separate addresses (selected by the A_1, A_0 inputs), and each Control Word specifies the Counter it applies to (SC0, SC1 bits), no special instruction sequence is required. Any programming sequence that follows the conventions above is acceptable.

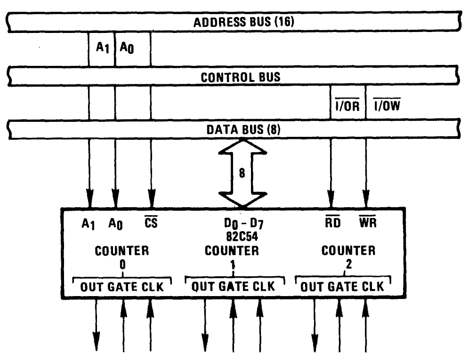


FIGURE 4. 82C54 SYSTEM INTERFACE

Control Word Format

A_1, A_0 = 11; $\overline{CS}$ = 0; $\overline{RD}$ = 1; $\overline{WR}$ = 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC — Select Counter:

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (See Read Operations)

RW — Read/Write:

RW1	RW0	
0	0	Counter Latch Command (See Read Operations)
0	1	Read/Write least significant byte only.
1	0	Read/Write most significant byte only.
1	1	Read/Write least significant byte first, then most significant byte.

M — Mode:

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD — Binary Coded Decimal:

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

NOTE: Don't Care bits (X) should be 0 to insure compatibility with future products.

FIGURE 5. CONTROL WORD FORMAT

	A_1	A_0
Control Word — Counter 0	1	1
LSB of count — Counter 0	0	0
MSB of count — Counter 0	0	0
Control Word — Counter 1	1	1
LSB of count — Counter 1	0	1
MSB of count — Counter 1	0	1
Control Word — Counter 2	1	1
LSB of count — Counter 2	1	0
MSB of count — Counter 2	1	0

	A_1	A_0
Control Word — Counter 2	1	1
Control Word — Counter 1	1	1
Control Word — Counter 0	1	1
LSB of count — Counter 2	1	0
MSB of count — Counter 2	1	0
LSB of count — Counter 1	0	1
MSB of count — Counter 1	0	1
LSB of count — Counter 0	0	0
MSB of count — Counter 0	0	0

	A_1	A_0
Control Word — Counter 0	1	1
Control Word — Counter 1	1	1
Control Word — Counter 2	1	1
LSB of count — Counter 2	1	0
LSB of count — Counter 1	0	1
LSB of count — Counter 0	0	0
MSB of count — Counter 0	0	0
MSB of count — Counter 1	0	1
MSB of count — Counter 2	1	0

	A_1	A_0
Control Word — Counter 1	1	1
Control Word — Counter 0	1	1
LSB of count — Counter 1	0	1
Control Word — Counter 2	1	1
LSB of count — Counter 0	0	0
MSB of count — Counter 1	0	1
LSB of count — Counter 2	1	0
MSB of count — Counter 0	0	0
MSB of count — Counter 2	1	0

NOTE: In all four examples, all counters are programmed to Read/Write two-byte counts. These are only four of many possible programming sequences.

FIGURE 6. A FEW POSSIBLE PROGRAMMING SEQUENCES

A new initial count may be written to a Counter at any time without affecting the Counter's programmed Mode in any way. Counting will be affected as described in the Mode definitions. The new count must follow the programmed count format.

If a Counter is programmed to read/write two-byte counts, the following precaution applies: A program must not transfer control between writing the first and second byte to another routine which also writes into that same Counter. Otherwise, the Counter will be loaded with an incorrect count.

Read Operations

It is often desirable to read the value of a Counter without disturbing the count in progress. This is easily done in the 82C54.

There are three possible methods for reading the Counters. The first is through the Read-Back command, which is explained later. The second is a simple read operation of the Counter, which is selected with the A_1, A_0 inputs. The only requirement is that the CLK input of the selected Counter must be inhibited by using either the GATE input or external logic. Otherwise, the count may be in process of changing when it is read, giving an undefined result.

Counter Latch Command

The other method for reading the Counters involves a special software command called the "Counter Latch Command". Like a Control Word, this command is written to the Control Word Register, which is selected when A_1, A_0 = 11. Also, like a Control Word, the SC0, SC1 bits select one of the three Counters, but two other bits, D_5 and D_4, distinguish this command from a Control Word.

A_1, A_0 = 11; $\overline{CS}$ = 0; $\overline{RD}$ = 1; $\overline{WR}$ = 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	0	0	X	X	X	X

SC1, SC0 — specify counter to be latched

SC1	SC0	Counter
0	0	0
0	1	1
1	0	2
1	1	Read-Back Command

D5, D4 — 00 designates Counter Latch Command
X — Don't Care

NOTE Don't Care bits (X) should be 0 to insure compatibility with future products.

FIGURE 7. COUNTER LATCH COMMAND FORMAT

The selected Counter's output latch (OL) latches the count when the Counter Latch Command is received. This count is held in the latch until it is read by the CPU (or until the Counter is reprogrammed). The count is then unlatched automatically and the OL returns to "following" the counting element (CE). This allows reading the contents of the Counters "on the fly" without affecting counting in progress. Multiple Counter Latch Commands may be used to latch more than one Counter. Each latched Counter's OL holds its count until read. Counter Latch Commands do not affect the programmed Mode of the Counter in any way.

If a Counter is latched and then, some time later, latched again before the count is read, the second Counter Latch Command is ignored. The count read will be the count at the time the first Counter Latch Command was issued.

With either method, the count must be read according to the programmed format; specifically, if the Counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other; read or write or programming operations of other Counters may be inserted between them.

Another feature of the 82C54 is that reads and writes of the same Counter may be interleaved; for example, if the Counter is programmed for two byte counts, the following sequence is valid.

1. Read least significant byte.
2. Write new least significant byte.
3. Read most significant byte.
4. Write new most significant byte.

If a Counter is programmed to read or write two-byte counts, the following precaution applies: A program MUST NOT transfer control between reading the first and second byte to another routine which also reads from that same Counter. Otherwise, an incorrect count will be read.

Read-Back Command

The read-back command allows the user to check the count value, programmed Mode, and current state of the OUT pin and Null Count flag of the selected counter(s).

The command is written into the Control Word Register and has the format shown in Figure 8. The command applies to the counters selected by setting their corresponding bits D_3, D_2, D_1 = 1.

A_0, A_1 = 11; $\overline{CS}$ = 0; $\overline{RD}$ = 1; $\overline{WR}$ = 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	$\overline{COUNT}$	$\overline{STATUS}$	CNT 2	CNT 1	CNT 0	0

D_5: 0 = Latch count of selected Counters(s)
D_4: 0 = Latch status of selected Counters(s)
D_3: 1 = Select Counter 2
D_2: 1 = Select Counter 1
D_1: 1 = Select Counter 0
D_0: Reserved for future expansion; Must be 0

FIGURE 8. READ-BACK COMMAND FORMAT

The read-back command may be used to latch multiple counter output latches (OL) by setting the COUNT bit D_5 = 0 and selecting the desired counter(s). This single command is functionally equivalent to several counter latch commands, one for each counter latched. Each counter's latched count is held until it is read (or the counter is reprogrammed). That counter is automatically unlatched when read, but other counters remain latched until they are read. If multiple count read-back commands are issued to the same counter without reading the count, all but the first are ignored; i.e., the count which will be read is the count at the time the first read-back command was issued.

The read-back command may also be used to latch status information of selected counter(s) by setting STATUS bit D_4 = 0. Status must be latched to be read; status of a counter is accessed by a read from that counter.

The counter status format is shown in Figure 9. Bits D_5 through D_0 contain the counter's programmed Mode exactly as written in the last Mode Control Word. OUTPUT bit D_7 contains the current state of the OUT pin. This allows the user to monitor the counter's output via software, possibly eliminating some hardware from a system.

D7	D6	D5	D4	D3	D2	D1	D0
OUTPUT	NULL COUNT	RW1	RW0	M2	M1	M0	BCD

D7 1 = Out Pin is 1
0 = Out pin is 0
D6 1 = Null count
0 = Count available for reading
D5-D0 = Counter programmed mode (See Figure 5)

FIGURE 9. STATUS BYTE

NULL COUNT bit D_6 indicates when the last count written to the counter register (CR) has been loaded into the counting element (CE). The exact time this happens depends on the Mode of the counter and is described in the Mode Definitions, but until the counter is loaded into the counting element (CE), it can't be read from the counter. If the count is latched or read before this time, the count value will not reflect the new count just written. The operation of Null Count is shown in Figure 10.

THIS ACTION:	CAUSES:
A. Write to the control word register: (1)	Null Count = 1
B. Write to the count register (CR): (2)	Null Count = 1
C. New count is loaded into CE (CR → CE):	Null Count = 0

(1) Only the counter specified by the control word will have its null count set to 1. Null count bits of other counters are unaffected.

(2) If the counter is programmed for two-byte counts (least significant byte then most significant byte) null count goes to 1 when the second byte is written.

FIGURE 10. NULL COUNT OPERATION

If multiple status latch operations of the counter(s) are performed without reading the status, all but the first are ignored; i.e., the status that will be read is the status of the counter at the time the first status read-back command was issued.

Both count and status of the selected counter(s) may be latched simultaneously by setting both COUNT and STATUS bits D_5, D_4 = 0. This is functionally the same as issuing two separate read-back commands at once, and the above discussions apply here also. Specifically, if multiple count and/or status read-back commands are issued to the same counter(s) without any intervening reads, all but the first are ignored. This is illustrated in Figure 11.

If both count and status of a counter are latched, the first read operation of that counter will return latched status, regardless of which was latched first. The next one or two reads (depending on whether the counter is programmed for one or two type counts) return latched count. Subsequent reads return unlatched count.

COMMAND									
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	DESCRIPTION	RESULT
1	1	0	0	0	0	1	0	Read back count and status of Counter 0	Count and status latched for Counter 0
1	1	1	0	0	1	0	0	Read-back status of Counter 1	Status latched for Counter 1
1	1	1	0	1	1	0	0	Read-back status of Counters 2, 1	Status latched for Counter 2, but not Counter 1
1	1	0	1	1	0	0	0	Read-back count of Counter 2	Count latched for Counter 2
1	1	0	0	0	1	0	0	Read-back count and status of Counter 1	Count latched for Counter 1, but not status
1	1	1	0	0	0	1	0	Read-back status of Counter 1	Command ignored, status already latched for Counter 1

FIGURE 11. READ-BACK COMMAND EXAMPLE

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	
0	1	0	0	0	Write into Counter 0
0	1	0	0	1	Write into Counter 1
0	1	0	1	0	Write into Counter 2
0	1	0	1	1	Write Control Word
0	0	1	0	0	Read from Counter 0
0	0	1	0	1	Read from Counter 1
0	0	1	1	0	Read from Counter 2
0	0	1	1	1	No-Operation (Three-State)
1	X	X	X	X	No-Operation (Three-State)
0	1	1	X	X	No-Operation (Three-State)

FIGURE 12. READ/WRITE OPERATIONS SUMMARY

Mode Definitions

The following are defined for use in describing the operation of the 82C54.

CLK PULSE:

A rising edge, then a falling edge, in that order, of a Counter's CLK input.

TRIGGER:

A rising edge of a Counter's Gate input.

COUNTER LOADING:

The transfer of a count from the CR to the CE (See "Functional Description")

Mode 0: Interrupt on Terminal Count

Mode 0 is typically used for event counting. After the Control Word is written, OUT is initially low, and will remain low until the Counter reaches zero. OUT then goes high and remains high until a new count or a new Mode 0 Control Word is written to the Counter.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

After the Control Word and initial count are written to a Counter, the initial count will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not go high until N + 1 CLK pulses after the initial count is written.

If a new count is written to the Counter it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

1- Writing the first byte disables counting. Out is set low immediately (no clock pulse required).

2- Writing the second byte allows the new count to be loaded on next CLK pulse.

This allows the counting sequence to be synchronized by software. Again OUT does not go high until N + 1 CLK pulses after the new count of N is written.

If an initial count is written while GATE = 0, it will still be loaded on the next CLK pulse. When GATE goes high, OUT will go high N CLK pulses later; no CLK pulse is needed to load the counter as this has already been done.

Mode 1: Hardware Retriggerable One-Shot

OUT will be initially high. OUT will go low on the CLK pulse following a trigger to begin the one-shot pulse, and will remain low until the Counter reaches zero. OUT will then go high and remain high until the CLK pulse after the next trigger.

After writing the Control Word and initial count, the Counter is armed. A trigger results in loading the Counter and setting OUT low on the next CLK pulse, thus starting the one-shot pulse N CLK cycles in duration. The one-shot is retriggerable, hence OUT will remain low for N CLK pulses after any trigger. The one-shot pulse can be repeated without rewriting the same count into the counter. GATE has no effect on OUT.

If a new count is written to the Counter during a one-shot pulse, the current one-shot is not affected unless the Counter is retriggered. In that case, the Counter is loaded with the new count and the one-shot pulse continues until the new count expires.

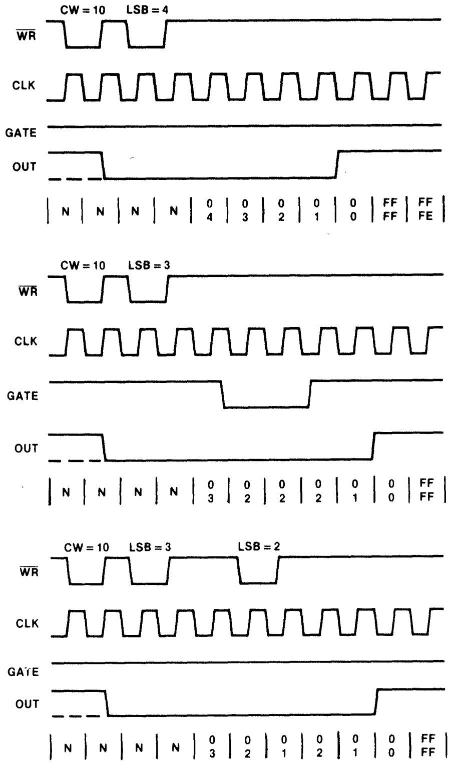
Mode 2: Rate Generator

This Mode functions like a divide-by-N counter. It is typically used to generate a Real Time Clock interrupt. OUT will initially be high. When the initial count has decremented to 1, OUT goes low for one CLK pulse. OUT then goes high again, the Counter reloads the initial count and the process is repeated. Mode 2 is periodic; the same sequence is repeated indefinitely. For an initial count of N, the sequence repeats every N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low during an output pulse, OUT is set high immediately. A trigger reloads the Counter with the initial count on the next CLK pulse; OUT goes low N CLK pulses after the trigger. Thus the GATE input can be used to synchronize the Counter.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. OUT goes low N CLK pulses after the initial count is written. This allows the Counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current period, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current counting cycle.



NOTE: The following conventions apply to all mode timing diagrams.

1. Counters are programmed for binary (not BCD) counting and for reading/writing least significant byte (LSB) only.
2. The counter is always selected ($\overline{CS}$ always low).
3. CW stands for "Control Word"; CW = 10 means a control word of 10, Hex is written to the counter.
4. LSB stands for "Least significant byte" of count.
5. Numbers below diagrams are count values. The lower number is the least significant byte. The upper number is the most significant byte. Since the counter is programmed to read/write LSB only, the most significant byte cannot be read.
6. N stands for an undefined count.
7. Vertical lines show transitions between count values.

FIGURE 13. MODE 0

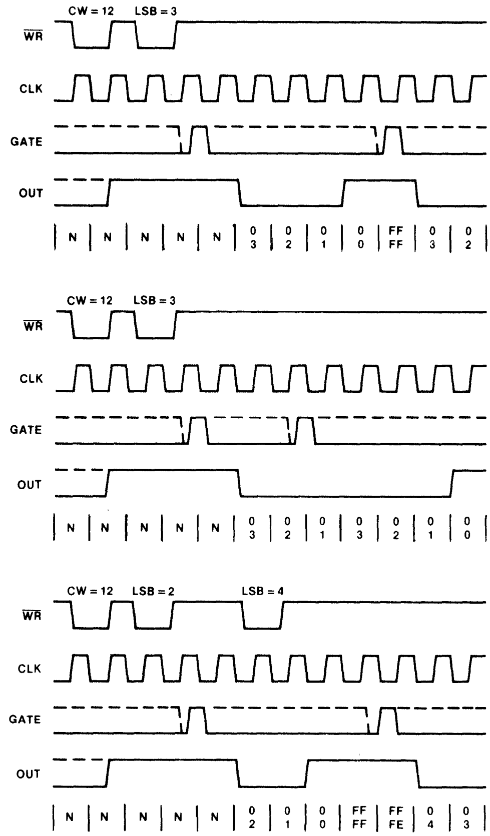


FIGURE 14. MODE 1

Mode 3: Square Wave Mode

Mode 3 is typically used for Baud rate generation. Mode 3 is similar to Mode 2 except for the duty cycle of OUT. OUT will initially be high. When half the initial count has expired, OUT goes low for the remainder of the count. Mode 3 is periodic; the sequence above is repeated indefinitely. An initial count of N results in a square wave with a period of N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low while OUT is low, OUT is set high immediately; no CLK pulse is required. A trigger reloads the Counter with the initial count on the next CLK pulse. Thus the GATE input can be used to synchronize the Counter.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This allows the Counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current half-cycle of the square wave, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current half-cycle.

Mode 3 is implemented as follows:

EVEN COUNTS: OUT is initially high. The initial count is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. When the count expires, OUT changes value and the Counter is reloaded with the initial count. The above process is repeated indefinitely.

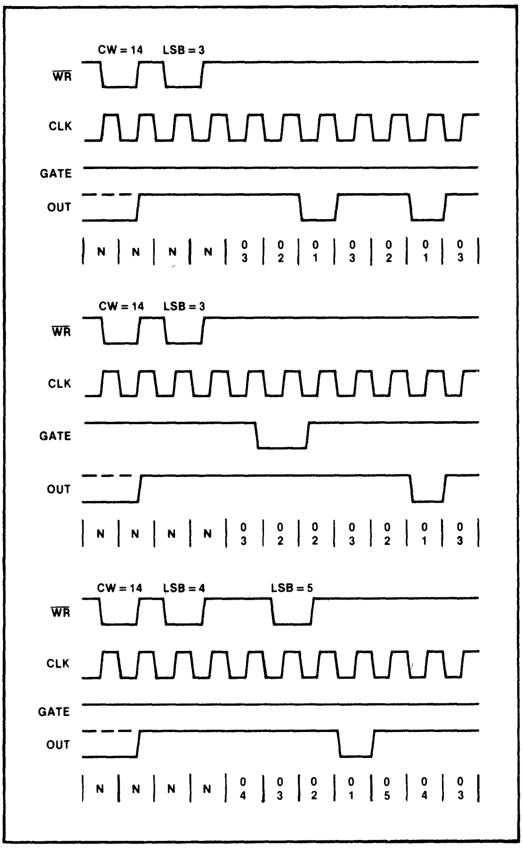


FIGURE 15. MODE 2

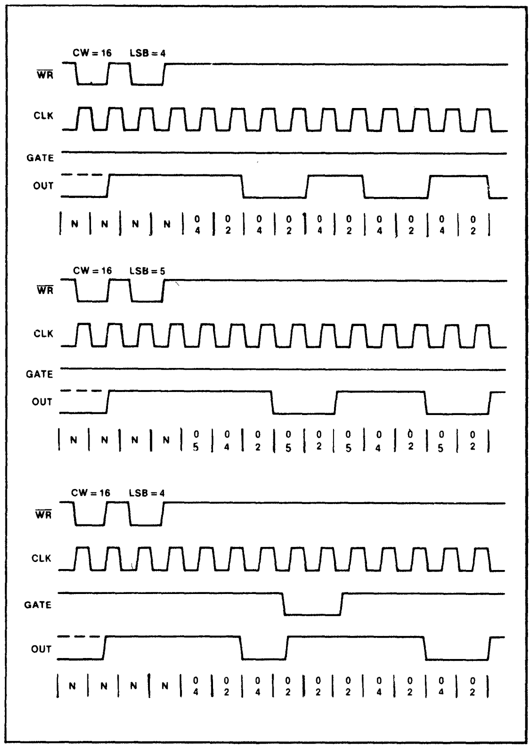


FIGURE 16. MODE 3

ODD COUNTS: OUT is initially high. The initial count is loaded on one CLK pulse, decremented by one on the next CLK pulse, and then decremented by two on succeeding CLK pulses. When the count expires, OUT goes low and the Counter is reloaded with the initial count. The count is decremented by three on the next CLK pulse, and then by two on succeeding CLK pulses. When the count expires, OUT goes high again and the Counter is reloaded with the initial count. The above process is repeated indefinitely. So for odd counts, OUT will be high for (N + 1)/2 counts and low for (N - 1)/2 counts.

Mode 4: Software Triggered Mode

OUT will be initially high. When the initial count expires, OUT will go low for one CLK pulse then go high again. The counting sequence is "Triggered" by writing the initial count.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after the initial count is written.

If a new count is written during counting, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

1. Writing the first byte has no effect on counting.
2. Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the sequence to be "retriggered" by software. OUT strobes low N + 1 CLK pulses after the new count of N is written.

Mode 5: Hardware Triggered Strobe (Retriggerable)

OUT will initially be high. Counting is triggered by a rising edge of GATE. When the initial count has expired, OUT will go low for one CLK pulse and then go high again.

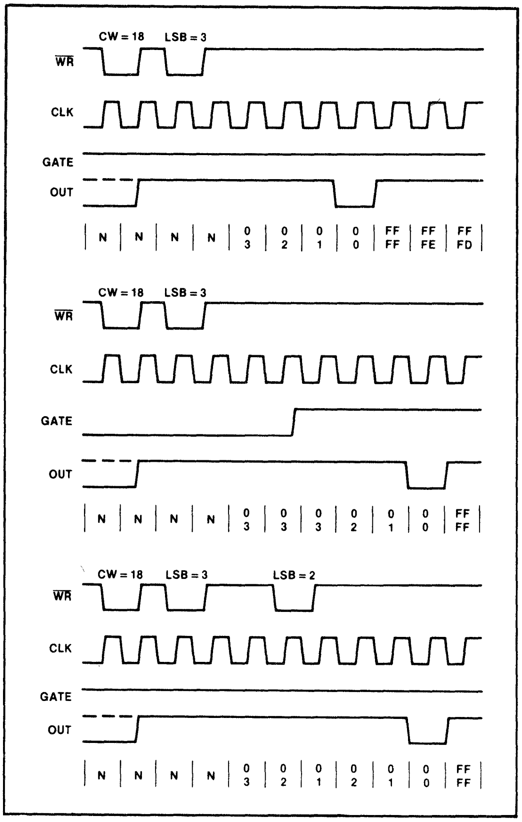


FIGURE 17. MODE 4

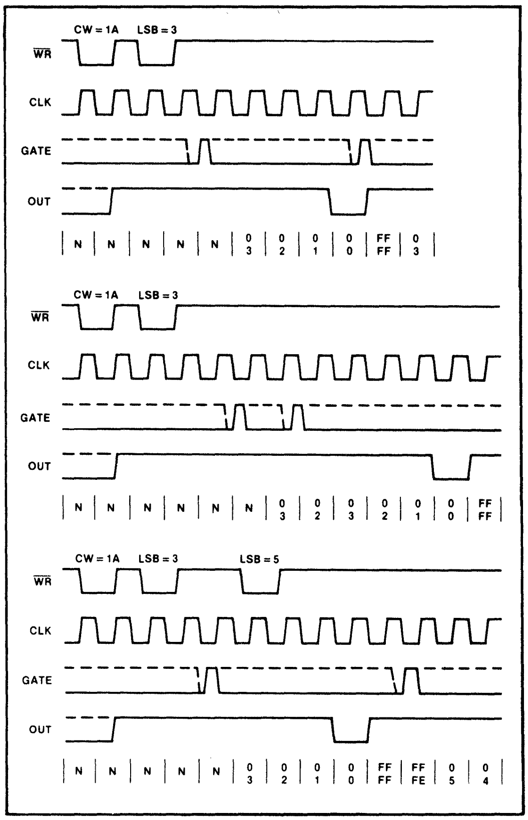


FIGURE 18. MODE 5

After writing the Control Word and initial count, the counter will not be loaded until the CLK pulse after a trigger. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after trigger.

A trigger results in the Counter being loaded with the initial count on the next CLK pulse. The counting sequence is triggerable. OUT will not strobe low for N + 1 CLK pulses after any trigger. GATE has no effect on OUT.

If a new count is written during counting, the current counting sequence will not be affected. If a trigger occurs after the new count is written but before the current count expires, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from there.

Operation Common to All Modes

Programming

When a Control Word is written to a Counter, all Control Logic is immediately reset and OUT goes to a known initial state; no CLK pulses are required for this.

Gate

The GATE input is always sampled on the rising edge of CLK. In Modes 0, 2, 3 and 4 the GATE input is level sensitive, and logic level is sampled on the rising edge of CLK. In modes 1, 2, 3 and 5 the GATE input is rising-edge sensitive. In these Modes, a rising edge of Gate (trigger) sets an edge-sensitive flip-flop in the Counter. This flip-flop is then sampled on the next rising edge of CLK. The flip-flop is reset immediately after it is sampled. In this way, a trigger will be detected no matter when it occurs - a high logic level does not have to be maintained until the next rising edge of CLK. Note that in Modes 2 and 3, the GATE input is both edge-and level-sensitive.

Counter

New counts are loaded and Counters are decremented on the falling edge of CLK.

The largest possible initial count is 0; this is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

The counter does not stop when it reaches zero. In Modes 0, 1, 4 and 5 the Counter "wraps around" to the highest count, either FFFF hex for binary counting or 9999 for BCD counting, and continues counting. Modes 2 and 3 are periodic; the Counter reloads itself with the initial count and continues counting from there.

SIGNAL STATUS MODES	LOW OR GOING LOW	RISING	HIGH
0	Disables counting	—	Enables counting
1	—	1) Initiates counting 2) Resets output after next clock	—
2	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
3	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
4	1) Disables counting	—	Enables counting
5	—	Initiates counting	—

FIGURE 19. GATE PIN OPERATIONS SUMMARY

MODE	MIN COUNT	MAX COUNT
0	1	0
1	1	0
2	2	0
3	2	0
4	1	0
5	1	0

NOTE: 0 is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

FIGURE 20. MINIMUM AND MAXIMUM INITIAL COUNTS

Absolute Maximum Ratings

Supply Voltage .... +8.0 Volts
Input, Output or I/O Voltage Applied .... GND -0.5V to VCC +0.5V
Storage Temperature Range .... -65°C to +150°C
Maximum Package Power Dissipation .... 1 Watt
θ_{jc} .... 17°C/W (CERDIP Package), 22°C/W (LCC Package)
θ_{ja} .... 54°C/W (CERDIP Package), 59°C/W (LCC Package)
Gate Count .... 2250 Gates
Junction Temperature .... +150°C
Lead Temperature (Soldering, Ten Seconds) .... +260°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Recommended Operating Conditions

Operating Voltage Range .... +4.5V to +5.5V
Operating Temperature Ranges:
C82C54 .... 0°C to +70°C
I82C54 .... -40°C to +85°C
M82C54 .... -55°C to +125°C

D. C. Electrical Specifications

VCC = 5.0V ± 10%
TA = 0°C to +70°C (C82C54)
TA = -40°C to +85°C (I82C54)
TA = -55°C to +125°C (M82C54)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	Logical One Input Voltage	2.0 2.2		V V	C82C54, I82C54 M82C54
VIL	Logical Zero Input Voltage		0.8	V	
VOH	Output High Voltage	3.0 VCC - 0.4		V V	IOH = -2.5mA IOH = -100μA
VOL	Output Low Voltage		0.4	V	IOL = +2.5mA
II	Input Leakage Current	-1.0	+1.0	μA	VIN = GND or VCC DIP Pins 9, 11, 14-16, 18-23
IO	I/O Leakage Current	-10.0	+10.0	μA	VO = GND or VCC DIP Pins 1-8
ICCSB	Standby Power Supply Current		10	μA	VCC = 5.5V VIN = VCC or GND, Outputs Open Counters Programmed
ICCOP	Operating Power Supply Current		10	mA	VCC = 5.5V CLK 0 = CLK 1 = CLK 2 = 8MHz, Outputs Open

Capacitance

TA = 25°C; VCC = GND = 0V; VIN = +5V or GND.

SYMBOL	PARAMETER	TYP	UNITS	TEST CONDITIONS
CIN	Input Capacitance	5	pF	FREQ = 1MHz Unmeasured pins returned to GND
COUT	Output Capacitance	15	pF	
CI/O	I/O Capacitance	20	pF	

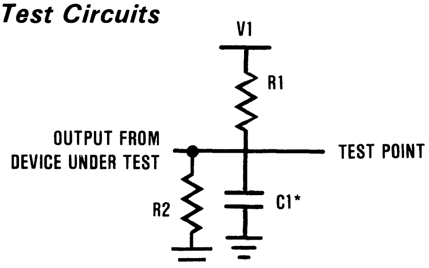
A.C. Electrical Specifications

VCC = +5V ± 10%
TA = 0°C to +70°C (C82C54)
TA = -40°C to +85°C (I82C54)
TA = -55°C to +125°C (M82C54)

BUS PARAMETERS

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
READ CYCLE					
TAR	Address Stable Before $\overline{RD}$	30		ns	1
TSR	CS Stable Before $\overline{RD}$	0		ns	
TRA	Address Hold Time After $\overline{RD}$	0		ns	
TRR	$\overline{RD}$ Pulse Width	150		ns	
TRD	Data Delay from $\overline{RD}$		120	ns	
TAD	Data Delay from Address		210	ns	
TDF	$\overline{RD}$ to Data Floating	5	85	ns	2
TRV	Command Recovery Time	200		ns	
WRITE CYCLE					
TAW	Address Stable Before $\overline{WR}$	0		ns	
TSW	CS Stable Before $\overline{WR}$	0		ns	
TWA	Address Hold Time $\overline{WR}$	0		ns	
TWW	$\overline{WR}$ Pulse Width	95		ns	
TDW	Data Setup Time Before $\overline{WR}$	140		ns	
TWD	Data Hold Time After $\overline{WR}$	25		ns	
TRV	Command Recovery Time	200		ns	
CLOCK AND GATE					
TCLK	Clock Period	125	DC	ns	1
TPWH	High Pulse Width	60		ns	1
TPWL	Low Puise Width	60		ns	1
TR	Clock Rise Time		25	ns	
TF	Clock Fall Time		25	ns	
TGW	Gate Width High	50		ns	1
TGL	Gate Width Low	50		ns	
TGS	Gate Setup Time to CLK	50		ns	
TGH	Gate Hold Time After CLK	50		ns	
TOD	Output Delay from CLK		150	ns	
TODG	Output Delay from Gate		120	ns	
TWO	OUT Delay from Mode Write		260	ns	

A.C. Test Circuits



*Includes stray and jig capacitance

TEST CONDITION	V1	R1	R2	C1
1	1.7V	523	OPEN	150pF
2	5.0V	2K	1.7K	50pF

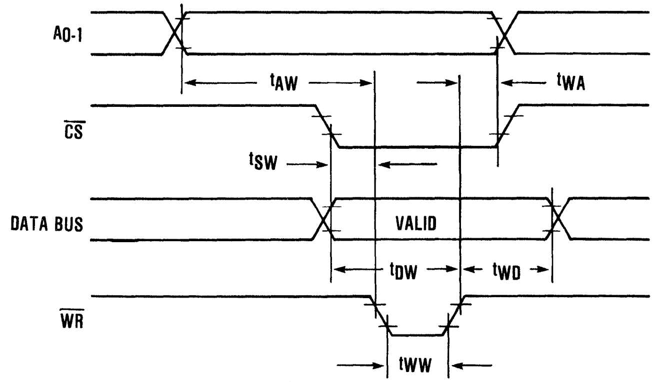
TEST CONDITION DEFINITION TABLE

A.C. Testing Input, Output Waveform

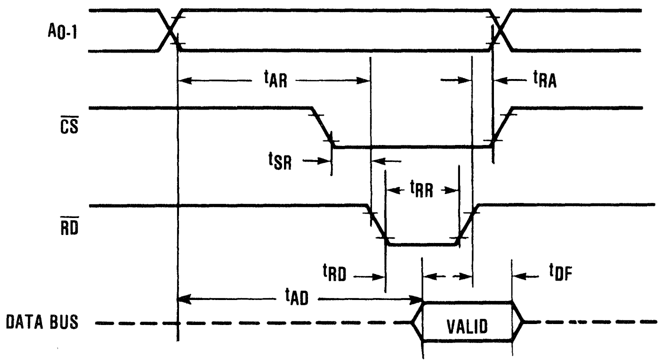
A. C. Testing: All input signals must switch between VIL -0.4V and VIH +0.4V. Input rise and fall times are driven at 1ns/V.

Waveforms

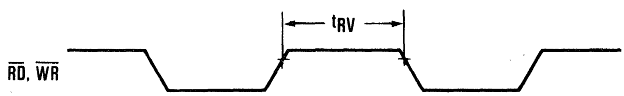
WRITE



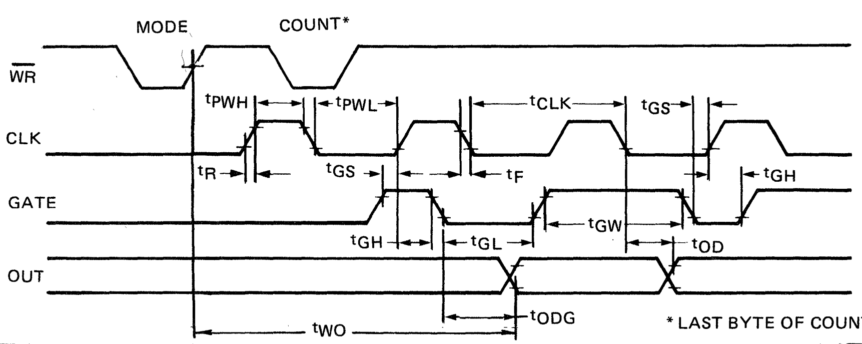
READ



RECOVERY



CLOCK AND GATE



* LAST BYTE OF COUNT BEING WRITTEN

82C55A

CMOS Programmable Peripheral Interface

Features

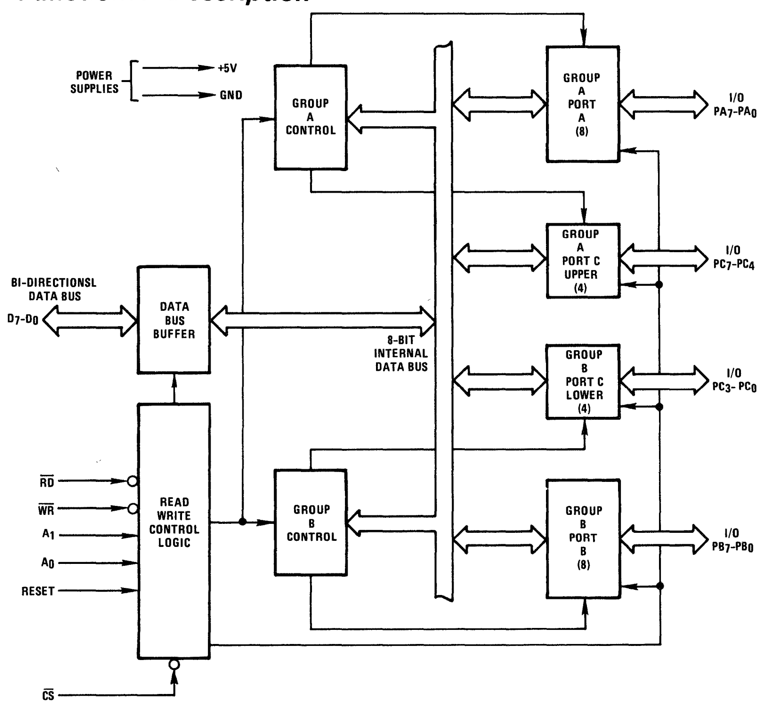
- Pin Compatible with NMOS 8255A
- 24 Programmable I/O Pins
- Fully TTL Compatible
- High Speed, No "Wait State" Operation with 5MHz and 8MHz 80C86/80C88
- Direct Bit Set/Reset Capability
- Enhanced Control Word Read Capability
- Scaled SAJI IV CMOS Process
- 2.5mA Drive Capability on All I/O Port Outputs
- Low Standby Power - ICCSB = 10μA
- Wide Operating Temperature Ranges:
  - C82C55A .... 0°C to +70°C
  - I82C55A .... -40°C to +85°C
  - M82C55A .... -55°C to +125°C

Description

The Harris 82C55A is a high performance CMOS version of the industry standard 8255A and is manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). It is a general purpose programmable I/O device which may be used with many different microprocessors. There are 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. The high performance and industry standard configuration of the 82C55A make it compatible with the 80C86, 80C88, and other microprocessors.

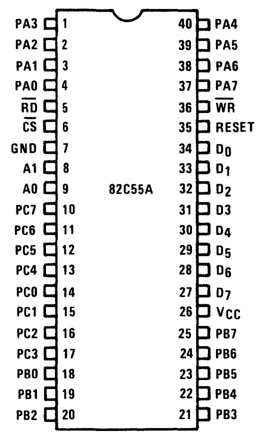
Static CMOS circuit design insures low operating power. TTL compatibility over the full temperature range and bus hold circuitry eliminate the need for pull-up resistors. The Harris advanced SAJI process results in performance equal to or greater than existing equivalent products at a fraction of the power.

Functional Description



Pinouts*

TOP VIEW



PIN NAMES

D7 - D0	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
CS	CHIP SELECT
RD	READ INPUT
WR	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V_{CC} *	+5 VOLTS
GND *	0 VOLTS

*A 0.1 μF decoupling capacitor from the V_{CC} pin to the GND pin is recommended.

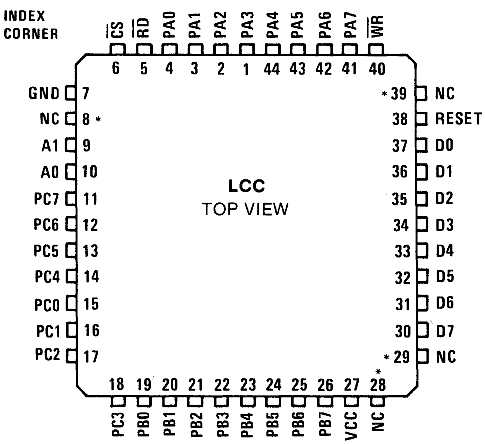
*LCC/PLCC Pinouts on Page 3-114

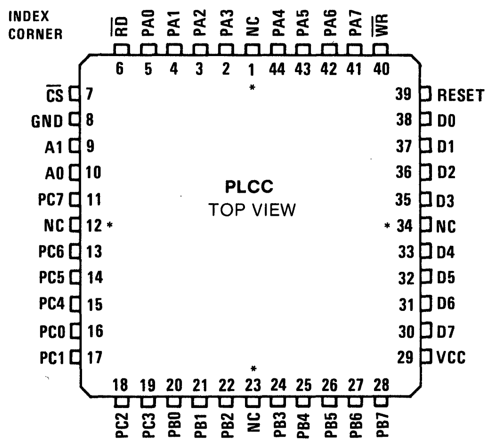
CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Pin Descriptions

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
VCC	26		VCC: the +5V power supply pin. A 0.1μF capacitor between pins 26 and 7 is recommended for decoupling.
GND	7		GROUND
D_0-D_7	27-34	I/O	DATA BUS: The Data Bus lines are bidirectional three-state pins connected to the system data bus.
RESET	35	I	RESET: A high on this input clears the control register and all ports (A, B, C) are set to the input mode with the "Bus Hold" circuitry turned on.
$\overline{\text{CS}}$	6	I	CHIP SELECT: Chip select is an active low input used to enable the 82C55A onto the Data Bus for CPU communications.
$\overline{\text{RD}}$	5	I	READ: Read is an active low input control signal used by the CPU to read status information or data via the data bus.
WR	36	I	WRITE: Write is an active low input control signal used by the CPU to load control words and data into the 82C55A
A0-A1	8, 9	I	ADDRESS: These input signals, in conjunction with the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ inputs, control the selection of one of the three ports or the control word registers A0 and A1 are normally connected to the least significant bits of the Address Bus A0, A1).
PA_0-PA_7	1-4, 37-40	I/O	PORT A: 8-Bit Input and Output Port. Both bus hold high and bus hold low circuitry are present on this port.
PB_0-PB_7	18-25	I/O	PORT B: 8-Bit input and output port. Bus hold high circuitry is present on this port.
PC_0-PC_7	10-17	I/O	PORT C: 8-Bit input and output port. Bus Hold High circuitry is present on this port.

LCC/PLCC Pinouts





No Connect

Functional Description

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to interface the 82C55A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

($\overline{CS}$)

Chip Select. A "low" on this input pin enables the communication between the 82C55A and the CPU.

($\overline{RD}$)

Read. A "low" on this input pin enables the 82C55A to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the 82C55A.

($\overline{WR}$)

Write. A "low" on this input pin enables the CPU to write data or control words into the 82C55A.

(A_0 and A_1)

Port Select 0 and Port Select 1. These input signals, in conjunction with the $\overline{RD}$ and $\overline{WR}$ inputs, control the selection of one of the three ports or the control word registers. They are normally connected to the least significant bits of the address bus (A_0 and A_1).

82C55A BASIC OPERATION

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	INPUT OPERATION (READ)
0	0	0	1	0	PORT A→DATA BUS
0	1	0	1	0	PORT B→DATA BUS
1	0	0	1	0	PORT C→DATA BUS
1	1	0	1	0	CONTROL WORD→DATA BUS
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	DATA BUS→PORT A
0	1	1	0	0	DATA BUS→PORT B
1	0	1	0	0	DATA BUS→PORT C
1	1	1	0	0	DATA BUS→CONTROL
					DISABLE FUNCTION
X	X	X	X	1	DATA BUS→3-STATE
X	X	1	1	0	DATA BUS→3-STATE

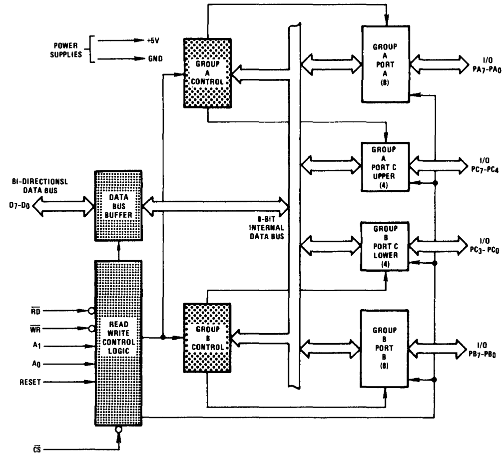


Figure 1
82C55A Block Diagram
Data Bus Buffer, Read/Write, Group A & B Control Logic Functions

(RESET)

Reset. A "high" on this input clears the control register and all ports (A, B, C) are set to the input mode. "Bus hold" devices internal to the 82C55A will hold the I/O port inputs to a logic "1" state with a maximum hold current of 400 μA.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the 82C55A. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the 82C55A.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A – Port A and Port C upper (C7-C4)

Control Group B – Port B and Port C lower (C3-C0)

The control word register can be both written and read as shown in the "Basic Operation" table. Figure 4 shows the control word format for both Read and Write operations. When the control word is read, bit D7 will always be a logic "1", as this implies control word mode information.

Ports A, B and C

The 82C55A contains three 8-bit ports (A, B, and C). All can be configured to a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 82C55A.

Port A One 8-bit data output latch/buffer and one 8-bit data input latch. Both "pull-up" and "pull-down" bus-hold devices are present on Port A. See Figure 2a.

Port B One 8-bit data input/output latch/buffer and one 8-bit data input buffer. See Figure 2b.

Port C One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B. See Figure 2b.

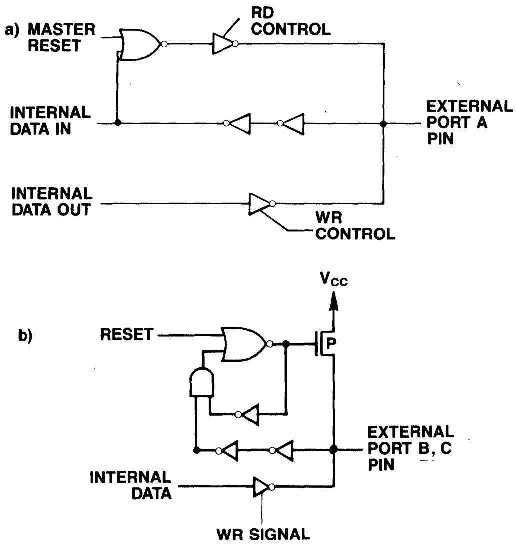


Figure 2
Port A & B, Port C Bus-hold Configuration

Operational Description

Mode Selection

There are three basic modes of operation that can be selected by the system software:

Mode 0 – Basic Input/Output
Mode 1 – Strobed Input/Output
Mode 2 – Bi-Directional Bus

When the reset input goes "high", all ports will be set to the input mode with all 24 port lines held at a logic "one" level by internal bus hold devices. After the reset is removed, the 82C55A can remain in the input mode with no additional initialization required. This eliminates the need for pullup or pulldown resistors in all-CMOS designs. During the execution of the system program, any of the other modes may be selected using a single output instruction. This allows a single 82C55A to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance: Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

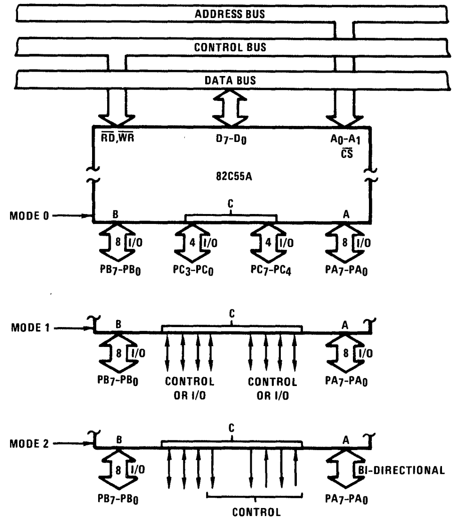


Figure 3
Basic Mode Definitions and Bus Interface

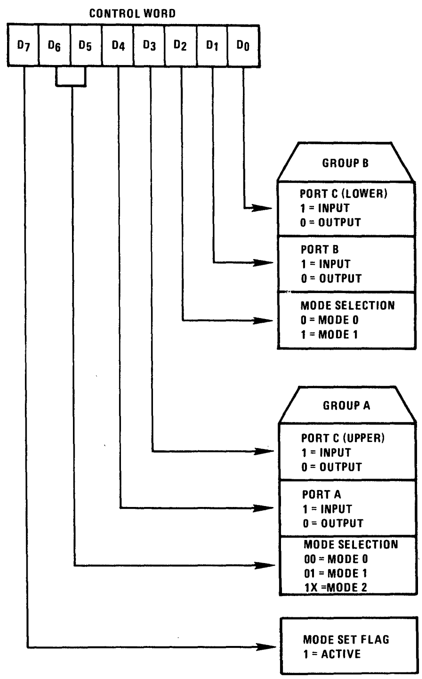


Figure 4
Mode Definition Format

The mode definitions and possible mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 82C55A has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

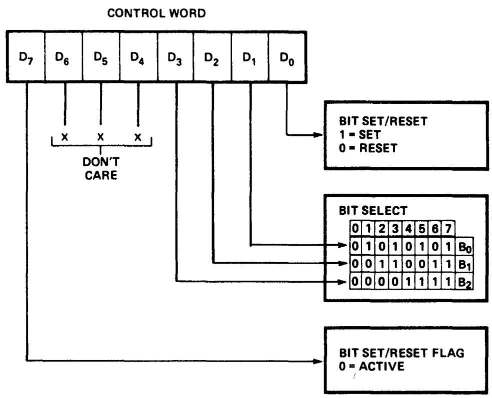


Figure 5
Bit Set/Reset Format

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction. This feature reduces software requirements in control-based applications.

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

Interrupt Control Functions

When the 82C55A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the programmer to enable or disable a CPU interrupt by a specific I/O device without affecting any other device in the interrupt structure.

INTE flip-flop definition:

(BIT-SET)–INTE is SET – Interrupt enable
(BIT-RESET)–INTE is RESET – Interrupt disable.

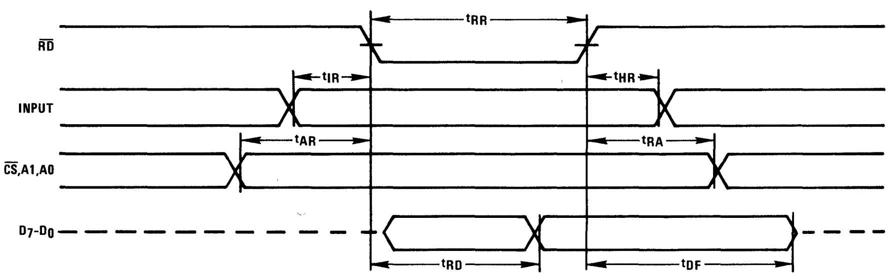
Note: All Mask flip-flops are automatically reset during mode selection and device Reset.

Operating Modes

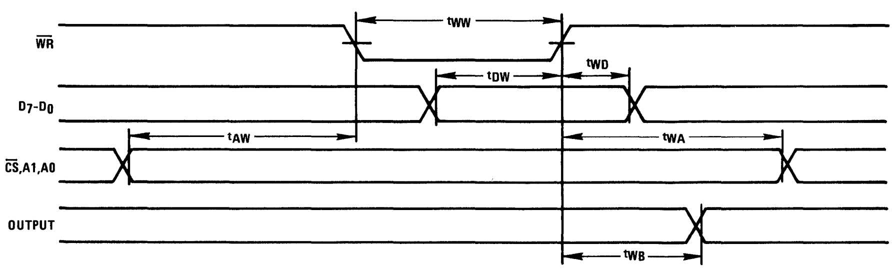
Mode O (Basic Input/Output). This functional configuration provides simple input and output operations for each of the three ports. No handshaking is required, data is simply written to or read from a specific port.

Mode O Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports
- Any port can be input or output
- Outputs are latched
- Inputs are not latched
- 16 different Input/Output configurations possible



MODE 0 (Basic Input)

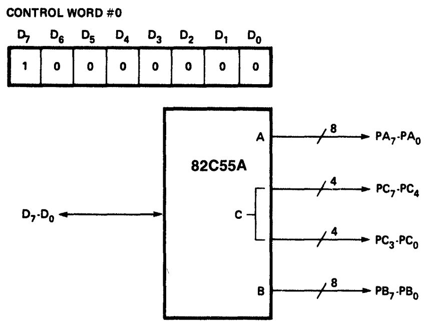


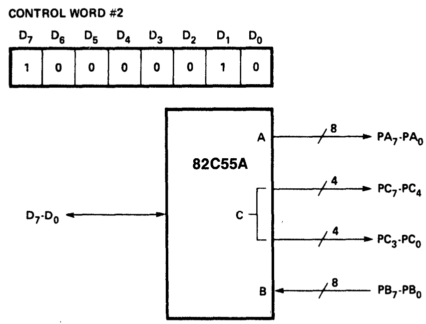
MODE 0 (Basic Output)

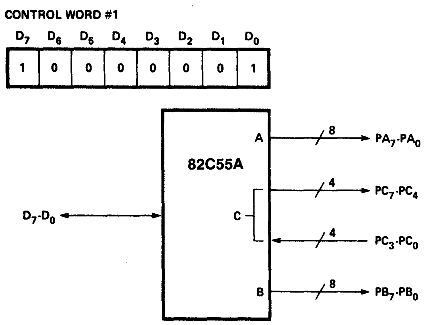
MODE 0 Port Definition

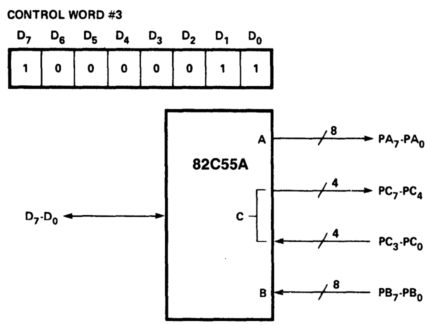
A		B		GROUP A			GROUP B	
D_4	D_3	D_1	D_0	PORT A	PORT C (UPPER)	#	PORT B	PORT C (LOWER)
0	0	0	0	OUTPUT	OUTPUT	0	OUTPUT	OUTPUT
0	0	0	1	OUTPUT	OUTPUT	1	OUTPUT	INPUT
0	0	1	0	OUTPUT	OUTPUT	2	INPUT	OUTPUT
0	0	1	1	OUTPUT	OUTPUT	3	INPUT	INPUT
0	1	0	0	OUTPUT	INPUT	4	OUTPUT	OUTPUT
0	1	0	1	OUTPUT	INPUT	5	OUTPUT	INPUT
0	1	1	0	OUTPUT	INPUT	6	INPUT	OUTPUT
0	1	1	1	OUTPUT	INPUT	7	INPUT	INPUT
1	0	0	0	INPUT	OUTPUT	8	OUTPUT	OUTPUT
1	0	0	1	INPUT	OUTPUT	9	OUTPUT	INPUT
1	0	1	0	INPUT	OUTPUT	10	INPUT	OUTPUT
1	0	1	1	INPUT	OUTPUT	11	INPUT	INPUT
1	1	0	0	INPUT	INPUT	12	OUTPUT	OUTPUT
1	1	0	1	INPUT	INPUT	13	OUTPUT	INPUT
1	1	1	0	INPUT	INPUT	14	INPUT	OUTPUT
1	1	1	1	INPUT	INPUT	15	INPUT	INPUT

MODE 0 Configurations



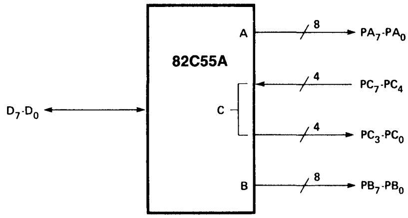






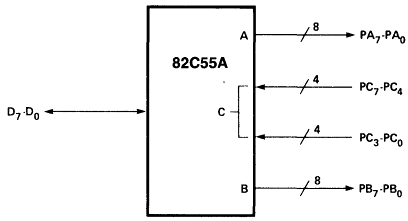
CONTROL WORD #4

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	0	0



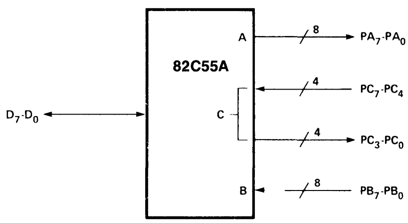
CONTROL WORD #5

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	0	1



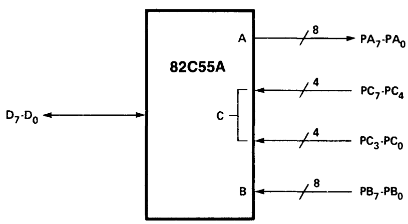
CONTROL WORD #6

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	1	0



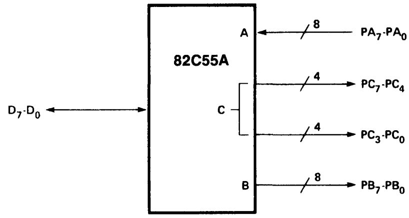
CONTROL WORD #7

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	1	1



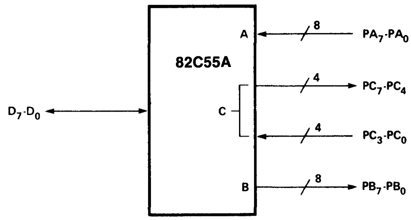
CONTROL WORD #8

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	0	0



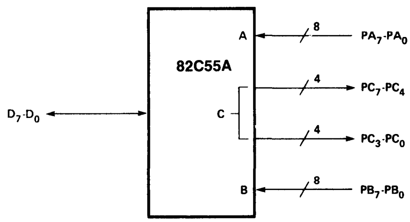
CONTROL WORD #9

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	0	1



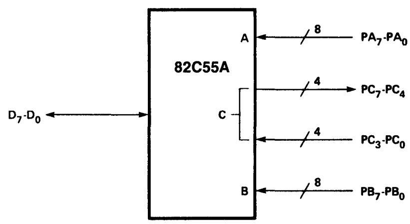
CONTROL WORD #10

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	1	0



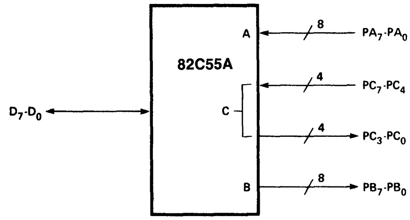
CONTROL WORD #11

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	1	1



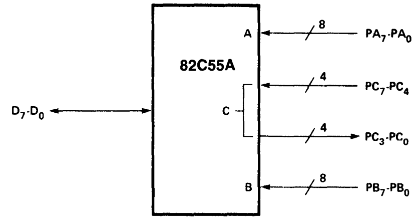
CONTROL WORD #12

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	1	0	0	0



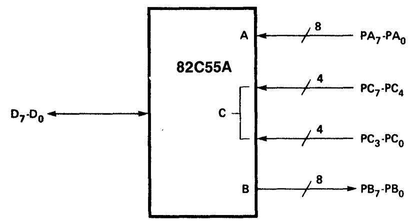
CONTROL WORD #14

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
[illegible]	0	0	1	1	0	1	0



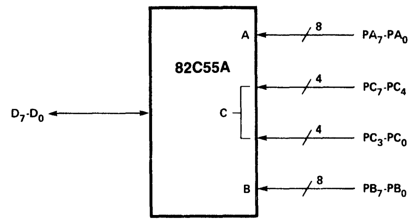
CONTROL WORD #13

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	1	0	0	1



CONTROL WORD #15

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	1	0	1	1



Operating Modes

Mode 1 (Strobed Input/Output). This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In mode 1, port A and port B use the lines on port C to generate or accept these "handshaking" signals.

Mode 1 Basic Functional Definitions:

- Two Groups (Group A and Group B)
- Each group contains one 8-bit port and one 4-bit control/data port.
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit port.

Input Control Signal Definition

$\overline{STB}$ (Strobe Input)

A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement. IBF is set by $\overline{STB}$ input being low and is reset by the rising edge of the $\overline{RD}$ input.

INTR (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the condition: $\overline{STB}$ is a "one", IBF is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{RD}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A

Controlled by bit set/reset of PC_4.

INTE B

Controlled by bit set/reset of PC_2.

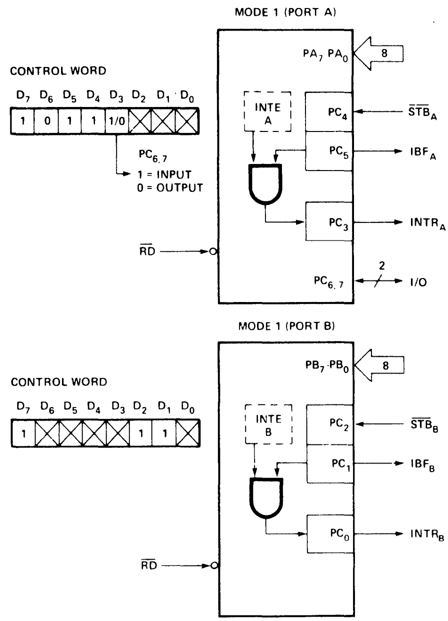


Figure 6
MODE 1 Input

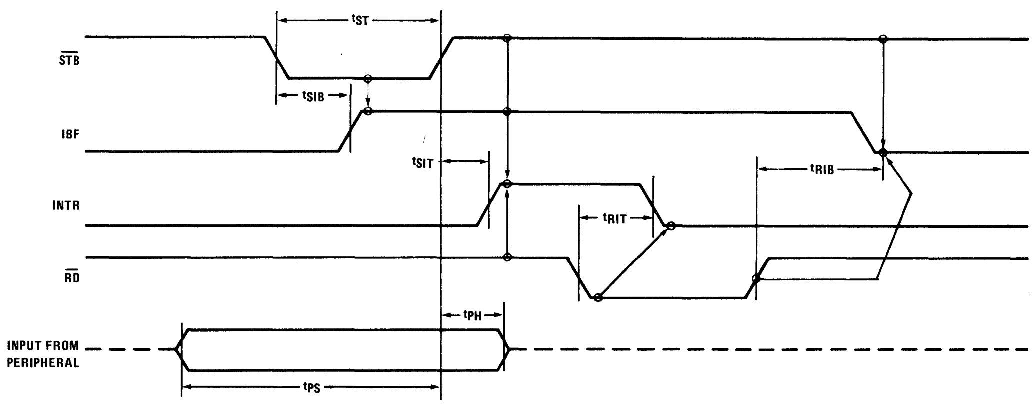


Figure 7
MODE 1 (Strobed Input)

OUTPUT CONTROL SIGNAL DEFINITION

OBF (Output Buffer Full F/F). The OBF output will go "low" to indicate that the CPU has written data out to the specified port. This does not mean valid data is sent out of the part at this time since OBF can go true before data is available. Data is guaranteed valid at the rising edge of OBF. See Note 1. The OBF F/F will be set by the rising edge of the WR input and reset by ACK Input being low.

ACK (Acknowledge Input). A "low" on this input informs the 82C55A that the data from Port A or Port B is ready to be accepted. In essence, a reponse from the peripheral device indicating that it is ready to accept data. See Note 1.

INTR (Interrupt Request). A "high" on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when ACK is a "one", OBF is a "one" and INTE is a "one". It is reset by the falling edge of WR.

INTE A

Controlled by Bit Set/Reset of PC6.

INTE B

Controlled by Bit Set/Reset of PC2.

NOTE:
To strobe data into the peripheral device, the user must operate the strobe line in a hand shaking mode. The user needs to send OBF to the peripheral device, generate an ACK from the peripheral device and then latch data into the peripheral device on the rising edge of OBF.

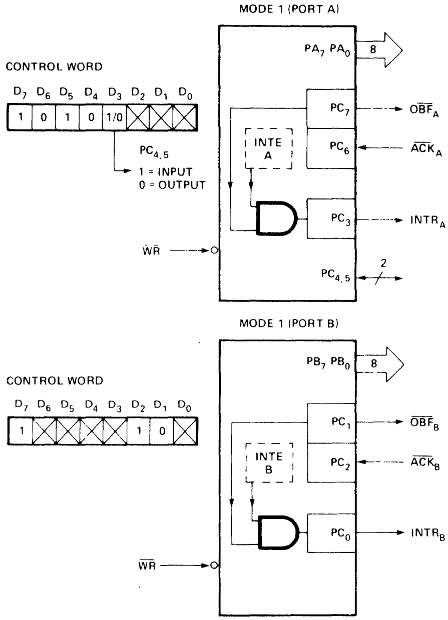


Figure 8
MODE 1 Output

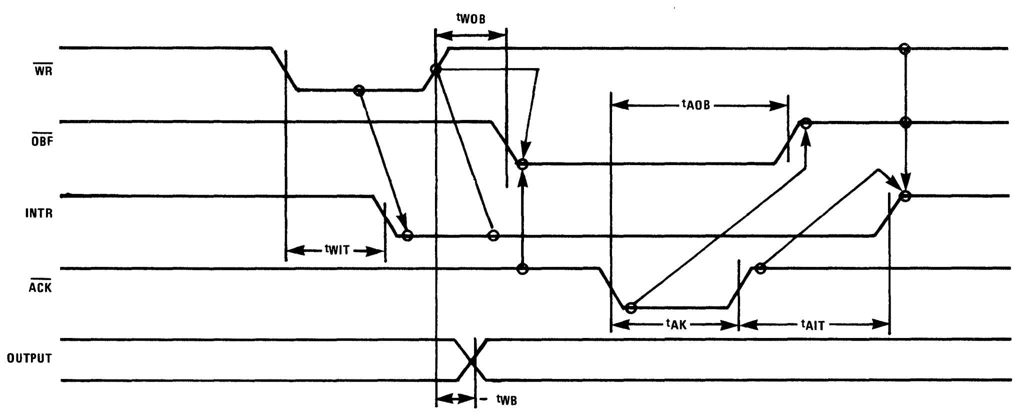


Figure 9
MODE 1 (Strobed Output)

Combinations of MODE 1: Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.

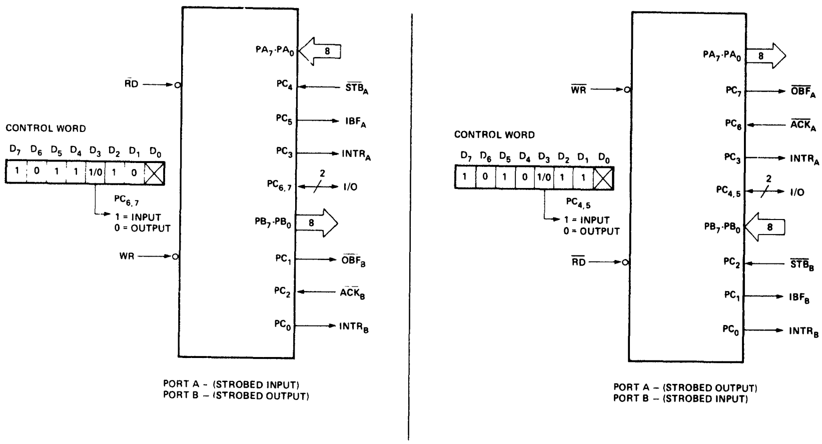


Figure 10
Combinations of MODE 1

Operating Modes

MODE 2 (Strobed Bidirectional Bus I/O)

The functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline similar to MODE 1. Interrupt generation and enable/disable functions are also available.

MODE 2 Basic Functional Definitions:

- Used in Group A only.
- One 8-bit, bi-directional bus Port (Port A) and a 5-bit control Port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A).

Bidirectional Bus I/O Control Signal Definition

INTR (Interrupt Request). A high on this output can be used to interrupt the CPU for both input or output operations.

Output Operations

$\overline{OBF}$ (Output Buffer Full). The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to port A.

$\overline{ACK}$ (Acknowledge). A "low" on this input enables the tri-state output buffer of port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE 1 (The INTE Flip-Flop Associated with $\overline{OBF}$). Controlled by bit set/reset of PC_6.

Input Operations

$\overline{STB}$ (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F). A "high" on this output indicates that data has been loaded into the input latch.

INTE 2 (The INTE Flip-Flop Associated with IBF). Controlled by bit set/reset of PC_4.

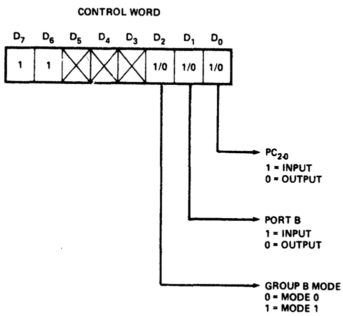


Figure 11. MODE Control Word

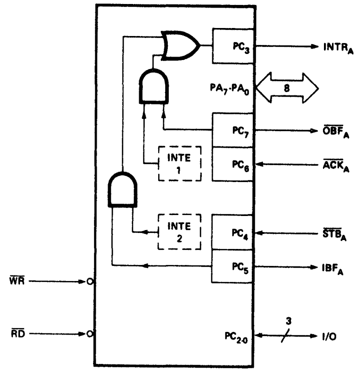


Figure 12. MODE 2

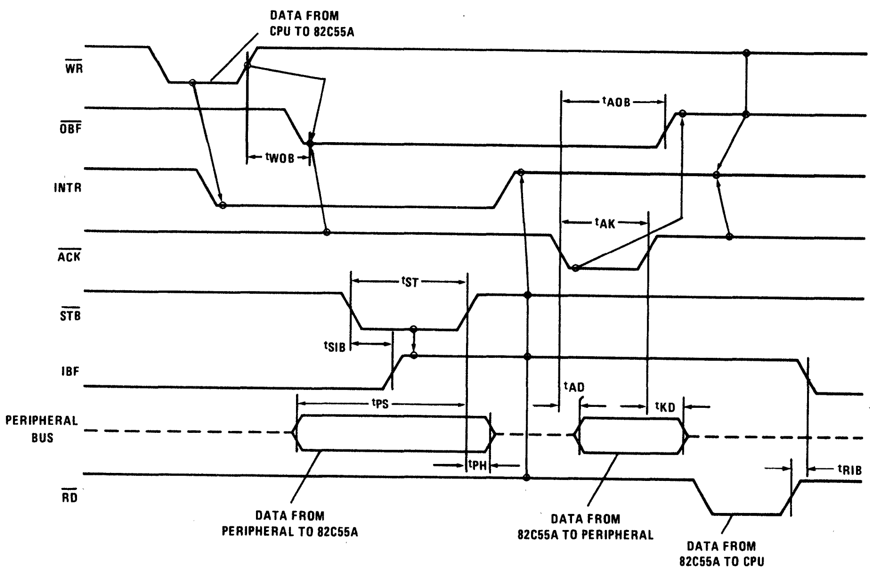


Figure 13. MODE 2 (Bidirectional)

Note: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible. ($INTR = IBF \cdot MASK \cdot \overline{STB} \cdot \overline{RD} + \overline{OBF} \cdot MASK \cdot \overline{ACK} \cdot \overline{WR}$)

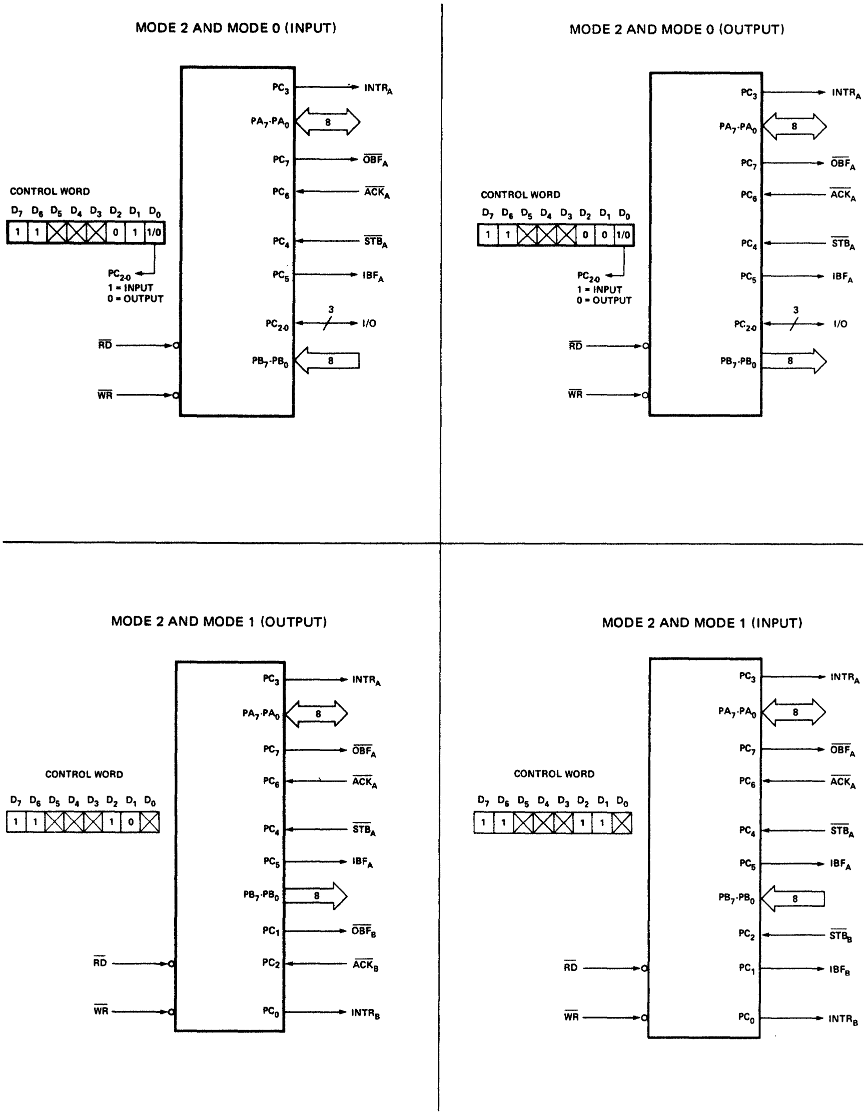


Figure 14

MODE 2 Combinations

Mode Definition Summary

	MODE 0		MODE 1		MODE 2
	IN	OUT	IN	OUT	GROUP A ONLY
PA_0	IN	OUT	IN	OUT	↔
PA_1	IN	OUT	IN	OUT	↔
PA_2	IN	OUT	IN	OUT	↔
PA_3	IN	OUT	IN	OUT	↔
PA_4	IN	OUT	IN	OUT	↔
PA_5	IN	OUT	IN	OUT	↔
PA_6	IN	OUT	IN	OUT	↔
PA_7	IN	OUT	IN	OUT	↔
PB_0	IN	OUT	IN	OUT	— (MODE 0 OR MODE 1 ONLY)
PB_1	IN	OUT	IN	OUT	—
PB_2	IN	OUT	IN	OUT	—
PB_3	IN	OUT	IN	OUT	—
PB_4	IN	OUT	IN	OUT	—
PB_5	IN	OUT	IN	OUT	—
PB_6	IN	OUT	IN	OUT	—
PB_7	IN	OUT	IN	OUT	—
PC_0	IN	OUT	$INTR_B$	$INTR_B$	I/O
PC_1	IN	OUT	IBF_B	$\overline{OBF}_B$	I/O
PC_2	IN	OUT	$\overline{STB}_B$	$\overline{ACK}_B$	I/O
PC_3	IN	OUT	$INTR_A$	$INTR_A$	$INTR_A$
PC_4	IN	OUT	$\overline{STB}_A$	I/O	$\overline{STB}_A$
PC_5	IN	OUT	IBF_A	I/O	IBF_A
PC_6	IN	OUT	I/O	$\overline{ACK}_A$	$\overline{ACK}_A$
PC_7	IN	OUT	I/O	$\overline{OBF}_A$	$\overline{OBF}_A$

Special Mode Combination Considerations:

There are several combinations of modes possible. For any combination, some or all of Port C lines are used for control or status. The remaining bits are either inputs or outputs as defined by a "Set Mode" command.

INPUT CONFIGURATION

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
I/O	I/O	IBF_A	$INTE_A$	$INTR_A$	$INTE_B$	IBF_B	$INTR_B$
GROUP A					GROUP B		

OUTPUT CONFIGURATION

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
$\overline{OBF}_A$	$INTE_A$	I/O	I/O	$INTR_A$	$INTE_B$	$\overline{OBF}_B$	$INTR_B$
GROUP A					GROUP B		

Figure 15. MODE 1 Status Word Format

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
$\overline{OBF}_A$	$INTE_1$	IBF_A	$INTE_2$	$INTR_A$	X	X	X
GROUP A					GROUP B		

(DEFINED BY MODE 0 OR MODE 1 SELECTION)

Figure 16. MODE 2 Status Word Format

During a read of Port C, the state of all the Port C lines, except the $\overline{ACK}$ and $\overline{STB}$ lines, will be placed on the data bus. In place of the $\overline{ACK}$ and $\overline{STB}$ line states, flag status will appear on the data bus in the PC2, PC4, and PC6 bit positions as illustrated by Figure 17.

Through a "Write Port C" command, only the Port C pins programmed as outputs in a Mode 0 group can be written. No other pins can be affected by a "Write Port C" command, nor can the interrupt enable flags be accessed. To write to any Port C output programmed as an output in a Mode 1 group or to change an interrupt enable flag, the "Set/Reset Port C Bit" command must be used.

With a "Set/Reset Port C Bit" command, any Port C line programmed as an output (including INTR, IBF and OBF) can be written, or an interrupt enable flag can be either set or reset. Port C lines programmed as inputs, including $\overline{ACK}$ and $\overline{STB}$ lines, associated with Port C are not affected by a "Set/Reset Port C Bit" command. Writing to the corresponding Port C bit positions of the $\overline{ACK}$ and $\overline{STB}$ lines with the "Set/Reset Port C Bit" command will affect the Group A and Group B interrupt enable flags, as illustrated in Figure 17.

Interrupt Enable Flag*	Position	Alternate Port C Pin Signal (Mode)
INTE B	PC2	$\overline{ACK_B}$ (Output Mode 1) or $\overline{STB_B}$ (Input Mode 1)
INTE A2	PC4	$\overline{STB_A}$ (Input Mode 1 or Mode 2)
INTE A1	PC6	$\overline{ACK_A}$ (Output Mode 1 or Mode 2)

Figure 17
Interrupt Enable Flags in Modes 1 and 2

Current Drive Capability:

Any output on Port A, B or C can sink or source 2.5mA. This feature allows the 82C55A to directly drive Darlington type drivers and high-voltage displays that require such sink or source current.

Reading Port C Status

In Mode 0, Port C transfers data to or from the peripheral device. When the 82C55A is programmed to function in Modes 1 or 2, Port C generates or accepts "hand-shaking" signals with the peripheral device. Reading the contents of Port C allows the programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is no special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

APPLICATIONS OF THE 82C55A

The 82C55A is a very powerful tool for interfacing peripheral equipment to the microcomputer system. It represents the optimum use of available pins and is flexible enough to interface almost any I/O device without the need for additional external logic.

Each peripheral device in a microcomputer system usually has a "service routine" associated with it. The routine manages the software interface between the device and the CPU. The functional definition of the 82C55A is programmed by the I/O service routine and becomes an extension of the system software. By examining the I/O devices interface characteristics for both data transfer and timing, and matching this information to the examples and tables in the detailed operational description, a control word can easily be developed to initialize the 82C55A to exactly "fit" the application. Figures 18 through 24 present a few examples of typical applications of the 82C55A.

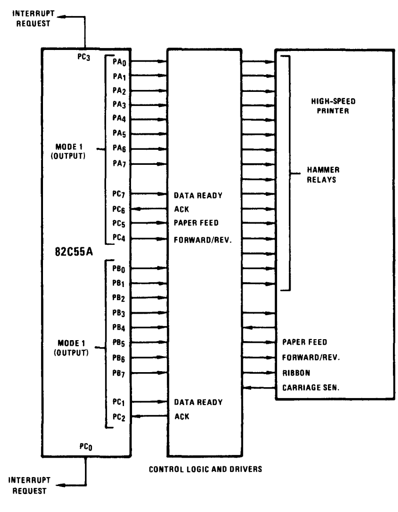


Figure 18. Printer Interface

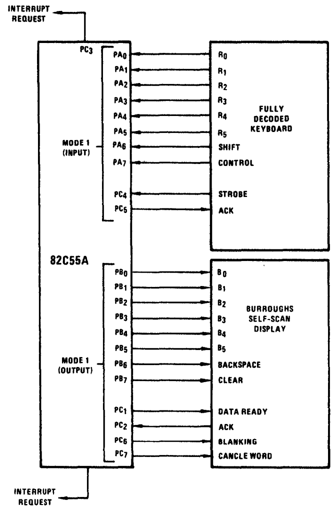


Figure 19. Keyboard and Display Interface

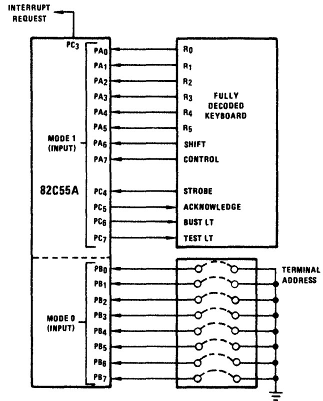


Figure 20. Keyboard and Terminal Address Interface

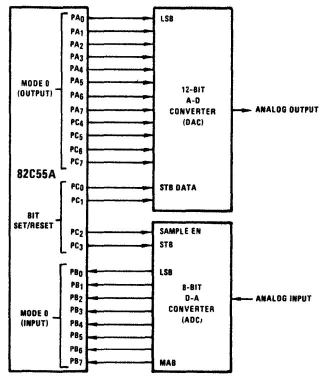


Figure 21. Digital to Analog, Analog to Digital

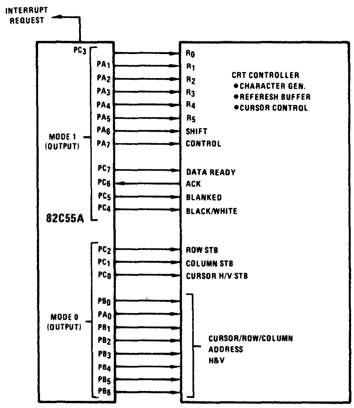


Figure 22. Basic CRT Controller Interface

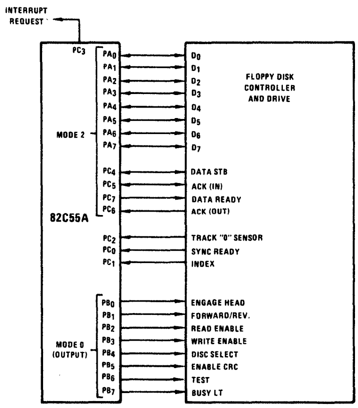


Figure 23. Basic Floppy Disc Interface

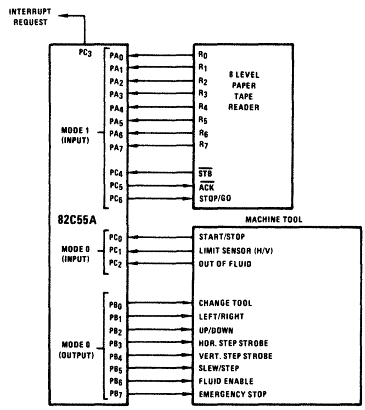


Figure 24. Machine Tool Controller Interface

Absolute Maximum Ratings

Supply Voltage	+8.0 Volts
Input, Output or I/O Voltage Applied	GND -0.5V to VCC +0.5V
Storage Temperature Range	-65°C to +150°C
Maximum Package Power Dissipation	1 Watt
θ_{jc}	22°C/W (CERDIP Package), 27°C/W (LCC Package)
θ_{ja}	55°C/W (CERDIP Package), 60°C/W (LCC Package)
Gate Count	1,000 Gates
Junction Temperature	+150°C
Lead Temperature (Soldering, Ten Seconds)	+260°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range	+4.5V to +5.5V
Operating Temperature Range	
C82C55A	0°C to +70°C
I82C55A	-40°C to +85°C
M82C55A	-55°C to +125°C

D.C. Electrical Specifications

VCC = 5.0V ± 10%; T_A = 0°C to +70°C (C82C55A); T_A = -40°C to +85°C (I82C55A); T_A = -55°C to +125°C (M82C55A)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	Logical One Input Voltage	2.0 2.2		V V	I82C55A, C82C55A, M82C55A
VIL	Logical Zero Input Voltage		0.8	V	
VOH	Logical One Output Voltage	3.0 VCC -0.4		V V	IOH = -2.5mA IOH = -100μA
VOL	Logical Zero Output Voltage		0.4	V	IOL = +2.5mA
II	Input Leakage Current	-1.0	1.0	μA	VIN = VCC OR GND, DIP Pins: 5, 6, 8, 9, 35, 36
IO	I/O Pin Leakage Current	-10.0	10.0	μA	VO = VCC or GND DIP Pins: 27-34
IBHH	Bus Hold High Current	-50	-400	μA	VO = 3.0V Ports A, B, C
IBHL	Bus Hold Low Current	+50	+400	μA	VO = 1.0V PORT A ONLY
IDAR	Darlington Drive Current	-2.0	Note 1	mA	PORTS A, B, C Test Condition 3
ICCSB	Standby Power Supply Current		10	μA	VCC = 5.5V, VIN = VCC or GND Outputs Open
ICCOP	Operating Power Supply Current		1	mA/MHz	T_A = +25°C, VCC = 5.0V, Typical (See Note 2)

NOTES: 1. No internal current limiting exists on Port Outputs. A resistor must be added externally to limit the current.
2. ICCOP = 1mA/MHz of Peripheral Read/Write cycle time. (Example: 1.0μs I/O Read/Write cycle time = 1mA).

Capacitance

T_A = 25°C; VCC = GND = 0V; VIN = +5V or GND.

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_{IN}	Input Capacitance	5	pF	FREQ = 1MHz Unmeasured pins returned to GND
$C_{I/O}$	I/O Capacitance	20	pF	

A.C. Electrical Specifications

VCC = +5V ± 10%, GND = 0V; T_A = −55°C to +125°C (M82C55A) (M82C55A-5)
VCC = +5V ± 10%, GND = 0V; T_A = −40°C to +85°C (I82C55A) (I82C55A-5)
VCC = +5V ± 10%, GND = 0V; T_A = 0°C to +70°C (C82C55A) (C82C55A-5)

Bus Parameters

READ

SYMBOL	PARAMETER	82C55A MIN	82C55A MAX	82C55A-5 MIN	82C55A-5 MAX	UNITS	TEST CONDITIONS
tAR	Address Stable Before READ	0		0		ns	
tRA	Address Stable After READ	0		0		ns	
tRR	READ Pulse Width	150		250		ns	
tRD	Data Valid From READ		120		200	ns	1
tDF	Data Float After READ	10	75	10	75	ns	2
tRV	Time Between READs and/or WRITEs	300		300		ns	

WRITE

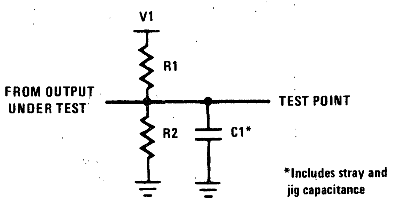
SYMBOL	PARAMETER	82C55A MIN	82C55A MAX	82C55A-5 MIN	82C55A-5 MAX	UNITS	TEST CONDITIONS
tAW	Address Stable Before WRITE	0		0		ns	
tWA	Address Stable After WRITE	20		20		ns	
tWW	WRITE Pulse Width	100		100		ns	
tDW	Data Valid to WRITE High	100		100		ns	
tWD	Data Valid After WRITE High	30		30		ns	

OTHER TIMINGS

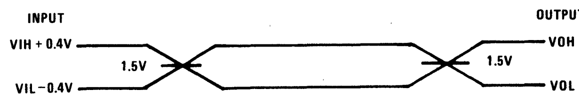
SYMBOL	PARAMETER	82C55A MIN	82C55A MAX	82C55A-5 MIN	82C55A-5 MAX	UNITS	TEST CONDITIONS
tWB	WR = 1 to Output		350		350	ns	1
tIR	Peripheral Data Before RD	0		0		ns	
tHR	Peripheral Data After RD	0		0		ns	
tAK	ACK Pulse Width	200		200		ns	
tST	STB Pulse Width	100		100		ns	
tPS	Per. Data Before STB High	20		20		ns	
tPH	Per. Data After STB High	50		50		ns	
tAD	ACK = 0 to Output		175		175	ns	1
tKD	ACK = 1 to Output Float	20	250	20	250	ns	2
tWOB	WR = 1 to OBF = 0		150		150	ns	1
tAOB	ACK = 0 to OBF = 1		150		150	ns	1
tSIB	STB = 0 to IBF = 1		150		150	ns	1
tRIB	RD = 1 to IBF = 0		150		150	ns	1
tRIT	RD = 0 to INTR = 0		200		200	ns	1
tSIT	STB = 1 to INTR = 1		150		150	ns	1
tAIT	ACK = 1 to INTR = 1		150		150	ns	1
tWIT	WR = 0 to INTR = 0		200		200	ns	1
tRES	Reset Pulse Width	500		500		ns	see note 1

Note 1. Period of initial Reset pulse after power-on must be at least 50μsec. Subsequent Reset pulses may be 500ns minimum.

A. C. Test Circuit



A.C. Testing Input, Output Waveforms



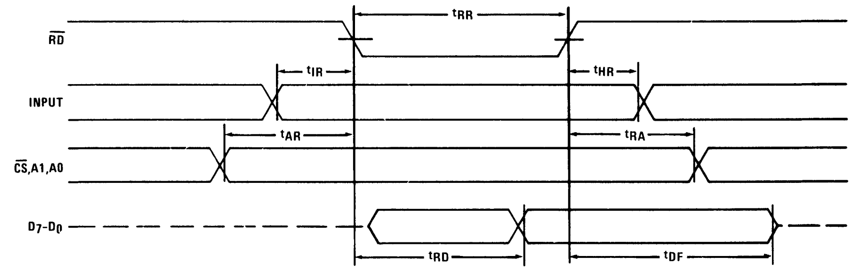
A.C. Testing: All parameters tested as per test circuits. Input rise and fall times are driven at 1ns/V.

TEST CONDITION	V1	R1	R2	C1
1	1.7V	523Ω	OPEN	150 pf
2	5.0V	2KΩ	1.7KΩ	50 pf
3	1.5V	750Ω	OPEN	OPEN

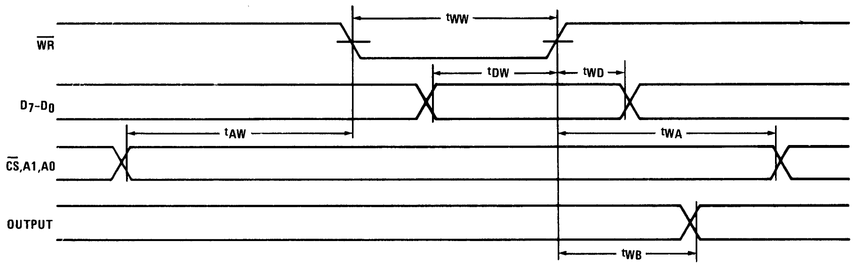
TEST CONDITION DEFINITION TABLE

Waveforms

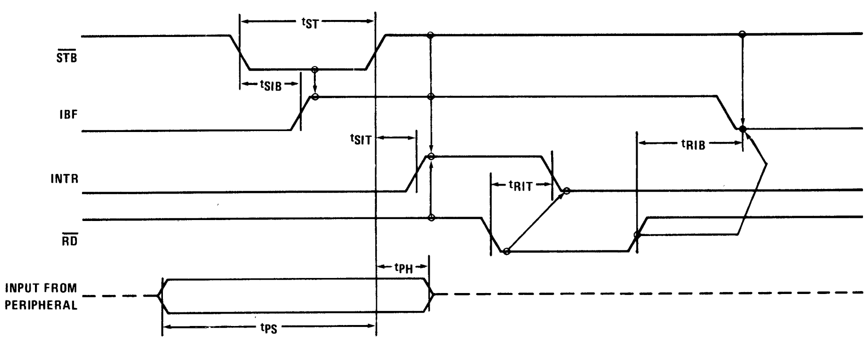
MODE 0 (BASIC INPUT)



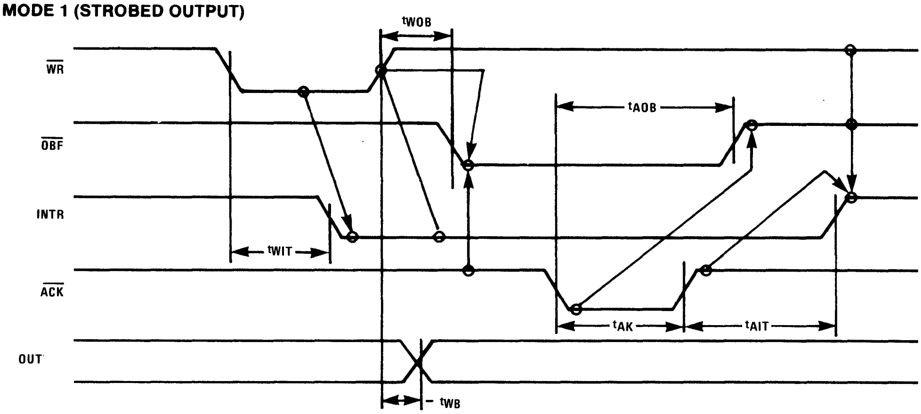
MODE 0 (BASIC OUTPUT)



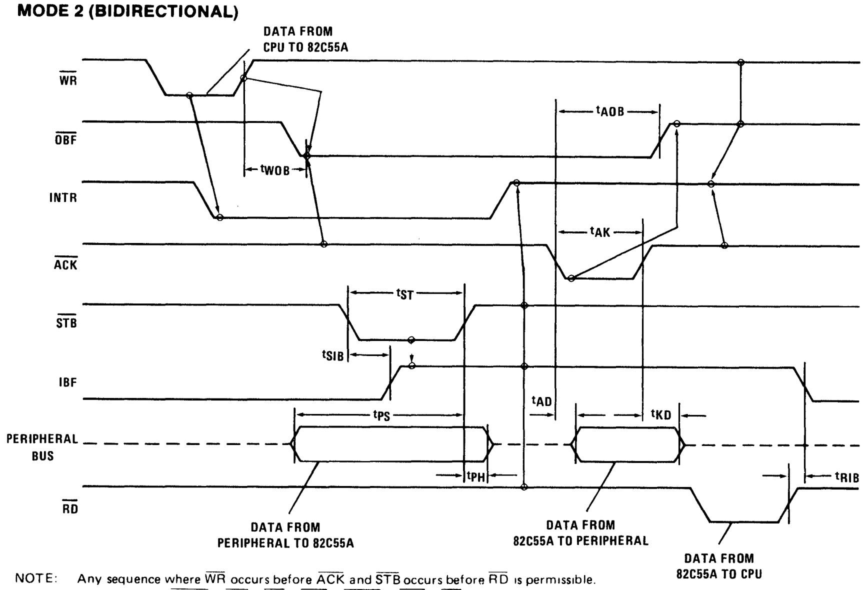
MODE 1 (STROBED INPUT)



MODE 1 (STROBED OUTPUT)

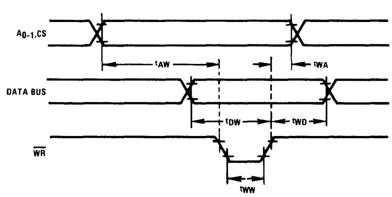


MODE 2 (BIDIRECTIONAL)

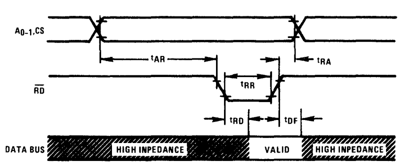


NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
(INTR = IBF • $\overline{MASK}$ • $\overline{STB}$ • $\overline{RD}$ + $\overline{OBF}$ • $\overline{MASK}$ • $\overline{ACK}$ • $\overline{WR}$)

WRITE TIMING



READ TIMING



HARRIS

82C59A

CMOS Priority Interrupt Controller

REFERENCE PAGE 3-203 FOR APPLICATION NOTE 109

Features

- Pin Compatible with NMOS 8259A
- 8MHz and 5MHz Versions Available
- Eight Level Priority Controller, Expandable to 64 Levels
- Fully TTL Compatible
- High Speed, No "Wait State" Operation with 8MHz 80C86 and 80C88
- Programmable Interrupt Modes
- 8080/8085 and 8086/80C86/80C88 Compatible Operation
- Individual Request Mask Capatibility
- Fully Static Design
- Scaled SAJI IV CMOS Process
- Single 5V Power Supply
- Low Standby Power — 10μA Maximum
- Wide Operating Temperature Ranges:
  - ▸ C82C59A .... 0°C to +70°C
  - ▸ I82C59A .... -40°C to +85°C
  - ▸ M82C59A .... -55°C to +125°C

Description

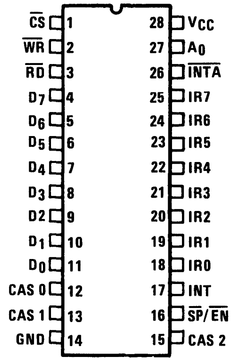
The Harris 82C59A is a high performance CMOS Priority Interrupt controller manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). The 82C59A is designed to relieve the system CPU from the task of polling in a multi-level priority interrupt system. The high speed and industry standard configuration of the 82C59A make it compatible with microprocessors such as the 80C86, 80C88, 8086, 8080/85 and NSC800.

The 82C59A can handle up to eight vectored priority interrupting sources and is cascadable to 64 without additional circuitry.Individual interrupting sources can be masked or prioritized to allow custom system configuration. Two modes of operation make the 82C59A compatible with both 8080/85 and 80C86/88 formats.

Static CMOS circuit design insures low operaing power. Harris advanced SAJI process results in performance equal to or greater than existing equivalent products at a fraction of the power.

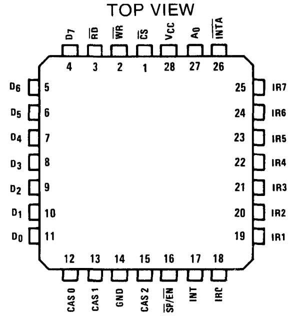
Pinouts

TOP VIEW

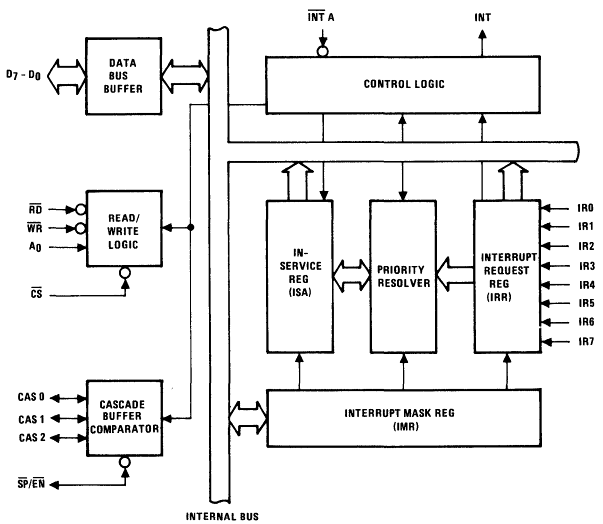


LCC/PLCC

TOP VIEW



Functional Diagram



D_7-D_0	DATA BUS (BI-DIRECTIONAL)
RD	READ INPUT
WR	WRITE INPUT
A_0	COMMAND SELECT ADDRESS
CS	CHIP SELECT
CAS 2 - CAS 0	CASCADE LINES
SP/EN	SLAVE PROGRAM INPUT ENABLE
INT	INTERRUPT OUTPUT
INTA	INTERRUPT ACKNOWLEDGE INPUT
IR0 - IR7	INTERRUPT REQUEST INPUTS

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Pin Description

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
V_{CC}	28	I	V_{CC}: The +5V power supply pin. A 0.1μF capacitor between pins 14 and 28 is recommended for decoupling.
GND	14	I	GROUND
$\overline{CS}$	1	I	CHIP SELECT: A low on this pins enables $\overline{RD}$ and $\overline{WR}$ communications between the CPU and the 82C59A. INTA functions are independent of $\overline{CS}$.
$\overline{WR}$	2	I	WRITE: A low on this pin when $\overline{CS}$ is low enables the 82C59A to accept command words form the CPU.
$\overline{RD}$	3	I	READ: A low on this pin when $\overline{CS}$ is low enables the 82C59A to release status onto the data bus for the CPU.
D_7-D_0	4-11	I/O	BIDIRECTIONAL DATA BUS: Control status and interrupt-vector information is transferred via this bus.
CAS 0 - CAS 2	12, 13, 15	I/O	CASCADE LINES: the CAS lines form a private 82C59A bus to control a multiple 82C59A structure. These pins are outputs for a master 82C59A and inputs for a slave 82C59A.
$\overline{SP}/\overline{EN}$	16	I/O	SLAVE PROGRAM/ENABLE BUFFER: This is a dual function pin. when in the Buffered Mode it can be used as an output to control buffer transceivers (EN). When not in the buffered mode it is used as an input to designate a master (SP = 1) or slave (SP = 0).
INT	17	0	INTERRUPT: This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU, thus it is connected to the CPU's interrupt pin.
IRO-IR7	18-25	I	INTERRUPT REQUESTS: Asynchronous inputs. An interrupt request is executed by raising an IR input (low to high), and holding it high until it is acknowledged (Edge Triggered Mode), or just by a high level on an IR input (Level Triggered Mode).
INTA	26	I	INTERRUPT ACKNOWLEDGE: This pin is used to enable 82C59A interrupt-vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
A0	27	I	ADDRESS LINE: This pin acts in conjunction with the $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ pins. It is used by the 82C59A to decipher various Command Words the CPU writes and status the CPU wishes to read. It is typically connected to CPU A0 address line (A for 80C86/88).

Functional Description

INTERRUPTS IN MICROCOMPUTER SYSTEMS

Microcomputer system design requires that I/O devices such as keyboards, displays, sensors and other components receive servicing in an efficient manner so that large amounts of the total system tasks can be assumed by the microcomputer with little or no effect on throughput.

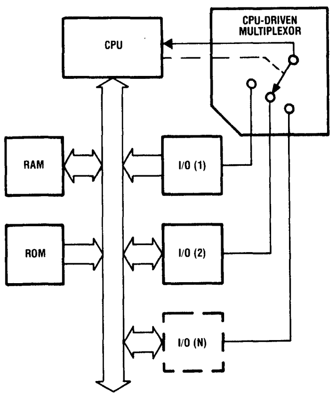
The most common method of servicing such devices is the Polled approach. This is where the processor must test each device in sequence and in effect "ask" each one if it needs servicing. It is easy to see that a large portion of the main program is looping through this continuous polling cycle and that such a method would have a serious, detrimental effect on system through-put, thus limiting the tasks that could be assumed by the microcomputer and reducing the cost effectiveness of using such devices.

A more desirable method would be one that would allow the microprocessor to be executing its main program and only stop to service peripheral devices when it is told to do so by the device itself. In effect, the method would provide an external asynchronous input that would inform the processor that it should complete whatever instruction that is currently being executed and fetch a new routine that will service the requesting device. Once this servicing is complete, however, the processor would resume exactly where it left off.

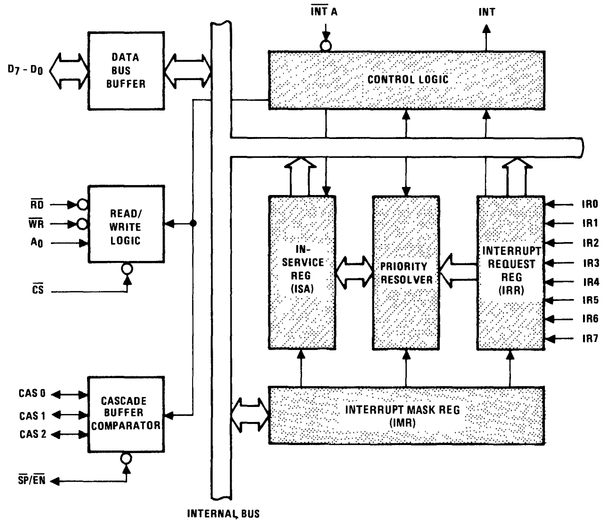
This is the interrupt-driven method. It is easy to see that system throughput would drastically increase, and thus more tasks could be assumed by the microcomputer to further enhance its cost effectiveness.

The Programmable Interrupt Controller (PIC) functions as an overall manager in an Interrupt-Driven system. It accepts requests from the peripheral equipment, determines which of the incoming requests is of the highest importance (priority), ascertains whether the incoming request has a higher priority value than the level currently being serviced, and issues an interrupt to the CPU based on this determination.

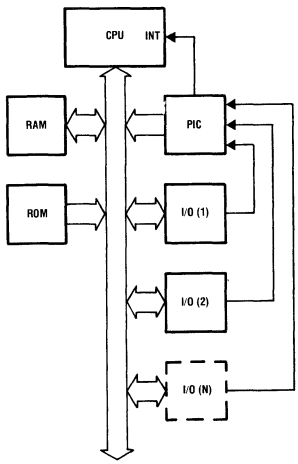
Each peripheral device or structure usually has a special program or "routine" that is associated with its specific functional or operational requirements; this is referred to as a "service routine". The PIC, after issuing an interrupt to the CPU, must somehow input information into the CPU that can "point" the Program Counter to the service routine associated with the requesting device. This "pointer" is an address in a vectoring table and will often be referred to, in this document, as vectoring data.



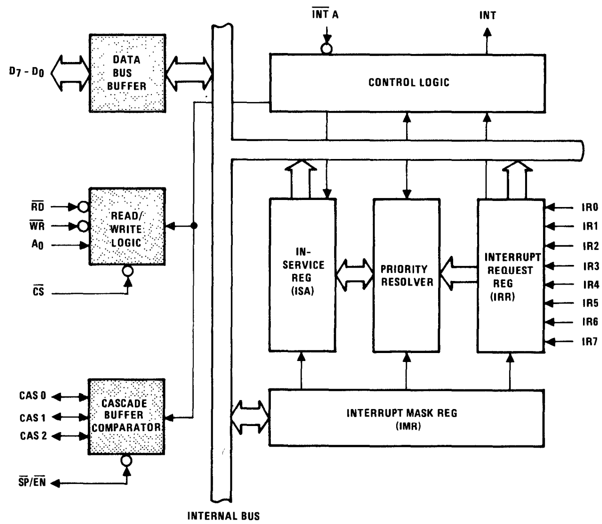
POLLED METHOD



82C59A INTERRUPT LOGIC



INTERRUPT METHOD



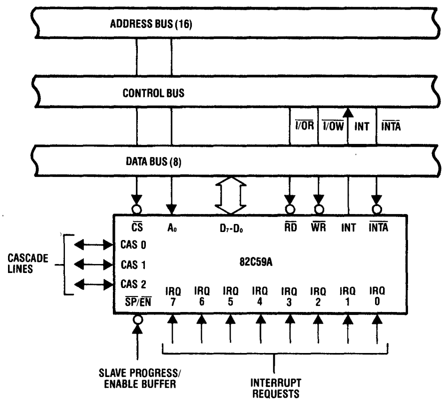
82C59A DATA AND CONTROL LOGIC

82C59A FUNCTIONAL DESCRIPTION

The 82C59A is a device specifically designed for use in real time, interrupt driven microcomputer systems. It manages eight levels of requests and has built-in features for expandability to other 82C59As (up to 64 levels). It is programmed by system software as an I/O peripheral. A selection of priority modes is available to the programmer so that the manner in which the requests are processed by the 82C59A can be configured to match system requirements. The priority modes can be changed or reconfigured dynamically at any time during main program operation. This means that the complete interrupt structure can be defined as required, based on the total system environment.

INTERRUPT REQUEST REGISTER (IRR) and IN-SERVICE REGISTER (ISR)

The interrupts at the IR input lines are handled by two registers in cascade, the Interrupt Request Register (IRR) and the In-Service Register (ISR). The IRR is used to store all the interrupt levels which are requesting service, and the ISR is used to store all the interrupt levels which are currently being serviced.



PRIORITY RESOLVER

This logic block determines the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during the INTA sequence.

INTERRUPT MASK REGISTER (IMR)

The IMR stores the bits which disable the interrupt lines to be masked. The IMR operates on the output of the IRR. Masking of a higher priority input will not affect the interrupt request lines of lower priority.

INTERRUPT (INT)

This output goes directly to the CPU interrupt input. The V_{OH} level on this line is designed to be fully compatible with the 8080A, 8085A, 8086 and 80C86 input levels.

INTERRUPT ACKNOWLEDGE ($\overline{INTA}$)

$\overline{INTA}$ pulses will cause the 82C59A to release vectoring information onto the data bus. The format of this data depends on the system mode (μPM) of the 82C59A.

DATA BUS BUFFER

This 3-state, bidirectional 8-bit buffer is used to interface the 82C59A to the system Data Bus. Control words and status information are transferred through the Data Bus Buffer.

READ/WRITE CONTROL LOGIC

The function of this block is to accept OUTput commands from the CPU. It contains the Initialization Command Word (ICW) registers and Operation Command Word (OCW) registers which store the various control formats for device operation. This function block also allows the status of the 82C59A to be transferred onto the Data Bus.

CHIP SELECT ($\overline{CS}$)

A LOW on this input enables the 82C59A. No reading or writing of the device will occur unless the device is selected.

WRITE ($\overline{WR}$)

A LOW on this input enables the CPU to write control words (ICWs and OCWs) to the 82C59A.

READ ($\overline{RD}$)

A LOW on this input enables the 82C59A to send the status of the Interrupt Request Register (IRR), In Service Register (ISR), the Interrupt Mask Register (IMR), or the interrupt level (in the poll mode) onto the Data Bus.

A_0

This input signal is used in conjunction with $\overline{WR}$ and $\overline{RD}$ signals to write commands into the various command registers, as well as reading the various status registers of the chip. This line can be tied directly to one of the address lines.

THE CASCADE BUFFER/COMPARATOR

This function block stores and compares the IDs of all 82C59As used in the system. The associated three I/O pins (CAS0-2) are outputs when the 82C59A is used as a master and are inputs when the 82C59A is used as a slave. As a master, the 82C59A sends the ID of the interrupting slave device onto the CAS0-2 lines. The slave thus selected will send its preprogrammed subroutine address onto the Data Bus during the next one or two consecutive INTA pulses. (See section "Cascading the 82C59A".)

INTERRUPT SEQUENCE

The powerful features of the 82C59A in a microcomputer system are its programmability and the interrupt routine addressing capability. The latter allows direct or indirect jumping to the specified interrupt routine requested without any polling of the interrupting devices. The normal sequence of events during an interrupt depends on the type of CPU being used.

These events occur in an 8080A/8085 system:

1. One or more of the INTERRUPT REQUEST lines (I0-I7) are raised high, setting the corresponding IRR bit(s).
2. The 82C59A evaluates these requests in the priority resolver and sends an interrupt (INT) to the CPU, if appropriate.
3. The CPU acknowledges the INT and responds with an $\overline{INTA}$ pulse.
4. Upon receiving an $\overline{INTA}$ from the CPU group, the highest priority ISR bit is set, and the corresponding IRR bit is reset. The 82C59A will also release a CALL instruction code (11001101) onto the 8-bit data bus through D_0-D_7.
5. This CALL instruction will initiate two additional $\overline{INTA}$ pulses to be sent to the 82C59A from the CPU group.
6. These two INTA pulses allow the 82C59A to release its preprogrammed subroutine address onto the data bus. The lower 8-bit address is released at the first INTA pulse and the higher 8-bit address is released at the second INTA pulse.
7. This completes the 3-byte CALL instruction released by the 82C59A. In the AEOI mode, the ISR bit is reset at the end of the third INTA pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt sequence.

The events occurring in an 80C86 system are the same until step 4.

4. Upon receiving an $\overline{INTA}$ from the CPU group, the highest priority ISR bit is set and the corresponding IRR bit is reset. The 82C59A does not drive the data bus during this cycle.
5. The 80C86 will initiate a second $\overline{INTA}$ pulse. During this pulse, the 82C59A releases an 8-bit pointer onto the data bus where it is read by the CPU.
6. This completes the interrupt cycle. In the AEOI mode, the ISR bit is reset at the end of the second $\overline{INTA}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.

If no interrupt request is present at step 4 of either sequence (i.e. the request was too short in duration), the 82C59A will issue an interrupt level 7. If a slave is programmed on IR bit 7, the CAS lines remain inactive and vector addresses are output from the master 82C59A.

Interrupt Sequence Outputs

8080, 8085

This sequence is timed by three $\overline{INTA}$ pulses. During the first $\overline{INTA}$ pulse, the CALL opcode is enabled onto the data bus.

First Interrupt Vector Byte Data: Hex CD

	D7	D6	D5	D4	D3	D2	D1	D0
CALL CODE	1	1	0	0	1	1	0	1

During the second $\overline{INTA}$ pulse, the lower address of the appropriate service routine is enabled onto the data bus. When interval = 4 bits, A_5-A_7 are programmed, while A_0-A_4 are automatically inserted by the 82C59A. When interval = 8, only A_6 and A_7 are programmed, while A_0-A_5 are automatically inserted.

Content of Second Interrupt Vector Byte

IR	Interval = 4							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	A5	1	1	1	0	0
6	A7	A6	A5	1	1	0	0	0
5	A7	A6	A5	1	0	1	0	0
4	A7	A6	A5	1	0	0	0	0
3	A7	A6	A5	0	1	1	0	0
2	A7	A6	A5	0	1	0	0	0
1	A7	A6	A5	0	0	1	0	0
0	A7	A6	A5	0	0	0	0	0

IR	Interval = 8							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	1	1	1	0	0	0
6	A7	A6	1	1	0	0	0	0
5	A7	A6	1	0	1	0	0	0
4	A7	A6	1	0	0	0	0	0
3	A7	A6	0	1	1	0	0	0
2	A7	A6	0	1	0	0	0	0
1	A7	A6	0	0	1	0	0	0
0	A7	A6	0	0	0	0	0	0

During the third $\overline{INTA}$ pulse, the higher address of the appropriate service routine, which was programmed as byte 2 of the initialization sequence (A_8-A_{15}), is enabled onto the bus.

Content of Third Interrupt Vector Byte

D7	D6	D5	D4	D3	D2	D1	D0
A15	A14	A13	A12	A11	A10	A9	A8

80C86, 80C88 INTERRUPT RESPONSE MODE

80C86 mode is similar to 8080/85 mode except that only two Interrupt Acknowledge cycles are issued by the processor and no CALL opcode is sent to the processor. The first interrupt acknowledge cycle is similar to that of 8080/85 systems in that the 82C59A uses it to internally freeze the state of the interrupts for priority resolution and, as a master, it issues the interrupt code on the cascade lines. On this first cycle, it does not issue any data to the processor and leaves its data bus buffers disabled. On the second interrupt acknowledge cycle in 80C86 mode, the master (or slave if so programmed) will send a byte of data to the processor with the acknowledged interrupt code composed as follows (note the state of the ADI mode control is ignored and A_5-A_{11} are unused in 80C86 mode.)

Content of Interrupt Vector Byte for 80C86 System Mode

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	T7	T6	T5	T4	T3	1	1	1
IR6	T7	T6	T5	T4	T3	1	1	0
IR5	T7	T6	T5	T4	T3	1	0	1
IR4	T7	T6	T5	T4	T3	1	0	0
IR3	T7	T6	T5	T4	T3	0	1	1
IR2	T7	T6	T5	T4	T3	0	1	0
IR1	T7	T6	T5	T4	T3	0	0	1
IR0	T7	T6	T5	T4	T3	0	0	0

PROGRAMMING THE 82C59A

The 82C59A accepts two types of command words generated by the CPU;

1. Initialization Command Words (ICWs): Before normal operation can begin, each 82C59A in the system must be brought to a starting point—by a sequence of 2 to 4 bytes timed by $\overline{WR}$ pulses.
2. Operation Command Words (OCWs): These are the command words which command the 82C59A to operate in various interrupt modes. Among these modes are:
   a. Fully nested mode
   b. Rotating priority mode
   c. Special mask mode
   d. Polled mode

The OCWs can be written into the 82C59A anytime after initialization.

Initialization Command Words (ICWS)

GENERAL

Whenever a command is issued with A0=0 and D4=1, this is interpreted as Initialization Command Word 1 (ICW1). ICW1 starts the initialization sequence during which the following automatically occur.

a. The edge sense circuit is reset, which means that following initialization, an interrupt request (IR) input must make a low-to-high transition to generate an interrupt.
b. The Interrupt Mask Register is cleared.
c. IR7 input is assigned priority 7.
d. Special Mask Mode is cleared and Status Read is set to IRR.
e. If IC4=0, then all functions selected in ICW4 are set to zero. (Non-Buffered mode*, no Auto-EOI, 8080/85 system).

*NOTE: Master/Slave in ICW4 is only used in the buffered mode.

INITIALIZATION COMMAND WORDS 1 and 2 (ICW1, ICW2)

A_5-A_{15}: Page starting address of service routines. In an 8080/85 system, the 8 request levels will generate CALLS to 8 locations equally spaced in memory. These can be programmed to be spaced at intervals of 4 or 8 memory locations, thus the 8 routines will occupy a page of 32 or 64 bytes, respectively.

The address format is 2 bytes long (A_0-A_{15}). When the routine interval is 4, A_0-A_4 are automatically inserted by the 82C59A, while A_5-A_{15} are programmed externally. When the routine interval is 8, A_0-A_5 are automatically inserted by the 82C59A while A_6-A_{15} are programmed externally.

The 8-byte interval will maintain compatibility with current software, while the 4-byte interval is best for a compact jump table.

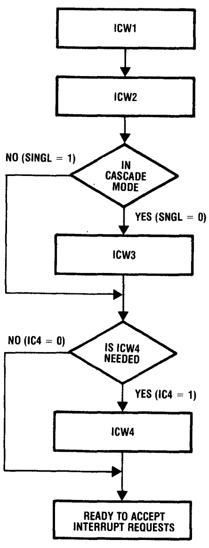
In an 80C86 system, A_{15}-A_{11} are inserted in the five most significant bits of the vectoring byte and the 82C59A sets the three least significant bits according to the interrupt level. A_{10}-A_5 are ignored and ADI (Address interval) has no effect.

LTIM: If LTIM = 1, then the 82C59A will operate in the level interrupt mode. Edge detect logic on the interrupt inputs will be disabled.

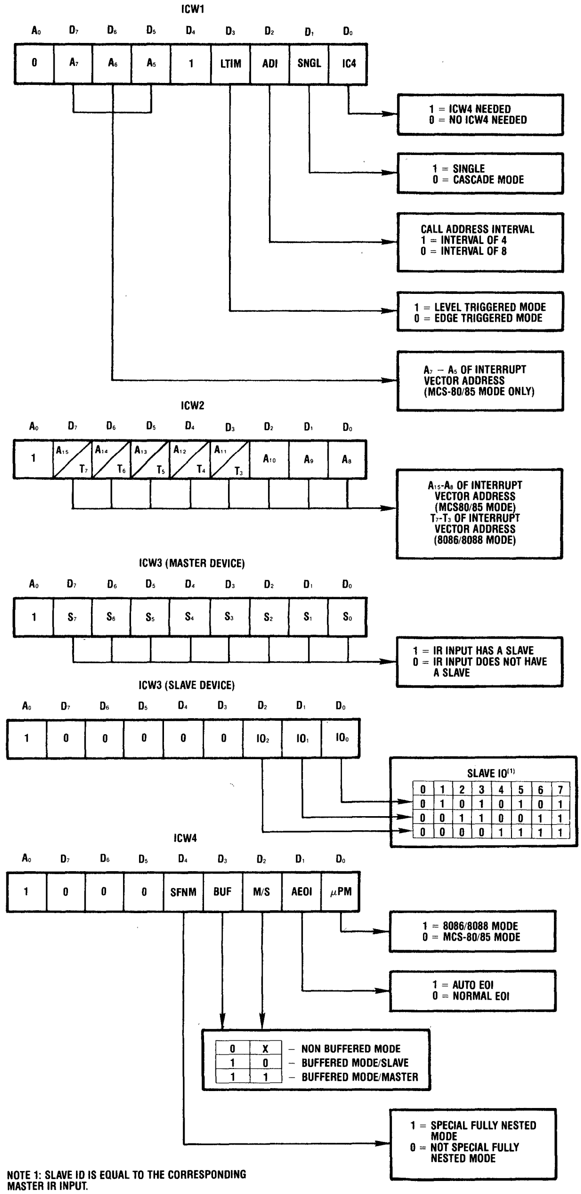
ADI: CALL address interval. ADI = 1 then interval = 4; ADI = 0 then interval = 8.

SNGL: Single. Means that this is the only 82C59A in the system. If SNGL=1, no ICW3 will be issued.

IC4: If this bit is set—ICW4 has to be issued. If ICW4 is not needed, set IC4 = 0.



82C59A INITIALIZATION SEQUENCE



82C59A INITIALIZATION COMMAND WORD FORMAT

INITIALIZATION COMMAND WORD 3 (ICW3)

This word is read only when there is more than one 82C59A in the system and cascading is used, in which case SNGL = 0. It will load the 8-bit slave register. The functions of this register are:

a. In the master mode (either when SP=1, or in buffered mode when M/S=1 in ICW4), a "1" is set for each slave in the bit corresponding to the appropriate IR line for the slave. The master then will release byte 1 of the call sequence (for 8080/85 system) and will enable the corresponding slave to release bytes 2 and 3 (for 80C86, only byte 2) through the cascade lines.

b. In the slave mode (either when SP=0, or if BUF=1 and M/S=0 in ICW4), bits 2-0 identify the slave. The slave compares its cascade input with these bits and if they are equal, bytes 2 and 3 of the call sequence (or just byte 2 for 80C86) are released by it on the Data Bus (Note: the slave address must correspond to the IR line it is connected to in the master ID).

INITIALIZATION COMMAND WORD 4 (ICW4)

SFNM: If SFNM = 1, the special fully nested mode is programmed.

BUF: If BUF = 1, the buffered mode is programmed. In buffered mode, $\overline{SP}/\overline{EN}$ becomes an enable output and the master/slave determination is by M/S.

M/S: If buffered mode is selected: M/S = 1 means the 82C59A is programmed to be a master, M/S = 0 means the 82C59A is programmed to be a slave. If BUF = 0, M/S has no function.

AEOI: If AEOI = 1, the automatic end of interrupt mode is programmed.

μPM: Microprocessor mode: μPM = 0 sets the 82C59A for 8080/85 system operation, μPM = 1 sets the 82C59A for 80C86 system operation.

OPERATION COMMAND WORDS (OCWs)

After the initialization Command Words (ICWs) are programmed into the 82C59A, the device is ready to accept interrupt requests at its input lines. However, during the 82C59A operation, a selection of algorithms can command the 82C59A to operate in various modes through the Operation Command Words (OCWs).

OPERATION CONTROL WORDS (OCWs)

	A0	D7	D6	D5	D4	D3	D2	D1	D0
OCW1	1	M7	M6	M5	M4	M3	M2	M1	M0
OCW2	0	R	SL	EOI	0	0	L2	L1	L0
OCW3	0	0	ESMM	SMM	0	1	P	RR	RIS

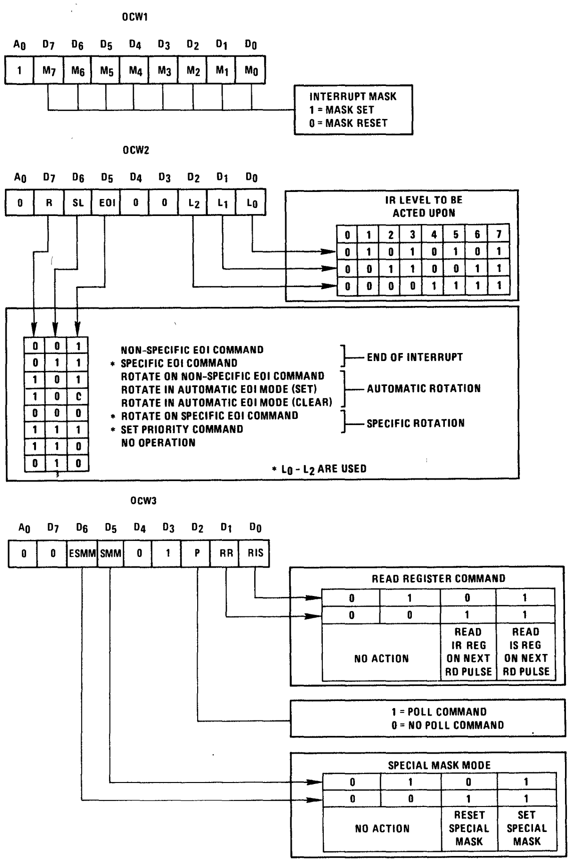
OPERATION CONTROL WORD 1 (OCW1)

OCW1 sets and clears the mask bits in the interrupt Mask Register (IMR). M_7-M_0 represent the eight mask bits. M=1 indicates the channel is masked (inhibited), M=0 indicates the channel is enabled.

OPERATION CONTROL WORD 2 (OCW2)

R, SL, EOI—These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations can be found on the Operation Command Word Format.

L_2, L_1, L_0—These bits determine the interrupt level acted upon when the SL bit is active.



82C59A OPERATION COMMAND WORD FORMAT

OPERATION CONTROL WORD 3 (OCW3)

ESMM – Enable Special Mask Mode. When this bit is set to 1 it enables the SMM bit to set or reset the Special Mask Mode. When ESMM=0,the SMM bit becomes a "don't care"

SMM – Special Mask Mode. If ESMM=1 and SMM=1,the 82C59A will enter Special Mask Mode. If ESMM=1 and SMM=0,the 82C59A will revert to normal mask mode. When ESMM=0, SMM has no effect.

FULLY NESTED MODE

This mode is entered after initialization unless another mode is programmed. The interrupt requests are ordered in priority from 0 through 7 (0 highest). When an interrupt is acknowledged the highest priority request is determined and its vector placed on the bus. Additionally, a bit of the Interrupt Service register (IS0-7) is set. This bit remains set until the microprocessor issues an End of Interrupt (EOI) command immediately before returning from the service routine, or if AEOI (Automatic End of Interrupt) bit is set, until the trailing edge of the last $\overline{INTA}$. While the IS bit is set, all further interrupts of the same or lower priority are inhibited, while higher levels will generate an interrupt (which will be acknowledged only if the microprocessor internal interrupt enable flip-flop has been re-enabled through software).

After the initialization sequence, IR0 has the highest priority and IR7 the lowest. Priorities can be changed, as will be explained, in the rotating priority mode or via the set priority command.

END OF INTERRUPT (EOI)

The In Service (IS) bit can be reset either automatically following the trailing edge of the last in sequence $\overline{INTA}$ pulse (when AEOI bit in ICW1 is set) or by a command word that must be issued to the 82C59A before returning from a service routine (EOI Command). An EOI command must be issued twice if in the Cascade mode, once for the master and once for the corresponding slave.

There are two forms of EOI command: Specific and Non-Specific. When the 82C59A is operated in modes which preserve the fully nested structure, it can determine which IS bit to reset on EOI. When a Non-Specific EOI command is issued the 82C59A will automatically reset the highest IS bit of those that are set, since in the fully nested mode the highest IS level was necessarily the last level acknowledged and serviced. A non-specific EOI can be issued with OCW2 (EOI=1, SL=0, R=0).

When a mode is used which may disturb the fully nested structure, the 82C59A may no longer be able to determine the last level acknowledged. In this case a Specific End of Interrupt must be issued which includes as part of the command the IS level to be reset. A specific EOI can be issued with OCW2 (EOI=1, SL=1, R=0, and L0-L2 is the binary level of the IS bit to be reset).

An IRR bit that is masked by an IMR bit will not be cleared by a non-specific EOI if the 82C59A is in the Special Mask Mode.

AUTOMATIC END OF INTERRUPT (AEOI) MODE

If AEOI=1 in ICW4, then the 82C59A will operate in AEOI mode continuously until reprogrammed by ICW4. In this mode the 82C59A will automatically perform a non-specific EOI operation at the trailing edge of the last interrupt acknowledge pulse (third pulse in 8080/85, second in 80C86). Note that from a system standpoint, this mode should be used only when a nested multi-level interrupt structure is not required within a single 82C59A.

AUTOMATIC ROTATION (Equal Priority Devices)

In some applications there are a number of interrupting devices of equal priority. In this mode a device, after being serviced, receives the lowest priority, so a device requesting an interrupt will have to wait, in the worst case until each of 7 other devices are serviced at most once. For example, if the priority and "in service" status is:

Before Rotate (IR4 the highest priority requiring service)

	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
"IS" STATUS	0	1	0	1	0	0	0	0
PRIORITY STATUS	7 (lowest)	6	5	4	3	2	1	0 (highest)

After Rotate (IR4 was serviced, all other priorities rotated correspondingly)

	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
"IS" STATUS	0	1	0	0	0	0	0	0
PRIORITY STATUS	2	1	0 (highest)	7 (lowest)	6	5	4	3

There are two ways to accomplish Automatic Rotation using OCW2, the Rotation on Non-Specific EOI Command (R=1, SL=0, EOI=1) and the Rotate in Automatic EOI Mode which is set by (R=1, SL=0, EOI=0) and cleared by (R=0, SL=0, EOI=0).

SPECIFIC ROTATION (Specific Priority)

The programmer can change priorities by programming the bottom priority and thus fixing all other priorities; i.e., if IR5 is programmed as the bottom priority device, then IR6 will have the highest one.

The Set Priority command is issued in OCW2 where: R=1, SL=1; L0-L2 is the binary priority level code of the bottom priority device.

Observe that in this mode internal status is updated by software control during OCW2. However, it is independent of the End of Interrupt (EOI) command (also executed by OCW2). Priority changes can be executed during an EOI command by using the Rotate on Specific EOI command in OCW2 (R=1, SL=1, EOI=1 and LO-12=IR level to receive bottom priority).

INTERRUPT MASKS

Each Interrupt Request input can be masked individually by the Interrupt Mask Register (IMR) programmed through OCW1. Each bit in the IMR masks one interrupt channel if it is set (1). Bit 0 masks IR0, Bit 1 masks IR1 and so forth. Masking an IR channel does not affect the other channels operation.

SPECIAL MASK MODE

Some applications may require an interrupt service routine to dynamically alter the system priority structure during its execution under software control. For example, the routine may wish to inhibit lower priority requests for a portion of its execution but enable some of them for another portion.

The difficulty here is that if an Interrupt Request is acknowledged and an End of Interrupt command did not reset its IS bit (i.e., while executing a service routine), the 82C59A would have inhibited all lower priority requests with no easy way for the routine to enable them.

That is where the Special Mask Mode comes in. In the special Mask Mode, when a mask bit is set in OCW1, it inhibits further interrupts at that level and enables interrupts from all other levels (lower as well as higher) that are not masked.

Thus, any interrupts may be selectively enabled by loading the mask register.

The special Mask Mode is set by OCW3 where: ESMM=1, SMM=1, and cleared where ESMM=1, SMM=0.

POLL COMMAND

In this mode, the INT output is not used or the microprocessor internal Interrupt Enable flip-flop is reset, disabling its interrupt input. Service to devices is achieved by software using a Poll command.

The Poll command is issued by setting P=1 in OCW3. The 82C59A treats the next $\overline{RD}$ pulse to the 82C59A (i.e. $\overline{RD}$=0, $\overline{CS}$=0) as an interrupt acknowledge, sets the appropriate IS bit if there is a request, and reads the priority level. Interrupt is frozen from $\overline{WR}$ to $\overline{RD}$.

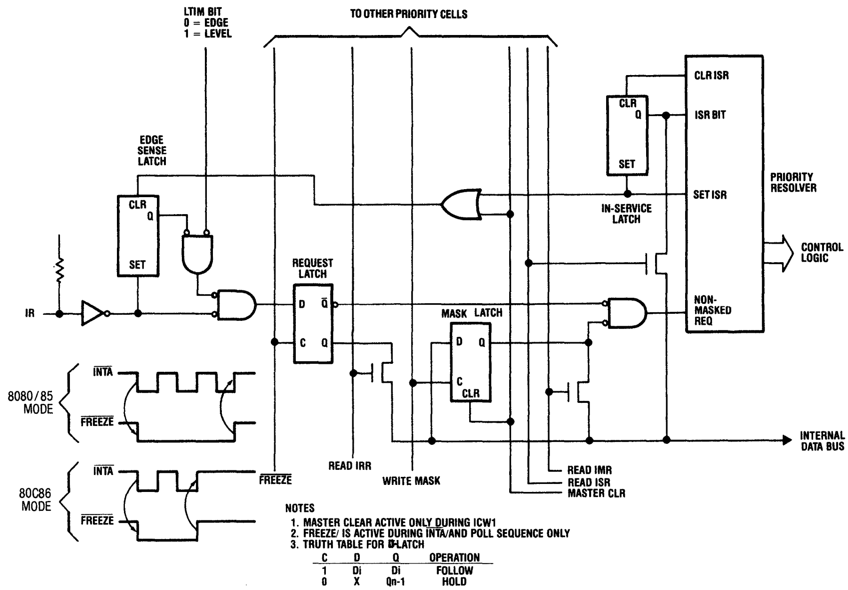
The word enabled onto the data bus during $\overline{RD}$ is:

D7	D6	D5	D4	D3	D2	D1	D0
I	—	—	—	—	W2	W1	W0

W0-W2: Binary code of the highest priority level requesting service.

I: Equal to a "1" if there is an interrupt.

This mode is useful if there is a routine command common to several levels so that the $\overline{INTA}$ sequence is not needed (saves ROM space). Another application is to use the poll mode to expand the number of priority levels to more than 64.



PRIORITY CELL—SIMPLIFIED LOGIC DIAGRAM

READING THE 82C59A STATUS

The input status of several internal registers can be read to update the user information on the system. The following registers can be read via OCW3 (IRR and ISR or OCW1 (IMR)).

In-Service Register (ISR): 8-bit register which contains the priority levels that are being serviced. The ISR is updated when an End of Interrupt Command is issued.

Interrupt Mask Register: 8-bit register which contains the interrupt request lines which are masked.

The IRR can be read when, prior to the $\overline{RD}$ pulse, a Read Register Command is issued with OCW3 (RR = 1, RIS = 0).

The ISR can be read when, prior to the $\overline{RD}$ pulse, a Read Register Command is issued with OCW3 (RR = 1, RIS = 1).

There is no need to write an OCW3 before every status read operation, as long as the status read corrersponds with the previous one; i.e., the 82C59A "remembers" whether the IRR or ISR has been previously selected by the OCW3. This is not true when poll is used. In the poll mode, the 82C59A treats the $\overline{RD}$ following a "poll write" operation as an INTA. After initialization, the 82C59A is set to IRR.

For reading the IMR, no OCW3 is needed. The output data bus will contain the IMR whenever $\overline{RD}$ is active and A0 = 1 (OCW1). Polling overrides status read when P = 1, RR = 1 in OCW3.

EDGE AND LEVEL TRIGGERED MODES

This mode is programmed using bit 3 in ICW1.

If LTIM = '0', an interrupt request will be recognized by a low to high transition on an IR input. The IR input can remain high without generating another interrupt.

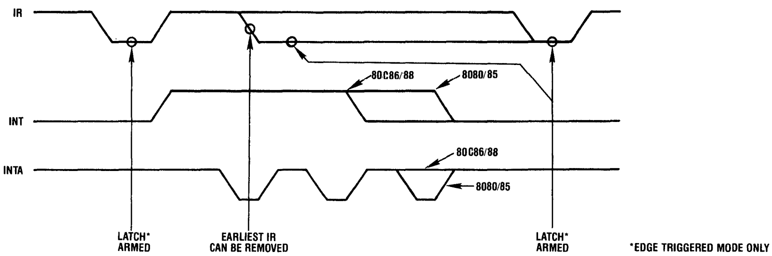
If LTIM = '1', an interrupt request will be recognized by a 'high' level on IR input, and there is no need for an edge detection. The interrupt request must be removed before the EOI command is issued or the CPU interrupt is enabled to prevent a second interrupt from occuring.

The priority cell diagram showns a conceptual circuit of the level sensitive and edge sensitive input circuitry of the 82C59A. Be sure to note that the request latch is a transparent D type latch.

In both the edge and level triggered modes the IR inputs must remain high until after the falling edge of the first INTA. If the IR input goes low before this time a DEFAULT IR7 will occur when the CPU acknowleges the interrupt. This can be a useful safeguard for detecting interrupts caused by spurious noise glitches on the IR inputs. To implement this feature the IR7 routine is used for "clean up" simply executing a return instruction, thus ignoring the interrupt. If IR7 is needed for other purposes a default IR7 can still be detected by reading the ISR. A normal IR7 interrupt will set the corresponding ISR bit, a default IR7 won't. If a default IR7 routine occurs during a normal IR7 routine, however, the ISR will remain set. In this case it is necessary to keep track of whether or not the IR7 routine was previously entered. If another IR7 occurs it is a default.

In power sensitive applications, it is advisable to place the 82C59A in the edge-triggered mode with the IR lines normally high. This will minimize the current through the pull-up resistors on the IR pins.

IR TRIGGERING TIMING REQUIREMENTS



THE SPECIAL FULLY NESTED MODE

This mode will be used in the case of a big system where cascading is used, and the priority has to be conserved within each slave. In this case the special fully nested mode will be programmed to the master (using ICW4). This mode is similar to the normal nested mode with the following exceptions:

a. When an interrupt request from a certain slave is in service, this slave is not locked out from the master's priority logic and further interrupt requests from higher priority IRs within the slave will be recognized by the master and will initiate interrupts to the processor. (In the normal nested mode a slave is masked out when its request is in service and no higher requests from the same slave can be serviced.)

b. When exiting the Interrupt Service routine the software has to check whether the interrupt serviced was the only one from that slave. This is done by sending a non-specific End of Interrupt (EOI) command to the slave and then reading its In-Service register and checking for zero. If it is empty, a non-specified EOI can be sent to the master, too. If not, no EOI should be sent.

BUFFERED MODE

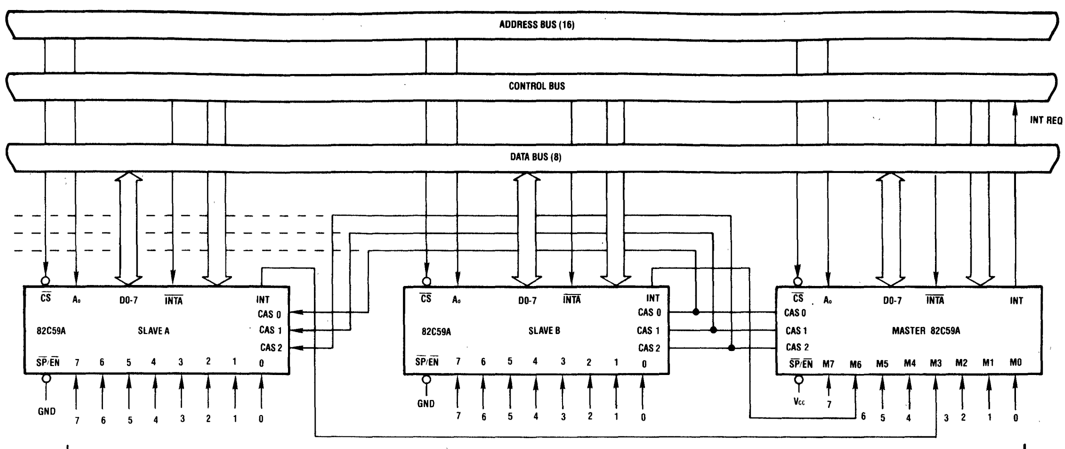
When the 82C59A is used in a large system where bus driving buffers are required on the data bus and the cascading mode is used, there exists the problem of enabling buffers.

The buffered mode will structure the 82C59A to send an enable signal of SP/EN to enable the buffers. In this mode, whenever the 82C59A's data bus outputs are enabled, the SP/EN output becomes active.

This modification forces the use of software programming to determine whether the 82C59A is a master or a slave. Bit 3 in ICW4 programs the buffered mode, and bit 2 in ICW4 determines whether it is a master or a slave.

CASCADE MODE

The 82C59A can be easily interconnected in a system of one master with up to eight slaves to handle up to 64 priority levels.



CASCADING THE 82C59A

The master controls the slaves through the 3 line cascade bus. The cascade bus acts like chip selects to the slaves during the $\overline{INTA}$ sequence.

In a cascade configuration, the slave interrupt outputs are connected to the master interrupt request inputs. When a slave request line is activated and afterwards acknowledged, the master will enable the corresponding slave to release the device routine address during bytes 2 and 3 of INTA. (Byte 2 only for 80C86/80C88).

The cascade bus lines are normally low and will contain the slave address code from the trailing edge of the first INTA pulse to the trailing edge of the third pulse. Each 82C59A in the system must follow a separate initialization sequence and can be programmed to work in a different mode. An EOI command must be issued twice: once for the master and once for the corresponding slave. Chip select decoding is required to activate each 82C59A.

Note: Auto EOI is supported in the slave mode for the 82C59A.

The cascade lines of the Master 82C59A are activated only for slave inputs, non-slave inputs leave the cascade line inactive (low). Therefore, it is necessary to use a slave address of 0 (zero) only after all other addresses are used.

Absolute Maximum Ratings

Supply Voltage .... +8.0 Volts
Input, Output or I/O Voltage Applied .... GND -0.5V to VCC +0.5V
Storage Temperature Range .... -65°C to +150°C
Maximum Package Power Dissipation .... 1 Watt
θ_{jc} .... 20°C/W (CERDIP package), 25°C/W (LCC package)
θ_{ja} .... 58°C/W (CERDIP package), 63°C/W (LCC package)
Gate Count .... 1250 Gates
Junction Temperature .... +150°C
Lead Temperature (Soldering, Ten Seconds) .... +260°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +4.5V to +5.5V
Operating Temperature Range
C82C59A .... 0°C to +70°C
I82C59A .... -40°C to +85°C
M82C59A .... -55°C to +125°C

D.C. Electrical Specifications

VCC = 5.0V ± 10%,
T_A = 0°C to +70°C (C82C59A);
T_A = -40°C to +85oC (I82C59A);
T_A = -55°C to +125°C (M82C59A)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	Logical One Input Voltage	2.0 2.2		V V	I82C59A C82C59A M82C59A
VIL	Logical Zero Input Voltage		0.8	V	
VOH	Output High Voltage	3.0 VCC - 0.4		V V	IOH = -2.5mA IOH = -100μA
VOL	Output Low Voltage		0.4	V	VOL = +2.5mA
II	Input Leakage Current	-1.0	+1.0	μA	VIN = GND or VCC DIP Pins: 1-3, 26-27
IO	I/O Leakage Current	-10.0	+10.0	μA	VO = GND or VCC DIP Pins 4-13,15-16
ILIR	IR Input Load Current		-300 -500 10	μA μA μA	VIN = 0, C82C59A VIN = 0, I82C59A, M82C59A VIN = VCC: All temperature ranges
ICCSB	Standby Power Supply Current		10	μA	VCC = 5.5V VIN = VCC or GND (Note 1) Outputs Open
ICCOP	Operating Power Supply Current		1	mA/MHz	TA = +25°C, VCC = 5V, Typical (Note 2)

1. Except for IR0-IR7 where VIN = VCC or open.
2. ICCOP = 1mA/MHz of peripheral read/write cycle time, (ex.: 1.0μs I/O read/write cycle time = 1mA.)

Capacitance

T_A = 25°C; VCC = GND = 0V; VIN = +5V or GND

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_{IN}	Input Capacitance	5	pF	FREQ = 1MHz Unmeasured pins returned to GND
C_{OUT}	Output Capacitance	15	pF	
C_{IO}	I/O Capacitance	20	pF	

A.C. Electrical Specifications

V_{CC} = +5V±10%, GND = 0V: T_A = 0°C to +70°C (C82C59A) (C82C59A-5)
: T_A = −40°C to +85°C (I82C59A) (I82C59A-5)
: T_A = −55°C to +125°C (M82C59A) (M82C59A-5)

Timing Requirements

SYMBOL	PARAMETER	82C59A-5 MIN	82C59A-5 MAX	82C59A MIN	82C59A MAX	UNITS	TEST CONDITIONS
TAHRL	AO/$\overline{CS}$ Setup to $\overline{RD}$/$\overline{INTA}$	10		10		ns	
TRHAX	AO/$\overline{CS}$ Hold after $\overline{RD}$/$\overline{INTA}$	5		5		ns	
TRLRH	$\overline{RD}$/$\overline{INTA}$ Pulse Width	235		160		ns	
TAHWL	AO/$\overline{CS}$ Setup to $\overline{WR}$	0		0		ns	
TWHAX	AO/$\overline{CS}$ Hold after $\overline{WR}$	5		5		ns	
TWLWH	$\overline{WR}$ Pulse Width	165		95		ns	
TDVWH	Data Setup to $\overline{WR}$	240		160		ns	
TWHDX	Data Hold after $\overline{WR}$	5		5		ns	
TJLJH	Interrupt Request Width (Low)	100		100		ns	See Note 1
TCVIAL	Cascade Setup to Second or Third $\overline{INTA}$ (Slave Only)	55		40		ns	
TRHRL	End of $\overline{RD}$ to next $\overline{RD}$; End of $\overline{INTA}$ to next $\overline{INTA}$ within an $\overline{INTA}$ sequence only	160		160		ns	
TWHWL	End of $\overline{WR}$ to next $\overline{WR}$	190		190		ns	
*TCHCL	End of Command to next Command (Not same command type) End of $\overline{INTA}$ sequence to next $\overline{INTA}$ sequence	500		400		ns	

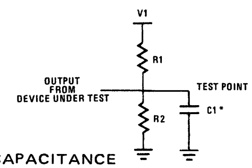
**Worst case timing for TCHCL in an actual microprocessor system is typically much greater than 400 ns (i.e. 8085A = 1.6μs, 8085A-2 = 1μs, 80C86 = 1μs).*

Note 1: This is the low time required to clear the input latch in the edge triggered mode.

Timing Responses

SYMBOL	PARAMETER	82C59A-5 MIN	82C59A-5 MAX	82C59A MIN	82C59A MAX	UNITS	TEST CONDITIONS
TRLDV	Data Valid from $\overline{RD}$/$\overline{INTA}$		160		120	ns	1
TRHDZ	Data Float after $\overline{RD}$/$\overline{INTA}$	10	100	10	85	ns	2
TJHIH	Interrupt Output Delay		350		300	ns	1
TIALCV	Cascade Valid from First $\overline{INTA}$ (Master Only)		565		360	ns	1
TRLEL	Enable Active from $\overline{RD}$ or $\overline{INTA}$		125		100	ns	1
TRHEH	Enable inactive from $\overline{RD}$ or $\overline{INTA}$		60		50	ns	1
TAHDV	Data Valid from Stable Address		210		200	ns	1
TCVDV	Cascade Valid to Valid Data		300		200	ns	1

A.C. Test Circuit

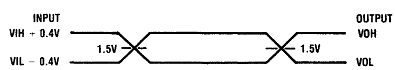


*INCLUDES STRAY AND JIG CAPACITANCE

TEST CONDITION	V1	R1	R2	C1
1	1.7V	523Ω	OPEN	100 pf
2	4.5V	1.8KΩ	1.8KΩ	30 pf

TEST CONDITION DEFINITION TABLE

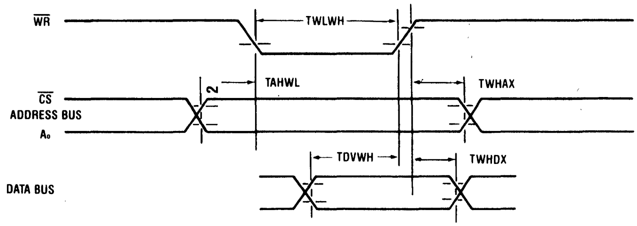
A.C. Testing Input, Output Waveforms



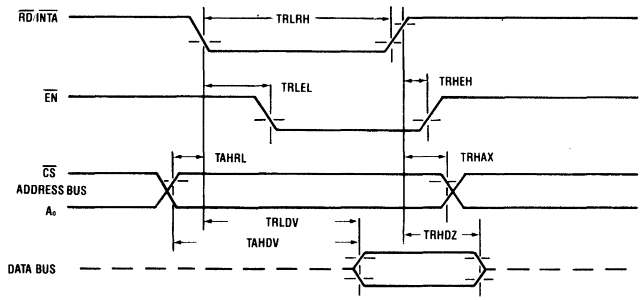
A.C. Testing: All input signals must switch between VIL - 0.4V and VIH + 0.4V. Input rise and fall times are driven at 1ns/V.

Waveforms

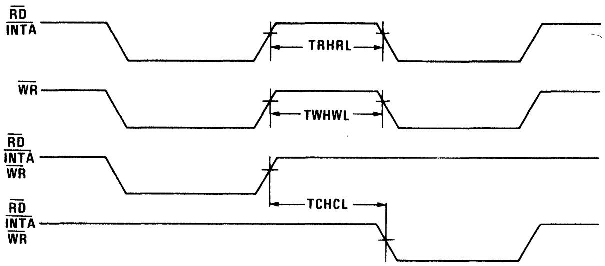
WRITE



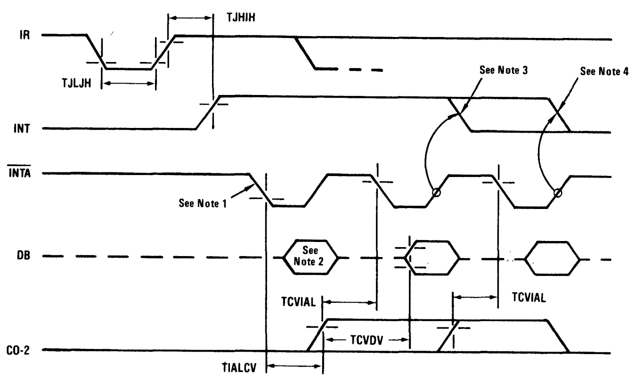
READ/INTA



OTHER TIMING



INTA SEQUENCE



Note 1: Interrupt Request (IR) must remain HIGH until leading edge of first $\overline{INTA}$.
Note 2: During first $\overline{INTA}$ the Data Bus is not active in 80C86/88 mode.
Note 3: 80C86/88 mode.
Note 4: 8080/8085 mode.

HARRIS

82C82

CMOS Octal Latching Bus Driver

Features

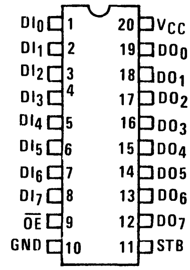
- Full Eight-Bit Parallel Latching Buffer
- Bipolar 8282 Compatible
- Three-State Non-Inverting Outputs
- Propagation Delay .... 35ns Max.
- A.C. Specifications Guaranteed for:
  - Full Temperature Range
  - 10% Power Supply Tolerance
  - CL = 300pF
- Gated Inputs
  - Reduce Operating Power
  - Eliminate the Need for Pull-Up Resistors
- Single 5V Power Supply
- Power Supply Current .... 10μA Max. Standby
- Outputs Guaranteed Valid at VCC = 2.0 Volts
- Wide Operating Temperature Ranges:
  - C82C82 .... 0°C to +70°C
  - I82C82 .... -40°C to +85°C
  - M82C82 .... -55°C to +125°C

Description

The Harris 82C82 is an octal latching buffer manufactured using a self-aligned silicon gate CMOS process. This circuit provides an eight-bit parallel latch/buffer in a 20-pin package. The active high strobe (STB) input allows transparent transfer of data and latches data on the negative transition of this signal. The active low output enable $\overline{OE}$ permits simple interface to state-of-the-art microprocessor systems.

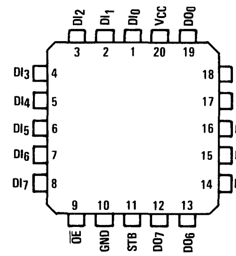
Pinouts

TOP VIEW

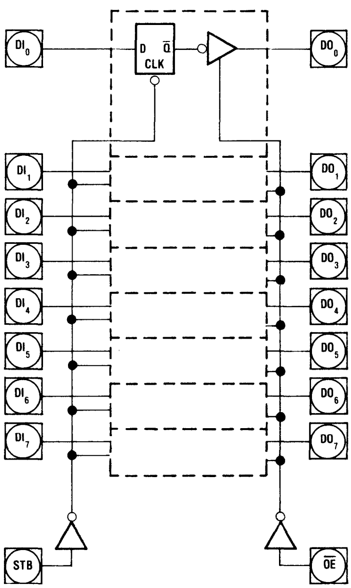


LCC/PLCC

TOP VIEW



Functional Diagram



PIN NAMES

DI_0 - DI7	Data Input Pins
DO_0 - DO7	Data Output Pins
STB	Active High Strobe
$\overline{OE}$	Active Low Output Enable

Truth Table

STB	$\overline{OE}$	DI	DO
X	H	X	Hi-Z
H	L	L	L
H	L	H	H
↓	L	X	*

H = Logic One
L = Logic Zero
X = Don't Care
Hi-Z = High Impedance
↓ = Negative Transition
* = Latched to Value of Last Data

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow standard IC Handling Procedures.

Absolute Maximum Ratings

Supply Voltage .... +8.0 Volts
Input, Output or I/O Voltage Applied .... GND -0.5V to V_{CC} +0.5V
Storage Temperature Range .... -65°C to +150°C
Maximum Package Power Dissipation .... 1 Watt
θ_{jc} .... 26°C/W (CERDIP Package), 31°C/W (LCC Package)
θ_{ja} .... 76°C/W (CERDIP Package), 81°C/W (LCC Package)
Gate Count .... 65 Gates
Junction Temperature .... +150°C
Lead Temperature (Soldering, Ten Seconds) .... +260°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +4.5V to +5.5V
Operating Temperature Range
C82C82 .... 0°C to +70°C
I82C82 .... -40°C to +85°C
M82C82 .... -55°C to +125°C

D.C. Electrical Specifications

VCC = 5.0V ± 10%; T_A = 0°C to +70°C (C82C82); T_A = -40°C to +85°C (I82C82); T_A = -55°C to +125°C (M82C82)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical One Input Voltage	2.0 2.2		V V	C82C82, I82C82 M82C82 (Note 1)
V_{IL}	Logical Zero Input Voltage		0.8	V	
V_{OH}	Logical Zero Output Voltage	2.9 VCC -0.4V		V	IOH = -8mA IOH = -100μA $\overline{OE}$ = LOW
V_{OL}	Logical Zero Output Voltage		0.4	V	IOL = 8mA $\overline{OE}$ = LOW
II	Input Leakage Current	-1.0	1.0	μA	VIN = GND or VCC DIP Pins 1-9, 11
I_O	Output Leakage Current	-10.0	10.0	μA	VO = GND OR VCC $\overline{OE}$ = VCC -0.5V DIP Pins 12-19
I_{CCSB}	Standby Power Supply Current		10	μA	VIN = VCC or GND VCC = 5.5V Outputs Open
I_{CCOP}	Operating Power Supply Current		1	mA/MHz	T_A = +25°C, VCC = 5V, Typical (See Note 2)

NOTES: 1. V_{IH} is measured by applying a pulse of magnitude = V_{IHmin} to one data input at a time and checking the corresponding device output for a valid logical "1" during valid input high time. Control pins (STB, $\overline{OE}$) are tested separately with all device data input pins at V_{CC} -0.5V.
2. Typical I_{CCOP} = 1mA/MHz of STB cycle time. (Example: 5MHz μP, ALE = 1.25MHz, I_{CCOP} = 1.25mA).

Capacitance

T_A = 25°C; VCC = GND = 0V; VIN = +5V or GND

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_{IN}	Input Capacitance	5	pF	FREQ = 1MHz Unmeasured pins returned to GND
C_{OUT}	Output Capacitance	15	pF	

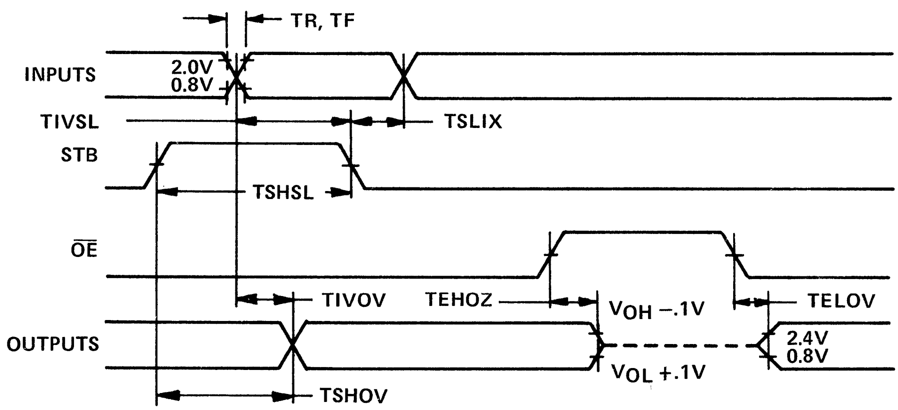
A.C. Electrical Specifications

V_{CC} = 5.0V ± 10%; C_L = 300pF*, FREQ = 1MHz
T_A = 0°C to +70°C (C82C82);
T_A = -40°C to +85°C (I82C82);
T_A = -55°C to +125°C (M82C82)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
TIVOV	Propagation Delay Input to Output		35	ns	see notes 1, 2
TSHOV	Propagation Delay STB to Output		55	ns	see notes 1, 2
TEHOZ	Output Disable Time		35	ns	see notes 1, 2
TELOV	Output Enable Time		50	ns	see notes 1, 2
TIVSL	Input to STB Set Up Time	0		ns	see notes 1, 2
TSLIX	Input to STB Hold Time	25		ns	see notes 1, 2
TSHSL	STB High Time	25		ns	see notes 1, 2
TR, TF	Input Rise/Fall Times		20	ns	see notes 1, 2

* Output load capacitance is rated at 300pF for ceramic and plastic packages.

NOTES:
1. All A.C. parameters tested as per test circuits and definitions in Figures 1 - 4. Input rise and fall times are driven at 1ns/V.
2. Input test signals must switch between VIL - 0.4V and VIH + 0.4V.



All timing measurements are made at 1.5V unless otherwise noted.

FIGURE 1. 82C82 TIMING RELATIONSHIPS

A.C. Test Circuit

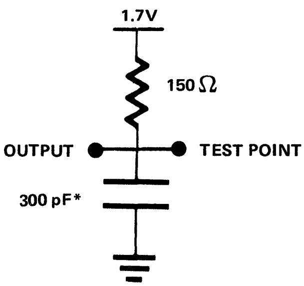


FIGURE 2.
TIVOV, TSHOV, TELOV
LOAD CIRCUIT

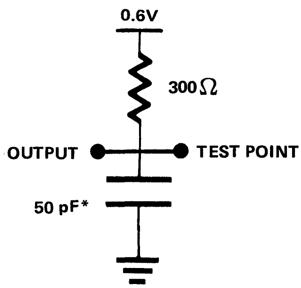


FIGURE 3.
TEHOZ
OUTPUT HIGH DISABLE
LOAD CIRCUIT

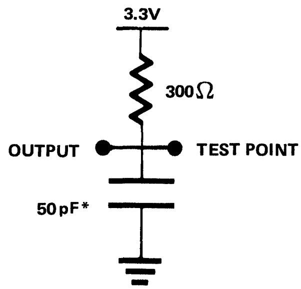


FIGURE 4.
TEHOZ
OUTPUT LOW DISABLE
LOAD CIRCUIT

*Includes stray and jig capacitance

Decoupling Capacitors

The transient current required to charge and discharge the 300pF load capacitance specified in the 82C82 data sheet is determined by

$$I = C_L \, (dv/dt)$$

Assuming that all outputs change state at the same time and that dv/dt is constant;

$$I = C_L \frac{(VCC \times 80\%)}{t_R/t_F}$$

where t_R = 20 ns, VCC = 5.0 volts, C_L = 300pF on each of eight outputs.

$$I = (8 \times 300 \times 10^{-12}) \times (5.0v \times 0.8)/(20 \times 10^{-9})$$

$$= 480 \text{ mA}$$

This current spike may cause a large negative voltage spike on VCC, which could cause improper operation of the device. To filter out this noise, it is recommended that a 0.1 μF ceramic disc decoupling capacitor be placed between VCC and GND at each device, with placement being as near to the device as possible.

GATED INPUTS

During normal system operation of a latch, signals on the bus at the device inputs will become high impedance or make transitions unrelated to the operation of the latch. These unrelated input transitions switch the input circuitry and typically cause an increase in power dissipation in CMOS devices by creating a low resistance path between V_{CC} and GND when the signal is at or near the input switching threshold. Additionally, if the driving signal becomes high impedance ("float" condition), it could create an indeterminate logic state at the inputs and cause a disruption in device operation.

The Harris 82C8X series of bus drivers eliminates these conditions by turning off data inputs when data is latched (STB = logic zero for the 82C82/83H) and when the device is disabled ($\overline{OE}$ = logic one for 82C86H/87H). These gated inputs disconnect the input circuitry from the V_{CC} and ground power supply pins by turning off the upper P-channel and lower N-channel (see Figure 5a, 5b). No current flow from V_{CC} to GND occurs during input transitions and invalid logic states from floating inputs are not transmitted. The next stage is held to a valid logic level internal to the device.

D.C. input voltage levels can also cause an increase in I_{CC} if these input levels approach the minimum V_{IH} or maximum V_{IL} conditions. This is due to the operation of the input circuitry in its linear operating region (partially conducting state). The 82C8X series gated inputs mean that this condition will occur only during the time the device is in the transparent mode (STB = logic one). I_{CC} remains below the maximum I_{CC} standby specification of 10 μA during the time inputs are disabled, thereby greatly reducing the average power dissipation of the 82C8X series devices.

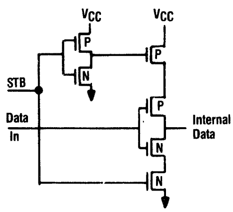


FIGURE 5a.
82C82/83H

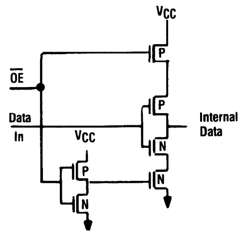


FIGURE 5b.
82C86H/87H GATED INPUTS

TYPICAL 82C82 SYSTEM EXAMPLE

In a typical 80C86/88 system, the 82C82 is used to latch multiplexed addresses and the STB input is driven by ALE (Address Latch Enable) (see Figure 6). The high pulse width of ALE is approximately 100ns with a bus cycle time of 800ns (80C86/88 @ 5MHz). The 82C82 inputs are active only 12.5% of the bus cycle time. Average power dissipation related to input transitioning is reduced by this factor also.

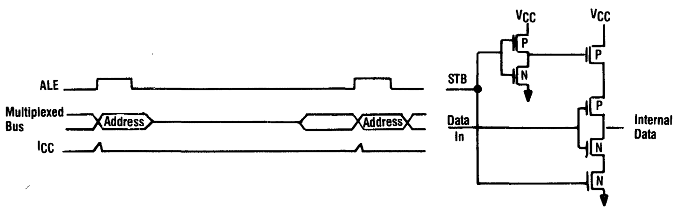


FIGURE 6.
SYSTEM EFFECTS OF GATED INPUTS

82C83H

CMOS Octal Latching Inverting Bus Driver

Features

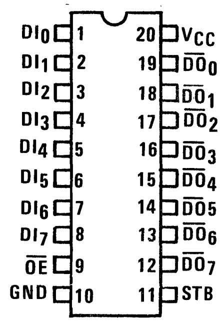
- Full Eight-Bit Parallel Latching Buffer
- Bipolar 8283 Compatible
- Three-State Inverting Outputs
- Propagation Delay .... 25ns Max.
- A. C. Specifications Guaranteed for:
  - Full Temperature Range
  - 10% Power Supply Tolerance
  - CL = 300pF
- Gated Inputs
  - Reduce Operating Power
  - Eliminate the Need for Pull-Up Resistors
- Single 5V Power Supply
- Power Supply Current .... 10μA Max. Standby
- Outputs Guaranteed Valid at VCC = 2.0 Volts
- Wide Operating Temperature Ranges:
  - C82C83H .... 0°C to +70°C
  - I82C83H .... -40°C to +85°C
  - M82C83H .... -55°C to +125°C

Description

The Harris 82C83H is an octal latching buffer manufactured using a self-aligned silicon gate CMOS process. This circuit provides an eight-bit parallel latch/buffer in a 20-pin package. The active high strobe (STB) input allows transparent transfer of data and latches data on the negative transition of this signal. The active low output enable (OE) permits simple interface to state-of-the-art microprocessor systems. The 82C83H provides inverted data at the outputs.

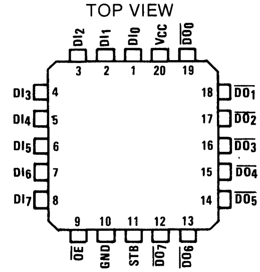
Pinouts

TOP VIEW

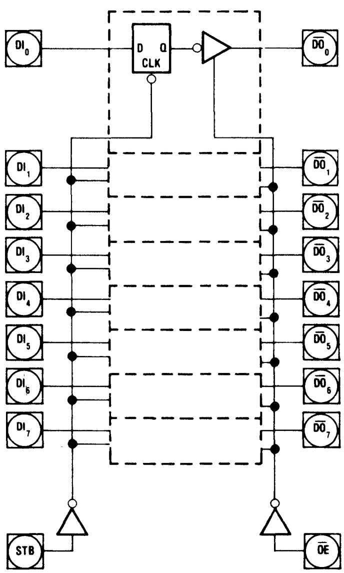


LCC/PLCC

TOP VIEW



Functional Diagram



PIN NAMES

DI0 - DI7 Data Input Pins
DO0 - DO7 Data Output Pins
STB Active High Strobe
OE Active Low Output Enable

Truth Table

STB	OE	DI	DO
X	H	X	Hi-Z
H	L	L	H
H	L	H	L
↓	L	X	*

H = Logic One
L = Logic Zero
X = Don't Care
Hi-Z = High Impedance
↓ = Negative Transition
* = Latched to Value of Last Data

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow standard IC Handling Procedures.

Absolute Maximum Ratings

Supply Voltage ... +8.0 Volts
Input, Output or I/O Voltage Applied ... GND -0.5V to V_{CC} +0.5V
Storage Temperature Range ... -65°C to +150°C
Maximum Package Power Dissipation ... 1 Watt
θ_{jc} ... 18°C/W (CERDIP Package), 23°C/W (LCC Package)
θ_{ja} ... 73°C/W (CERDIP Package), 78°C/W (LCC Package)
Gate Count ... 265 Gates
Junction Temperature ... +150°C
Lead Temperature (Soldering, Ten Seconds) ... +260°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range ... +4.5V to +5.5V
Operating Temperature Range
C82C83H ... 0°C to +70°C
I82C83H ... -40°C to +85°C
M82C83H ... -55°C to +125°C

D.C. Electrical Specifications

VCC = 5.0V ± 10%; T_A = 0°C to +70°C (C82C83H);
T_A = -40°C to +85°C (I82C83H);
T_A = -55°C to +125°C (M82C83H)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical One Input Voltage	2.0 2.2		V V	C82C83H, I82C83H M82C83H
V_{IL}	Logical Zero Input Voltage		0.8	V	
V_{OH}	Logical Zero Output Voltage	3.0 VCC -0.4V		V	IOH = -8mA IOH = -100μA $\overline{OE}$ = LOW
V_{OL}	Logical Zero Output Voltage		0.45	V	IOL = 20mA $\overline{OE}$ = LOW
II	Input Leakage Current	-10	10	μA	VIN = GND or VCC DIP Pins 1-9, 11
I_O	Output Leakage Current	-10	10	μA	VO = GND or VCC $\overline{OE}$ ≥ VCC -0.5V DIP Pins 12-19
I_{CCSB}	Standby Power Supply Current		10	μA	VIN = VCC or GND VCC = 5.5V Outputs Open
I_{CCOP}	Operating Power Supply Current		1	mA/MHz	T_A = +25°C, VCC = 5V, Typical (See Note 2)

NOTES: 1. V_{IH} is measured by applying a pulse of magnitude = V_{IHmin} to one data input at a time and checking the corresponding device output for a valid logical "1" during valid input high time. Control pins (STB, $\overline{OE}$) are tested separately with all device data input pins at V_{CC} -0.5V.
2. Typical I_{CCOP} = 1mA/MHz of STB cycle time. (Example: 5MHz μP, ALE = 1.25MHz, I_{CCOP} = 1.25mA).

Capacitance

T_A = 25°C; VCC = GND = 0V; VIN = +5V or GND

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_{IN}	Input Capacitance	12	pF	FREQ = 1MHz Unmeasured pins returned to GND
C_{OUT}	Output Capacitance	17	pF	

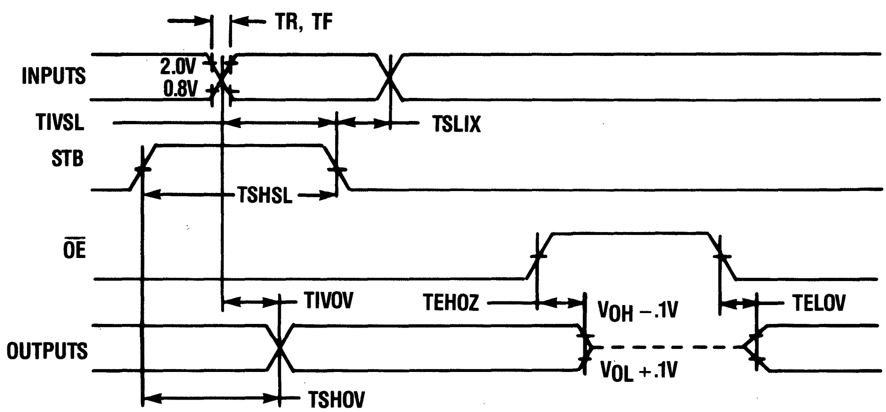
Electrical Specifications

V_{CC} = 5.0V ± 10%; C_L = 300pF*, FREQ = 1MHz
T_A = 0°C to +70°C (C82C83H); T_A = -40°C to +85°C (I82C83H); T_A = -55°C to +125°C (M82C83H)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
TIVOV	Propagation Delay Input to Output	5	25	ns	see notes 1, 2
TSHOV	Propagation Delay STB to Output	10	50	ns	see notes 1, 2
TEHOZ	Output Disable Time	5	22	ns	see notes 1, 2
TELOV	Output Enable Time	10	45	ns	see notes 1, 2
TIVSL	Input to STB Set Up Time	0		ns	see notes 1, 2
TSLIX	Input to STB Hold Time	30		ns	see notes 1, 2
TSHSL	STB High Time	15		ns	see notes 1, 2
TR, TF	Input Rise/Fall Times		20	ns	see notes 1, 2

*Output load capacitance is rated at 300 pF for both ceramic and plastic packages.

NOTES: 1. All A.C. Parameters tested as per test circuits and definitions in Figures 1-5. Input rise and fall times are driven at 1 ns/V.
2. Input test signals must switch between V_{IL} −0.4V and V_{IH} +0.4V.



All timing measurements are made at 1.5V unless otherwise noted.

Figure 1
82C83H Timing Relationships

A.C. Test Circuit

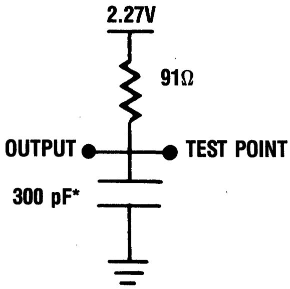


Figure 2
Switching
Load Circuit

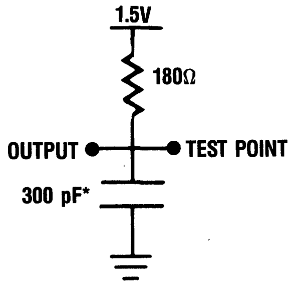


Figure 3
TELOV
Output High Enable
Load Circuit

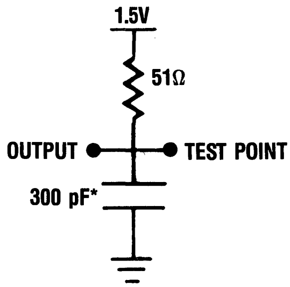


Figure 4
TELOV
Output Low Enable
Load Circuit

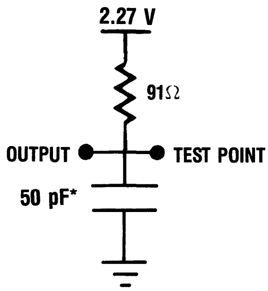


Figure 5
TEHOZ
Output Low/High Disable
Load Circuit

*Includes jig and stray capacitance

Decoupling Capacitors

The transient current required to charge and discharge the 300 pF load capacitance specified in the 82C83H data sheet is determined by

$$I = C_L(dv/dt)$$

Assuming that all outputs change state at the same time and that dv/dt is constant;

$$I = C_L \frac{(V_{CC} \times 80\%)}{t_R/t_F}$$

where t_R = 20 ns, V_{CC} = 5.0 volts, C_L = 300 pF on each of eight outputs.

$$I = (8 \times 300 \times 10^{-12}) \times (5.0V \times 0.8)/(20 \times 10^{-9})$$

$$= 480 \text{ mA}$$

This current spike may cause a large negative voltage spike on V_{CC}, which could cause improper operation of the device. To filter out this noise, it is recommended that a 0.1 μF ceramic disc capacitor be placed between V_{CC} and GND at each device, with placement being as near to the device as possible.

GATED INPUTS

During normal system operation of a latch, signals on the bus at the device inputs will become high impedance or make transitions unrelated to the operation of the latch. These unrelated input transitions switch the input circuitry and typically cause an increase in power dissipation in CMOS devices by creating a low resistance path between V_{CC} and GND when the signal is at or near the input switching threshold. Additionally, if the driving signal becomes high impedance ("float" condition), it could create an indeterminate logic state at the inputs and cause a disruption in device operation.

The Harris 82C8X series of bus drivers eliminates these conditions by turning off data inputs when data is latched (STB = logic zero for the 82C82/83H) and when the device is disabled ($\overline{OE}$ = logic one for 82C86H/87H). These gated inputs disconnect the input circuitry from the V_{CC} and ground power supply pins by turning off the upper P-channel and lower N-channel (see Figure 6a, 6b). No current flow from V_{CC} to GND occurs during input transitions and invalid logic states from floating inputs are not transmitted. The next stage is held to a valid logic level internal to the device.

D.C. input voltage levels can also cause an increase in I_{CC} if these input levels approach the minimum V_{IH} or maximum V_{IL} conditions. This is due to the operation of the input circuitry in its linear operating region (partially conducting state). The 82C8X series gated inputs mean that this condition will occur only during the time the device is in the transparent mode (STB = logic one). I_{CC} remains below the maximum I_{CC} standby specification of 10 µA during the time inputs are disabled, thereby greatly reducing the average power dissipation of the 82C8X series devices.

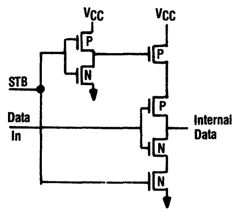


Figure 6a
82C82/83H

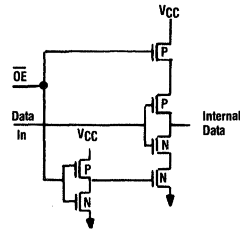


Figure 6b
82C86H/87H Gated Inputs

TYPICAL 82C83H SYSTEM EXAMPLE

In a typical 80C86/88 system, the 82C83H is used to latch multiplexed addresses and the STB input is driven by ALE (Address Latch Enable) (see Figure 7). The high pulse width of ALE is approximately 100ns with a bus cycle time of 800ns (80C86/88 @ 5MHz). The 82C83H inputs are active only 12.5% of the bus cycle time. Average power dissipation related to input transitioning is reduced by this factor also.

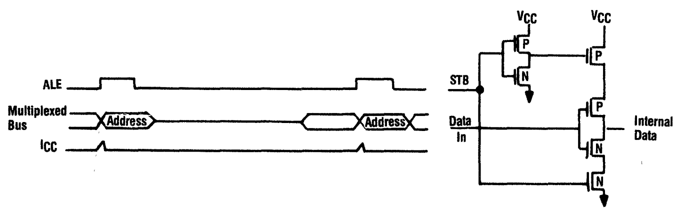


Figure 7
System Effects of Gated Inputs

ADVANCE INFORMATION

82C84A

CMOS Clock Generator Driver

Features

- Generates the System Clock For CMOS or NMOS Microprocessors
- Up to 25MHz Operation
- Uses a Parallel Mode Crystal Circuit or External Frequency Source
- Provides Ready Synchronization
- Generates System Reset Output From Schmitt Trigger Input
- Capable of Clock Synchronization With Other 82C84As
- TTL Compatible Inputs/Outputs
- Very Low Power Consumption
- Single +5V Power Supply
- Wide Operating Temperature Ranges:
  - C82C84A .... 0°C to +70°C
  - I82C84A .... -40°C to +85°C
  - M82C84A .... -55°C to +125°C

Description

The Harris 82C84A is a high performance CMOS clock generator-driver which is designed to service the requirements of both CMOS and NMOS microprocessors such as the 80C86, 80C88, 8086 and the 8088. The chip contains a crystal controlled oscillator, a divide-by-three counter and complete "Ready" synchronization and reset logic.

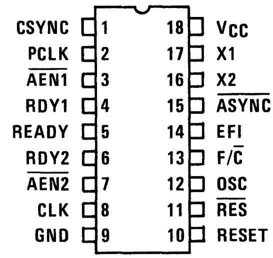
Static CMOS circuit design permits operation with an external frequency source from DC to 25MHz. Crystal controlled operation to 25MHz is guaranteed with the use of a parallel, fundamental mode crystal and two small load capacitors.

All inputs (except X1, X2 and $\overline{RES}$) are TTL compatible over temperature and voltage ranges.

Power consumption is a fraction of that of the equivalent bipolar circuits. This speed-power characteristic of CMOS permits the designer to custom tailor his system design with respect to power and/or speed requirements.

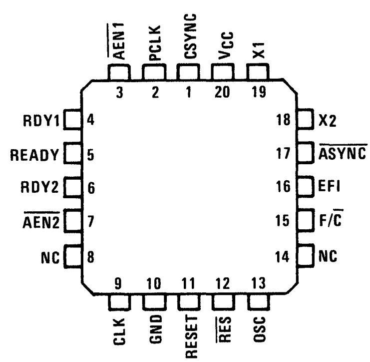
Pinouts

TOP VIEW

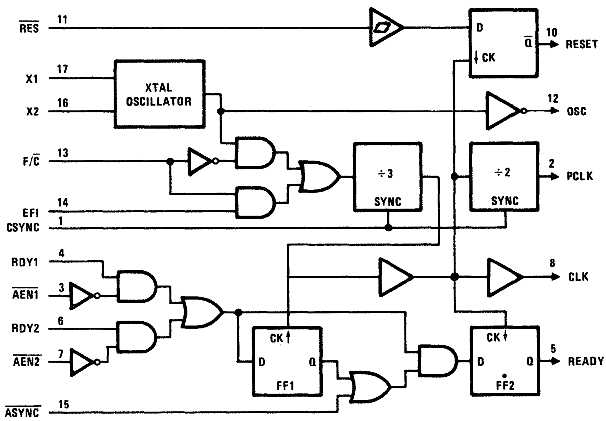


LCC/PLCC

TOP VIEW



Block Diagram



CONTROL PIN	LOGICAL 1	LOGICAL 0
F/$\overline{C}$	External Clock	Crystal Drive
$\overline{RES}$	Normal	Reset
RDY1 RDY2	Bus Ready	Bus Not Ready
$\overline{AEN1}$ $\overline{AEN2}$	Address Disabled	Address Enabled
$\overline{ASYNC}$	2 Stage Ready Synchronization	1 Stage Ready Synchronization

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Pin Description

TABLE 1.

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
$\overline{AEN1}$, $\overline{AEN2}$	3, 7	I	ADDRESS ENABLE: $\overline{AEN}$ is an active LOW signal. $\overline{AEN}$ serves to qualify its respective Bus Ready Signal (RDY1 or RDY2). $\overline{AEN1}$ validates RDY1 while $\overline{AEN2}$ validates RDY2. Two AEN signal inputs are useful in system configurations which permit the processor to access two Multi-Master System Busses. In non-Multi-Master configurations, the $\overline{AEN}$ signal inputs are tied true (LOW).
RDY 1, RDY 2	4, 6	I	BUS READY (Transfer Complete). RDY is an active HIGH signal which is an indication from a device located on the system data bus that data has been received, or is available. RDY1 is qualified by AEN1 while RDY2 is qualified by AEN2.
$\overline{ASYNC}$	15	I	READY SYNCHRONIZATION SELECT: $\overline{ASYNC}$ is an input which defines the synchronization mode of the READY logic. When $\overline{ASYNC}$ is low, two stages of READY synchronization are provided. When $\overline{ASYNC}$ is left open or HIGH a single stage of READY synchronization is provided.
READY	5	O	READY: READY is an active HIGH signal which is the synchronized RDY signal input. READY is cleared after the guaranteed hold time to the processor has been met.
X1, X2	17, 16	I	CRYSTAL IN: X1 and X2 are the pins to which a crystal is attached. The crystal frequency is 3 times the desired processor clock frequency.*
F/$\overline{C}$	13	I	FREQUENCY/CRYSTAL SELECT: F/$\overline{C}$ is a strapping option. When strapped LOW, F/$\overline{C}$ permits the processor's clock to be generated by the crystal. When F/$\overline{C}$ is strapped HIGH, CLK is generated from the EFI input.
EFI	14	I	EXTERNAL FREQUENCY IN: When F/$\overline{C}$ is strapped HIGH, CLK is generated from the input frequency appearing on this pin. The input signal is a square wave 3 times the frequency of the desired CLK output.
CLK	8	O	PROCESSOR CLOCK: CLK is the clock output used by the processor and all devices which directly connect to the processor's local bus. CLK has an output frequency which is 1/3 of the crystal or EFI input frequency and a 1/3 duty cycle.
PCLK	2	O	PERIPHERAL CLOCK: PCLK is a peripheral clock signal whose output frequency is 1/2 that of CLK and has a 50% duty cycle.
OSC	12	O	OSCILLATOR OUTPUT: OSC is the output of the internal oscillator circuitry. Its frequency is equal to that of the crystal.
$\overline{RES}$	11	I	RESET IN: $\overline{RES}$ is an active LOW signal which is used to generate RESET. The 82C84A provides a Schmitt trigger input so that an RC connection can be used to establish the power-up reset of proper duration.
RESET	10	O	RESET: RESET is an active HIGH signal which is used to reset the 80C86 family processors. Its timing characteristics are determined by $\overline{RES}$.
CSYNC	1	I	CLOCK SYNCHRONIZATION: CSYNC is an active HIGH signal which allows multiple 82C84As to be synchronized to provide clocks that are in phase. When CSYNC is HIGH the internal counters are reset. When CSYNC goes LOW the internal counters are allowed to resume counting. CSYNC needs to be externally synchronized to EFI. When using the internal oscillator CSYNC should be hardwired to ground.
GND	9		Ground
VCC	18		VCC: the +5V power supply pin. A 0.1μF capacitor between pins 18 and 9 is recommended for decoupling.

*If the crystal inputs are not used X1 must be tied to VCC or GND and X2 should be left open.

Functional Description

Oscillator

The oscillator circuit of the 82C84A is designed primarily for use with an external parallel resonant, fundamental mode crystal from which the basic operating frequency is derived.

The crystal frequency should be selected at three times the required CPU clock. X1 and X2 are the two crystal input crystal connections. For the most stable operation of the oscillator (OSC) output circuit, two capacitors (C1 = C2) as shown in the waveform figures are recommended. The output of the oscillator is buffered and brought out on OSC so that other system timing signals can be derived from this stable, crystal-controlled source.

Capacitors C1, C2 are chosen such that their combined capacitance

$$CT = \frac{C1 \times C2}{C1 + C2} \text{ (Including stray capacitance)}$$

matches the load capacitance as specified by the crystal manufacturer. This insures operation within the frequency tolerance specified by the crystal manufacturer.

Clock Generator

The clock generator consists of a synchronous divide-by-three counter with a special clear input that inhibits the counting. This clear input (CSYNC) allows the output clock to be synchronized with an external event (such as another 82C84A clock). It is necessary to synchronize the CSYNC input to the EFI clock external to the 82C84A. This is accomplished with two flip-flops. (See Figure 1). The counter output is a 33% duty cycle clock at one-third the input frequency.

*The F/$\overline{C}$ input is a strapping pin that selects either the crystal oscillator or the EFI input as the clock for the ÷ 3 counter. If the EFI input is selected as the clock source, the oscillator section can be used independently for another clock source. Output is taken from OSC.

Clock Outputs

The CLK output is a 33% duty cycle clock driver designed to drive the 80C86, 80C88 processors directly. PCLK is a peripheral clock signal whose output frequency is 1/2 that of CLK. PCLK has a 50% duty cycle.

Reset Logic

The reset logic provides a Schmitt trigger input ($\overline{RES}$) and a synchronizing flip-flop to generate the reset timing. The reset signal is synchronized to the falling edge of CLK. A simple RC network can be used to provide power-on reset by utilizing this function of the 82C84A. Waveforms for clocks and reset signals are illustrated in Figure 2.

READY Synchronization

Two READY inputs (RDY1, RDY2) are provided to accommodate two system busses. Each input has a qualifier ($\overline{AEN1}$ and $\overline{AEN2}$, respectively). The $\overline{AEN}$ signals validate their respective RDY signals. If a Multi-Master system is not being used the $\overline{AEN}$ pin should be tied LOW.

Synchronization is required for all asynchronous active-going edges of either RDY input to guarantee that the RDY setup and hold times are met. Inactive-going edges of RDY in normally ready systems do not require synchronization but must satisfy RDY setup and hold as a matter of proper system design.

The $\overline{ASYNC}$ input defines two modes of READY synchronization operation.

When $\overline{ASYNC}$ is LOW, two stages of synchronization are provided for active READY input signals. Positive-going asynchronous READY inputs will first be synchronized to flip-flop one at the rising edge of CLK (requiring a setup time t_{R1VCH}) and then synchronized to flip-flop two at the next falling edge of CLK, after which time the READY output will go active (HIGH). Negative-going asynchronous READY inputs will be synchronized directly to flip-flop two at the falling edge of CLK, after which time the READY output will go inactive. This mode of operation is intended for use by asynchronous (normally not ready) devices in the system which cannot be guaranteed by design to meet the required RDY setup timing, t_{R1VCL}, on each bus cycle. (Refer to Figure 3.)

When $\overline{ASYNC}$ is high or left open, the first READY flip-flop is bypassed in the READY synchronization logic. READY inputs are synchronized by flip-flop two on the falling edge of CLK before they are presented to the processor. This mode is available for synchronous devices that can be guaranteed to meet the required RDY setup time. (Refer to Figure 4.)

$\overline{ASYNC}$ can be changed on every bus cycle to select the appropriate mode of synchronization for each device in the system.

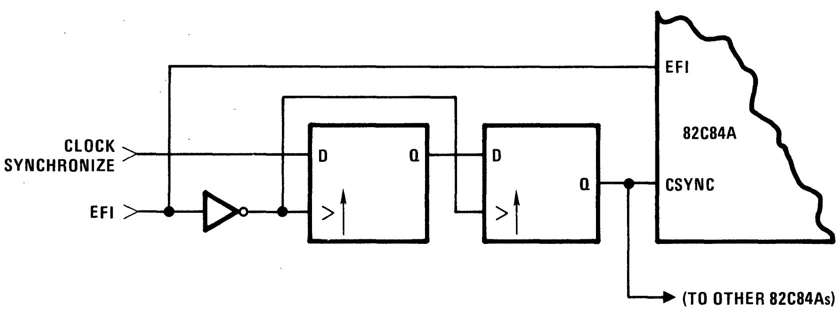


FIGURE 1. CSYNC SYNCHRONIZATION

*NOTE: If EFI input is used, then crystal input X1 must be tied to VCC or GND and X2 should be left open. If the crystal inputs are used, then EFI should be tied to VCC or GND.

Absolute Maximum Ratings

Supply Voltage .... +8.0 Volts
Input, Output or I/O Voltage Applied .... GND -0.5V to VCC +0.5V
Storage Temperature Range .... -65°C to +150°C
Maximum Package Power Dissipation .... 1 Watt
θ_{jc} .... 28°C/W (CERDIP Package), 33°C/W (LCC Package)
θ_{ja} .... 81°C/W (CERDIP Package), 86°C/W (LCC Package)
Gate Count .... 50 Gates
Junction Temperature .... +150°C
Lead Temperature (Soldering, Ten Seconds) .... +260°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +4.5V to +5.5V
Operating Temperature Range
C82C84A .... 0°C to +70°C
I82C84A .... -40°C to +85°C
M82C84A .... -55°C to +125°C

D.C. Electrical Specifications

VCC = 5.0V ±10%;
T_A = 0°C to +70°C (C82C84A);
T_A = -40°C to +85°C (I82C84A);
T_A = -55°C to +125°C (M82C84A)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	Logical One Input Voltage	2.0 2.2		V V	C82C84A, I82C84A M82C84A
VIL	Logical Zero Input Voltage		0.8	V	
VIHR	Reset Input High Voltage	VCC -0.8		V	
VILR	Reset Input Low Voltage		0.5	V	
VT+ - VT-	Reset Input Hysteresis	0.2 VCC			
VOH	Logical One Output Voltage	VCC -0.4		V	IOH = -4.0mA for CLK Output IOH = -2.5mA For All Others
VOL	Logical Zero Output Voltage		0.4	V	IOL = +4.0mA for CLK Output IOL = +2.5mA For All Others
II	Input Leakage Current	-1.0	1.0	μA	VIN = VCC or GND except $\overline{\text{ASYNC}}$, X1: See Note 1.
ICCOP	Operating Power Supply Current		40	mA	Crystal Frequency = 25MHz Outputs Open

NOTES: 1. ASYNC pin includes an internal 17.5KΩ nominal pull-up resistor. For $\overline{\text{ASYNC}}$ input at GND, $\overline{\text{ASYNC}}$ input leakage current = 130μA nominal. X1 - crystal feedback input.

Capacitance T_A = 25°C. VCC = GND = 0V; VIN = +5V or GND.

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
CIN	Input Capacitance	5	pF	Frequency = 1MHz

A.C. Electrical Specifications

T_A = 0°C to +70°C, V_{CC} = 5V ±10% – C82C84A
T_A = -40°C to +85°C, V_{CC} = 5V ±10% –I82C84A
T_A = -55°C to +125°C, VCC = 5V ±10% –M82C84A

TIMING REQUIREMENTS

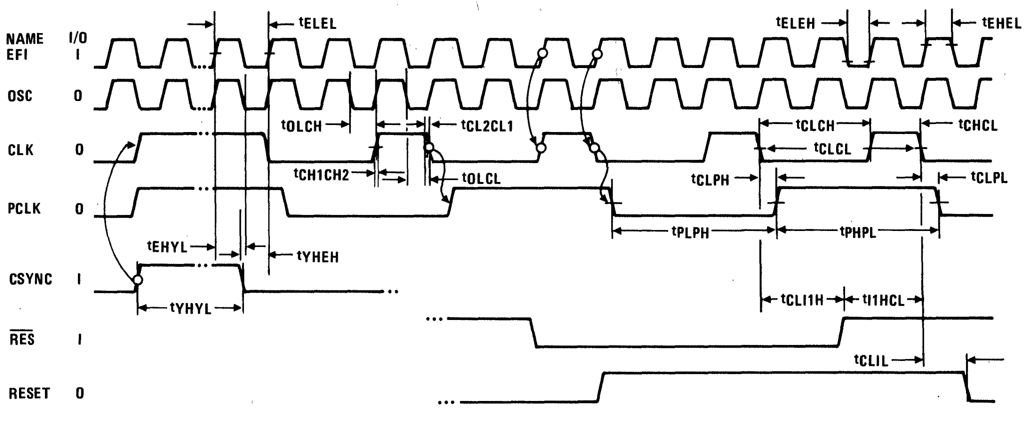
Symbol	Parameter	Min.	Max.	Units	Test Conditions
t_{EHEL}	External Frequency HIGH Time	13		ns	90% - 90% V_{IN}
t_{ELEH}	External Frequency LOW Time	13		ns	10%-10% V_{IN}
t_{ELEL}	EFI Period	36		ns	
	XTAL Frequency	2.4	25	MHz	
t_{R1VCL}	RDY1, RDY2 Active Setup to CLK	35		ns	ASYNC = HIGH
t_{R1VCH}	RDY1, RDY2 Active Setup to CLK	35		ns	ASYNC = LOW
t_{R1VCL}	RDY1, RDY2 Inactive Setup to CLK	35		ns	
t_{CLR1X}	RDY1, RDY2 Hold to CLK	0		ns	
t_{AYVCL}	ASYNC Setup to CLK	50		ns	
t_{CLAYX}	ASYNC Hold to CLK	0		ns	
t_{A1VR1V}	AEN1, AEN2 Setup to RDY1, RDY2	15		ns	
t_{CLA1X}	AEN1, AEN2 Hold to CLK	0		ns	
t_{YHEH}	CSYNC Setup to EFI	20		ns	
t_{EHYL}	CSYNC Hold to EFI	20		ns	
t_{YHYL}	CSYNC Width	$2 \cdot t_{ELEL}$		ns	
t_{I1HCL}	RES Setup to CLK	65		ns	(Note 2)
t_{CLI1H}	RES Hold to CLK	20		ns	(Note 2)

TIMING RESPONSES

Symbol	Parameter	Min.	Max.	Units	Test Conditions
t_{CLCL}	CLK Cycle Period	125		ns	
t_{CHCL}	CLK HIGH Time	(1/3 t_{CLCL}) +2.0		ns	Fig. 7 & Fig. 8
t_{CLCH}	CLK LOW Time	(2/3 t_{CLCL}) -15.0		ns	Fig. 7 & Fig. 8
t_{CH1CH2} t_{CL2CL1}	CLK Rise or Fall Time		10	ns	1.0V to 3.5V
t_{PHPL}	PCLK HIGH Time	t_{CLCL}-20		ns	
t_{PLPH}	PCLK LOW Time	t_{CLCL}-20		ns	
t_{RYLCL}	Ready Inactive to CLK (See note 4)	-8		ns	Fig. 8 & Fig. 10
t_{RYHCH}	Ready Active to CLK (See note 3)	(2/3 t_{CLCL}) -15.0		ns	Fig. 9 & Fig. 10
t_{CLIL}	CLK to Reset Delay		40	ns	
t_{CLPH}	CLK to PCLK HIGH Delay		22	ns	
t_{CLPL}	CLK to PCLK LOW Delay		22	ns	
t_{OLCH}	OSC to CLK HIGH Delay	-5	22	ns	
t_{OLCL}	OSC to CLK LOW Delay	2	35	ns	

NOTES:
1. Output signals switch between VOH and VOL unless otherwise specified.
2. Setup and hold necessary only to guarantee recognition at next clock.
3. Applies only to T3 TW states.
4. Applies only to T2 states.
5. All timing delays are measured at 1.5 volts unless otherwise noted.
6. Input rise and fall times are driven at Ins/V.

+Figure 11 illustrates test load measurement condition.



NOTE: ALL TIMING MEASUREMENTS ARE MADE AT 1.5 VOLTS, UNLESS OTHERWISE NOTED.

FIGURE 2. WAVEFORMS FOR CLOCKS AND RESET SIGNALS

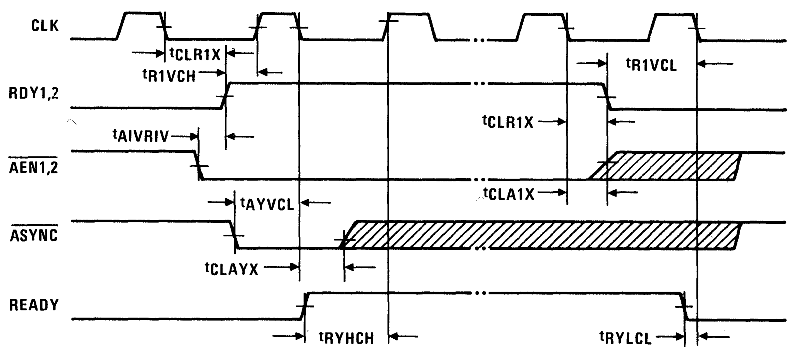


FIGURE 3. WAVEFORMS FOR READY SIGNALS (FOR ASYNCHRONOUS DEVICES)

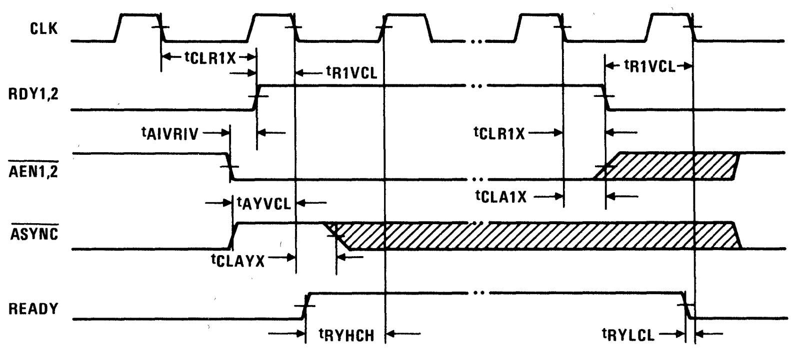


FIGURE 4. WAVEFORMS FOR READY SIGNALS (FOR SYNCHRONOUS DEVICES)

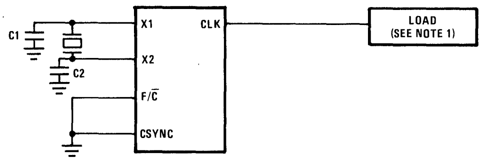


FIGURE 5. CLOCK HIGH AND LOW TIME (USING X1, X2)

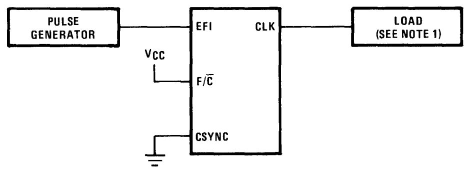


FIGURE 6. CLOCK HIGH AND LOW TIME (USING EFI)

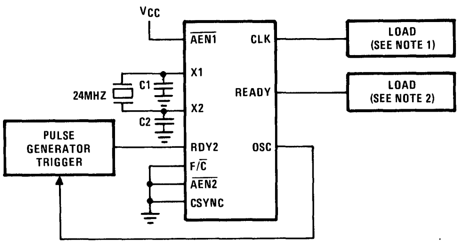


FIGURE 7. READY TO CLOCK (USING X1, X2)

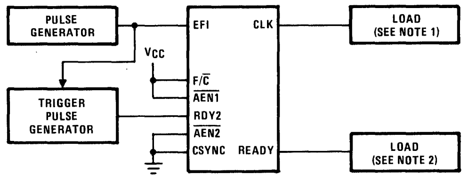


FIGURE 8. READY TO CLOCK (USING EFI)

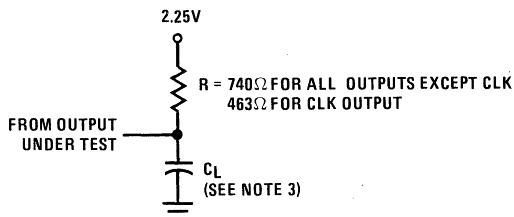
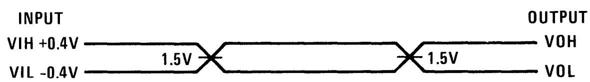


FIGURE 9. TEST LOAD MEASUREMENT CONDITIONS

NOTES:
1. C_L = 100pF
2. C_L = 30pF
3. C_L INCLUDES PROBE AND JIG CAPACITANCE

A.C. Testing Input, Output Waveforms



* A.C. Testing: All parameters tested as per test circuits.
Input rise and fall times are driven at 1ns/V.

PARAMETER	TYPICAL CRYSTAL SPEC
Frequency	2.4 - 25MHz, Fundamental, "AT" cut
Type of Operation	Parallel
Unwanted Modes	-6db (Minimum)
Load Capacitance	18 - 32pf

TABLE 2. CRYSTAL SPECIFICATIONS

See Harris Publication TB-47 for recommended crystal specifications.

82C85

CMOS Static Clock Controller/Generator

Features

- Generates System Clocks for CMOS or NMOS Microprocessors and Peripherals
- Complete Control Over System Clock Operation for Very Low System Power
  - ▶ Stop-Oscillator ▶ Low Frequency
  - ▶ Stop-Clock ▶ Full Speed Operation
- DC to 25 MHz Operation (DC to 8 MHz System Clock)
- Generates Both 50% and 33% Duty Cycle Clocks (Synchronized)
- Uses a Parallel Mode Crystal Circuit or External Frequency Source
- TTL/CMOS Compatible Inputs/Outputs
- 24-Pin Slimline Dual-In-Line or 28-Pad Square LCC Package Options
- Wide Operating Temperature Ranges:
  - ▶ C82C85 .... 0°C to +70°C
  - ▶ I82C85 .... -40°C to +85°C
  - ▶ M82C85 .... -55°C to +125°C

Description

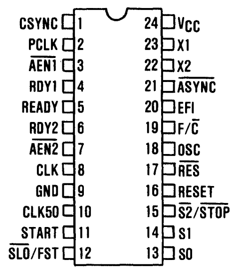
The Harris 82C85 Static CMOS Clock Controller/Generator provides simple, complete control of static CMOS system operating modes and supports full speed, slow, stop-clock and stop-oscillator operation. While directly compatible with the Harris 80C86/80C88 16-bit Static CMOS Microprocessor Family, the 82C85 can also be used for general system clock control.

For static system designs, separate signals are provided on the 82C85 for stop (S0, S1, $\overline{S2}/\overline{STOP}$) and start ($\overline{START}$) control of the crystal oscillator and system clocks. A single control line ($\overline{SLO}$/FST) determines 82C85 fast (crystal/EFI frequency divided by 3) or slow (crystal/EFI frequency divided by 768) mode operation. Automatic maximum mode 80C86/88 software HALT instruction decode logic in the 82C85 enables software-based clock control. Restart logic insures valid clock start-up and complete synchronization of system clocks.

The 82C85 is manufactured using the Harris advanced Scaled SAJI IV CMOS process. In addition to clock control circuitry, the 82C85 also contains a crystal controlled oscillator (up to 25 MHz), clock generation logic, complete "Ready" synchronization and reset logic. This permits the designer to tailor the system power-performance product to provide optimum performance at low power levels.

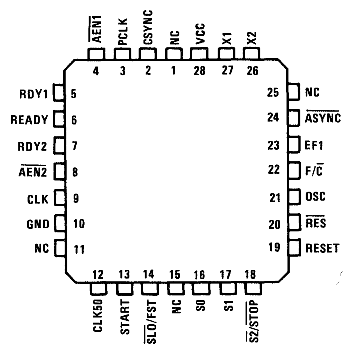
Pinouts

TOP VIEW

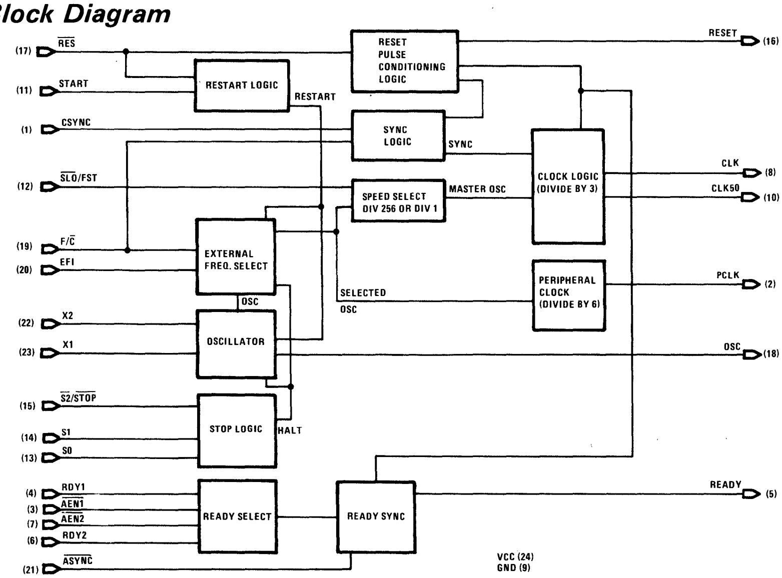


LCC/PLCC

TOP VIEW



Functional Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Pin Description

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
X1 X2	23 22	I O	CRYSTAL CONNECTIONS: X1 and X2 are the crystal oscillator connections. The crystal frequency must be 3 times the maximum desired processor clock frequency. X1 is the oscillator circuit input and X2 is the output of the oscillator circuit.
EFI	20	I	EXTERNAL FREQUENCY IN: When F/$\overline{C}$ is HIGH, CLK is generated from the EFI input signal. This input signal should be a square wave with a frequency of three times the maximum desired CLK output frequency.
F/$\overline{C}$	19	I	FREQUENCY/CRYSTAL SELECT: F/$\overline{C}$ selects either the crystal oscillator or the EFI input as the main frequency source. When F/$\overline{C}$ is LOW, the 82C85 clocks are derived from the crystal oscillator circuit. When F/$\overline{C}$ is HIGH, CLK is generated from the EFI input. F/$\overline{C}$ cannot be dynamically switched during normal operation.
START	11	I	A low-to-high transition on START will restart the CLK, CLK50 and PCLK outputs after the appropriate restart sequence is completed. When in the crystal mode (F/$\overline{C}$ LOW) with the oscillator stopped, the oscillator will be restarted when a Start command is received. The CLK, CLK50 and PCLK outputs will start after the oscillator input signal (X1) reaches the Schmitt trigger input threshold and an 8K internal counter reaches terminal count. If F/$\overline{C}$ is HIGH (EFI mode), CLK, CLK50 and PCLK will restart within 3 EFI cycles after START is recognized. The 82C85 will restart in the same mode ($\overline{SLO}$/FST) in which it stopped. A high level on START disables the STOP mode.
S0 S1 $\overline{S2}$/$\overline{STOP}$	13 14 15	I I I	$\overline{S2}$/$\overline{STOP}$, S1, S0 are used to stop the 82C85 clock outputs (CLK, CLK50, PCLK) and are sampled by the rising edge of CLK. CLK, CLK50 and PCLK are stopped by $\overline{S2}$/$\overline{STOP}$, S1, S0 being in the LHH state on the low-to-high transition of CLK. This LHH state must follow a passive HHH state ocurring on the previous low-to-high CLK transition. CLK and CLK50 stop in the high state. PCLK stops in it's current state (high or low). When in the crystal mode (F/$\overline{C}$) low and a STOP command is issued, the 82C85 oscillator will stop along with the CLK, CLK50 and PCLK outputs. When in the EFI mode, only the CLK, CLK50 and PCLK outputs will be halted. The oscillator circuit if operational, will continue to run. The oscillator and/or clock is restarted by the START input signal going true (HIGH) or the reset input ($\overline{RES}$) going low.
$\overline{SLO}$/FST	12	I	$\overline{SLO}$/FST is a level-triggered input. When HIGH, the CLK and CLK50 outputs run at the maximum frequency (crystal or EFI frequency divided by 3). When LOW, CLK and CLK50 frequencies are equal to the crystal or EFI frequency divided by 768. $\overline{SLO}$/FST mode changes are internally synchronized to eliminate glitches on the CLK and CLK50. START and STOP control of the oscillator or EFI is available in either the SLOW or FAST frequency modes. The $\overline{SLO}$/FST input must be held LOW for at least 195 OSC/EFI clock cycles before it will be recognized. This eliminates unwanted frequency changes which could be caused by glitches or noise transients. The $\overline{SLO}$/FST input must be held HIGH for at least 6 OSC/EFI clock pulses to guarantee a transition to FAST mode operation.
CLK	8	O	PROCESSOR CLOCK: CLK is the clock output used by the 80C86 or 80C88 processor and other peripheral devices. When $\overline{SLO}$/FST is high, CLK has an output frequency which is equal to the crystal or EFI input frequency divided by three. When $\overline{SLO}$/FST is low, CLK has an output frequency which is equal to the crystal or EFI input frequency divided by 768. CLK has a 33% duty cycle.
CLK50	10	O	50% DUTY CYCLE CLOCK: CLK50 is an auxiliary clock with a 50% duty cycle and is synchronized to the falling edge of CLK. When $\overline{SLO}$/FST is high, CLK50 has an output frequency which is equal to the crystal or EFI input frequency divided by 3. When $\overline{SLO}$/FST is low, CLK50 has an output frequency equal to the crystal or EFI input frequency divided by 768.
PCLK	2	O	PERIPHERAL CLOCK: PCLK is a peripheral clock signal whose output frequency is equal to the crystal or EFI input frequency divided by 6 and has a 50% duty cycle. PCLK frequency is unaffected by the state of the $\overline{SLO}$/FST input.

Pin Description

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
OSC	18	O	OSCILLATOR OUTPUT: OSC is the output of the internal oscillator circuitry. Its frequency is equal to that of the crystal oscillator circuit. OSC is unaffected by the state of the $\overline{SLO}$/FST input.
			When the 82C85 is in the crystal mode (F/$\overline{C}$ low) and a STOP command is issued, the OSC output will stop in the HIGH state. When the 82C85 is in the EFI mode (F/$\overline{C}$ HIGH), the oscillator (if operational) will continue to run when a STOP command is issued and OSC remains active.
$\overline{RES}$	17	I	RESET IN: $\overline{RES}$ is an active LOW signal which is used to generate RESET. The 82C85 provides a Schmitt trigger input so that an RC connection can be used to establish the power-up reset of proper duration. $\overline{RES}$ starts cyrstal oscillator operation.
RESET	16	O	RESET: RESET is an active HIGH signal which is used to reset the 80C86 family processors. Its timing characteristics are determined by $\overline{RES}$. RESET is guaranteed to be HIGH for a minimum of 16 CLK pulses after the rising edge of $\overline{RES}$.
CSYNC	1	I	CLOCK SYNCHRONIZATION: CSYNC is an active HIGH signal which allows multiple 82C85s and 82C84As to be synchronized to provide multiple in-phase clock signals. When CSYNC is HIGH, the internal counters are reset and force CLK, CLK50 and PCLK into a HIGH state. When CSYNC is LOW, the internal counters are allowed to count and the CLK, CLK50 and PCLK outputs are active. CSYNC must be externally synchronized to EFI.
$\overline{AEN1}$ $\overline{AEN2}$	3 7	I I	ADDRESS ENABLE: $\overline{AEN}$ is an active LOW signal. $\overline{AEN}$ serves to qualify its respective Bus Ready Signal (RDY1 or RDY2). $\overline{AEN1}$ validates $\overline{RDY1}$ while $\overline{AEN2}$ validates RDY2. Two $\overline{AEN}$ signal inputs are useful in system configurations which permit the processor to access two Multi-Master System Buses.
RDY1 RDY2	4 6	I I	BUS READY: (Transfer Complete). RDY is an active HIGH signal which is an indication from a device located on the system data bus that data has been received, or is available. RDY1 is qualified by $\overline{AEN1}$ while RDY2 is qualified by $\overline{AEN2}$.
$\overline{ASYNC}$	21	I	READY SYNCHRONIZATION SELECT: $\overline{ASYNC}$ is an input which defines the synchronization mode of the READY logic. When $\overline{ASYNC}$ is LOW, two stages of READY synchronization are provided. When $\overline{ASYNC}$ is left open or HIGH a single stage of READY synchronization is provided.
READY	5	O	READY: READY is an active HIGH signal which is the synchronized RDY signal input.
GND	9	I	Ground
VCC	24	I	VCC: is the +5V power supply pin. A 0.1μF capacitor between pins 24 and 9 is recommended.

Functional Description

The 82C85 Static Clock Controller/Generator provides simple and complete control of static CMOS system operating modes. The 82C85 supports full speed, slow, stop-clock and stop-oscillator operation. While it is directly compatible with the Harris 80C86 and 80C88 CMOS 16-bit static microprocessors, the 82C85 can also be used for general purpose system clock control.

The 82C85 pinout is a superset of the 82C84A Clock Generator/Driver. 82C85 pins 1-9, 16-24 are compatible with 82C84A pins 1-9, 10-18, respectively. An 82C84A can be placed in the upper 18 pins of an 82C85 socket and it will operate correctly (without the ability to control the clock and oscillator operation.) This allows dual design for simple system upgrades. The 82C85 will also emulate an 82C84A when pins 11-15 on the 82C85 are tied to VCC.

For static system designs, separate signals are provided on the 82C85 for stop and start control of the crystal oscillator and clock outputs. A single control line determines 82C85 fast (crystal/EFI frequency divided by 3) or slow (crystal/EFI frequency divided by 768) mode operation. The 82C85 also contains a crystal controlled oscillator, clock generation logic, complete "Ready" synchronization and reset logic.

Automatic 80C86/88 software HALT instruction decode logic is present to ease the design of software-based clock control systems and provide complete software control of STOP mode operation. Restart logic insures valid clock start-up and complete synchronization of CLK, CLK50 and PCLK.

Static Operating Modes

In static CMOS system design, there are four basic operating modes. The 82C85 Static Clock Controller supports each of them. These modes are: FAST, SLOW, STOP-CLOCK and STOP-OSCILLATOR. Each has distinct power and performance characteristics which can be matched to the needs of a particular system at a specific time (See Table 1).

Keep in mind that a single system may require all of these operating modes at one time or another during normal operation. A design need not be limited to a single operating mode or a specific combination of modes. The appropriate operating mode can be matched to the power-performance level needed at a specific time or in a particular circumstance.

Reset Logic

The 82C85 reset logic provides a Schmitt trigger input ($\overline{RES}$) and a synchronizing flip-flop to generate the reset timing. The reset signal is synchronized to the falling edge of CLK. A simple RC network can be used to provide power-on reset by utilizing this function of the 82C85.

When in the crystal oscillator (F/$\overline{C}$ = LOW) or the EFI (F/$\overline{C}$ = HIGH) mode, a LOW state on the $\overline{RES}$ input will set the RESET output to the HIGH state. It will also restart the oscillator circuit if it is in the idle state. The RESET output is guaranteed to stay in the HIGH state for a minimum of 16 CLK cycles after a low-to-high transition of the $\overline{RES}$ input.

An oscillator restart count sequence will not be disturbed by RESET if this count is already in progress. After the restart counter expires, the RESET output will stay HIGH at least for 16 periods of CLK before going LOW. RESET can be kept high beyond this time by a continuing low input on the $\overline{RES}$ input.

If F/$\overline{C}$ is low (crystal oscillator mode), a low state on $\overline{RES}$ starts the crystal oscillator circuit. The stopped outputs remain inactive until the oscillator signal amplitude reaches the X1 Schmitt trigger input threshold voltage and 8192 cycles of the crystal oscillator output are counted by an internal counter. After this count is complete, the stopped outputs (CLK, CLK50, PCLK) start cleanly with the proper phase relationships.

This 8192 count requirement insures that the CLK, CLK50 and PCLK outputs will meet minimum clock requirements and will not be affected by unstable oscillator characteristics which may exist during the oscillator start-up sequence. This sequence is also followed when a START command is issued while the 82C85 oscillator is stopped.

Oscillator/Clock Start Control

Once the oscillator is stopped (or committed to stop) or at power-on, the restart sequence is initiated by a HIGH state on START or LOW state on $\overline{RES}$. If F/$\overline{C}$ is HIGH, then restart occurs immediately after the START or $\overline{RES}$ input is synchronized internally. This insures that stopped outputs (CLK, PCLK, OSC and CLK50) start cleanly with the proper phase relationship.

If F/$\overline{C}$ is low (crystal oscillator mode), a HIGH state on the START input or a low state on $\overline{RES}$ causes the crystal oscillator to be restarted. The stopped outputs remain stopped, until the oscillator signal amplitude reaches the X1 Schmitt trigger input threshold voltage and 8192 cycles of the crystal oscillator output are counted by an internal counter. After this count is complete, the stopped outputs (CLK, CLK50, PCLK) start cleanly with the proper phase relationships.

TABLE 1. STATIC SYSTEM OPERATING MODE CHARACTERISTICS

OPERATING MODE	DESCRIPTION	POWER LEVEL	PERFORMANCE
Stop - Oscillator	All system clocks and main clock oscillator are stopped	Maximum savings	Slowest response due to oscillator restart time
Stop - Clock	System CPU and peripherals clocks stop but main clock oscillator continues to run at rated frequency	Reduced system power	Fast restart — no oscillator restart time
Slow	System CPU clocks are slowed while peripheral clock and main clock oscillator run at rated frequency	Power dissipation slightly higher than Stop-Clock	Continuous operation at low frequency
Fast	All clocks and oscillators run at rated frequency	Highest power	Fastest response

Typically, any input signal which meets the START input timing requirements can be used to start the 82C85. In many cases, this would be the INT output from an 82C59A CMOS Priority Interrupt Controller (See Figure 1). This output, which is active high, can be connected to both the 82C85 START pin and to the appropriate interrupt request input on the microprocessor.

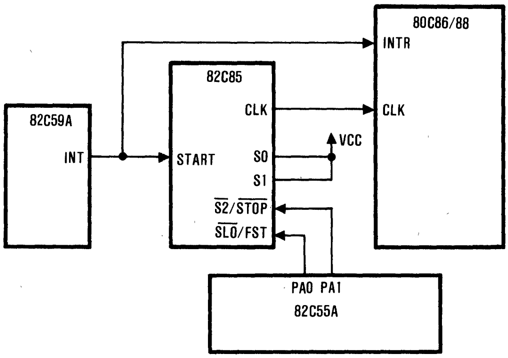


FIGURE 1. CMOS PERIPHERAL CONTROL OF 82C85 STOP, START AND SLOW/FAST OPERATIONS

When the INT output becomes active, the oscillator/clock circuit on the 82C85 will restart. Upon completion of the appropriate restart sequence, the CLK signal to the CPU will become active. The CPU can then respond to the still-pending interrupt request.

If the 82C59A/82C85 restart combination is used in conjunction with an 82C55A $\overline{STOP}$ control, the 82C55A must be initialized prior to the 82C59A after reset. The 82C59A interrupt output is driven high at reset, causing the 82C85 to remain in the START mode regardless of the state of the $\overline{S2}/\overline{STOP}$ input. This will avoid stopping the 82C85 due to negative transitions on the $\overline{S2}/\overline{STOP}$ input which may occur during a mode change on the 82C55A or during the operation of any peripheral I/O device prior to initialization.

Another method of insuring proper operation of the START function upon reset or system initialization is to bias the $\overline{S2}/\overline{STOP}$ input low with an external pull-down resistor. The $\overline{S2}/\overline{STOP}$ input will remain low until driven high by the 82C55A port pin or by external logic. This insures that the 82C85 STOP command (HHH prior to LHH requirement on the status inputs) will not be satisfied. To minimize power dissipation in this case (using a pull-down resistor), the $\overline{S2}/\overline{STOP}$ input should be normally LOW and pulsed HIGH to develop the necessary HHH-to-LHH $\overline{STOP}$ sequence. In this manner, the output driving the $\overline{S2}/\overline{STOP}$ input be normally LOW and will not be driving to the opposite state of the pull-down resistor.

Fast Mode

The most common operating mode for a system is the FAST mode. In this mode, the 82C85 operates at the maximum frequency determined by the main oscillator or EFI frequency. FAST mode operation is enabled by each of two conditions:

— The $\overline{SLO}/FST$ input is HIGH and a START or reset command is issued

— The $\overline{SLO}/FST$ input is held HIGH for at least 3 oscillator or EFI cycles.

Alternate Operating Modes

Using alternate modes of operation (slow, stop-clock, stop-oscillator) will reduce the average system operating power dissipation in a static CMOS system (See Table 2). This does not mean that system speed or throughput must be reduced. When used appropriately, the slow, stop-clock, stop-oscillator modes can make your design more power-efficient while maintaining maximum system performance.

TABLE 2. TYPICAL SYSTEM POWER SUPPLY CURRENT FOR STATIC CMOS OPERATING MODES

	FAST	SLOW	STOP-CLOCK	STOP-OSC
CPU Freq.	5 MHz	20 KHz	DC	DC
XTAL Freq.	15 MHz	15 MHz	15 MHz	DC
ICC				
82C85	24.7 mA	16.9 mA	14.1 mA	24.4 μA
80C88	23.8 mA	173.0 μA	106.6 μA	106.6 μA
82C82	1.7 mA	6.5 μA	1.0 μA	1.0 μA
82C86	1.4 mA	14.0 μA	1.0 μA	1.0 μA
82C88	3.5 mA	14.3 μA	3.8 μA	3.8 μA
82C52	151.2 μA	72.0 μA	1.0 μA	1.0 μA
82C54	943.0 μA	915.0 μA	3.5 μA	1.0 μA
82C55A	3.2 μA	1.2 μA	1.0 μA	1.0 μA
82C59A	580.0 μA	520.0 μA	1.0 μA	1.0 μA
74HCXX + other	2.9 mA	110.0 μA	90.0 μA	90.0 μA
HM-6516	820.0 μA	132.0 μA	1.9 μA	1.9 μA
HM-6616	6.3 mA	52.5 μA	12.0 μA	12.0 μA
Total	66.8 mA	18.9 mA	13.8 mA	244.7 μA

All measurements taken at room temperature, VCC = +5.0 volts. Power supply current levels will be dependent upon system configuration and frequency of operation.

Stop-Oscillator Mode

When the 82C85 is stopped while in the crystal mode (F/$\overline{C}$ LOW), the oscillator, in addition to all system clock signals (CLK, CLK50 and PCLK), are stopped. CLK and CLK50 stop in the high state. PCLK stops in it's current state (high or low).

With the oscillator stopped, 82C85 power drops to it's lowest level. All clocks and oscillators are stopped. All devices in the system which are driven by the 82C85 go into the lowest power standby mode. The 82C85 also goes into standby and requires a power supply current of less than 100 microamps.

Stop-Clock Mode

When the 82C85 is in the EFI mode (F/$\overline{C}$ HIGH) and a $\overline{STOP}$ command is issued, all system clock signals (CLK, CLK50 and PCLK) are stopped. CLK and CLK50 stop in the high state. PCLK stops in it's current state (high or low).

The 82C85 can also provide it's own EFI source simply by connecting the OSC output to the EFI input and pulling the F/$\overline{C}$ input HIGH. This puts the 82C85 into the External Frequency Mode using it's own oscillator as an external source signal (See Figure 2). In this configuration, when the 82C85 is stopped in the EFI mode, the oscillator continues to run. Only the clocks to the CPU and peripherals (CLK, CLK50 and PCLK) are stopped.

Oscillator/Clock Stop Operation

Three control lines determine when the 82C85 clock outputs or oscillator will stop. These are S0, S1 and $\overline{S2}/\overline{STOP}$. These three lines are designed to connect directly to the MAXimum mode 80C86 and 80C88 status lines or to be driven by external I/O signals (such as an 82C55A output port).

In the MAXimum mode configuration, the 82C85 will automatically recognize a software HALT command from the 80C86 or 80C88 and stop the system clocks or oscillator. This allows complete software control of the $\overline{STOP}$ function.

If the 80C86 or 80C88 is used in the MINimum mode, the 82C85 can be controlled using the $\overline{S2}/\overline{STOP}$ input (with S0 and S1 held high). This can be done using an external I/O control line, such as from an 82C55A or by decoding the state of the 80C86 MINimum mode status signals.

82C85 status inputs $\overline{S2}/\overline{STOP}$, S1, S0 are sampled on the rising edge of CLK. The oscillator (F/$\overline{C}$ LOW only) and clock outputs are stopped by $\overline{S2}/\overline{STOP}$, S1, S0 being in the LHH state on a low-to-high transition of CLK. This LHH state must follow a passive HHH state ocurring on the previous low-to-high CLK transition. CLK and CLK50 will stop in the logic HIGH state after two additional complete cycles of CLK. PCLK stops in it's current state (HIGH or LOW). This is true for both SLOW and FAST mode operation.

80C86/88 Maximum Mode Clock Control

The 82C85 $\overline{STOP}$ function has been optimized for 80C86/88 MAXimum mode operation. In this mode, the three 82C85 status inputs ($\overline{S2}/\overline{STOP}$, S1, S0) are connected directly to the MAXimum mode status lines (S2, S1, S0) of the Harris 80C86 or 80C88 static CMOS microprocessors (See Figure 3).

When in the MAXimum mode, the 80C86/88 status lines identify which type of bus cycle the CPU is starting to execute. 82C85 $\overline{S2}/\overline{STOP}$, S1 and S0 control input logic will recognize a valid MAXimum mode software HALT executed by the 80C86 or 80C88. Once this state has been recognized, the 82C85 stops the clock (F/$\overline{C}$ HIGH) or oscillator (F/$\overline{C}$ LOW) operation.

The 82C85 $\overline{S2}/\overline{STOP}$, S1 and S0 control lines were designed to detect a passive 111 state followed by a HALT 011 logic state before recognizing the HALT instruction and stopping the system clocks. In the MAXimum mode, the 80C86/88 status lines go into a passive (no bus cycle) logic 111 state prior to executing a HALT instruction. The qualification of a passive no bus cycle logic 111 state insures that random transitions of the status lines into a logic 011 state will not stop the system clock. This is necessary since the status lines of the 80C86/88 transition through an unknown state during T3 of the bus cycle.

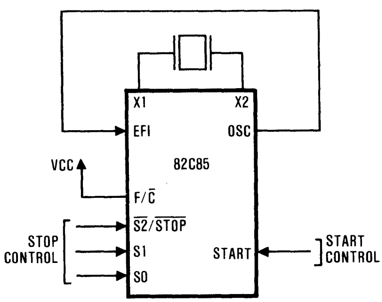


FIGURE 2. STOP-CLOCK MODE USING 82C85 IN EFI MODE WITH OSCILLATOR AS FREQUENCY SOURCE

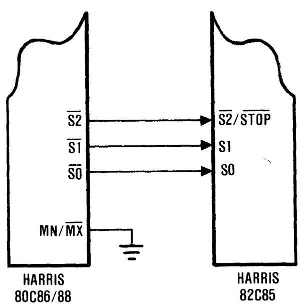


FIGURE 3. 82C85 STOP CONTROL USING 80C86/88 MAXIMUM MODE STATUS LINES

Once the HALT instruction is decoded by the 82C85, either the oscillator is stopped (STOP-OSCILLATOR mode - F/C̄ tied low) or the external frequency source is gated off internally (STOP-CLOCK mode - F/C̄ HIGH). When the HALT instruction is decoded, the CLK and CLK50 will be stopped in a logic high state after 2 additional cycles of the clock. PCLK stops in it's current state (high or low). This is true for both SLOW and FAST mode operation. The halt instruction is detected in the same manner whether the 82C85 is in the SLOW or the FAST mode.

Independent Stop Control for Minimum Mode Operation

When the 80C86 and 80C88 microprocessors are configured in MINimum Mode (MN/M̄X̄ pin tied high), their status lines S0, S1, and S2 assume alternate functions. The logic states and sequences (passive before a HALT) necessary for automatic HALT detect in the 82C85 do not occur as in the MAXimum mode. The 82C85 controller cannot use the microprocessor status lines to detect a software Halt instruction when operating in MINimum mode.

However, the negative edge-activated S̄2̄/S̄T̄ŌP̄ pin provides a simple means for clock control in MINimum mode 80C86 and 80C88 systems. S̄2̄/S̄T̄ŌP̄ can be used as an independent S̄T̄ŌP̄ control when S1 and S2 are held in the logical HIGH state. Keeping the S0 and S1 inputs at a logic 1 level and transitioning S̄2̄/S̄T̄ŌP̄ from high to low will meet the passive 111 state prior to a 011 state requirement of the 82C85. This feature allows 82C85 operation with the 80C86 and 80C88 in the MINimum mode, provides compatibility with other static CMOS microprocessors and allows maximum flexibility in a system.

With S̄2̄/S̄T̄ŌP̄ being used as a stand-alone STOP command line, system clocks can be controlled via an 82C55A programmable peripheral interface or other similar interface circuits. This is accomplished by driving the S̄2̄/S̄T̄ŌP̄ input with a PORT pin on the 82C55A (See Figure 1). The 82C55A port pin should be configured as an output and must present a logic HIGH to the S̄2̄/S̄T̄ŌP̄ input for at least one CLK cycle, followed by a LOW state. This will meet the 82C85 status input requirement of 111 followed by a 011.

When a logic 0 is written to a 82C55A port pin, the S̄2̄/S̄T̄ŌP̄ pin is pulled low, stopping the system clocks (CLK, CLK50, PCLK). In essence, the 82C85 is software controlled via the 82C55A. As with the SLO/F̄S̄T̄ interface, PORT C is a logical choice for this job since the individual bit set and reset commands available for this port make control of the S̄2̄/S̄T̄ŌP̄ input simple.

A START command issued to the 82C85 will override a S̄T̄ŌP̄ command and the 82C85 will begin normal operation. The low state of the negative-edge triggered S̄2̄/S̄T̄ŌP̄ input will not prohibit the clocks from restarting. After a START or R̄ĒS̄ command, the 82C85 must see a passive (111) state followed by a HALT (011) state to stop the system clocks. To accomplish this, the 82C55A port output must be brought high and then returned low again for the 82C85 to recognize the next S̄T̄ŌP̄ command.

External Decode Adds Halt Control

SS0, IO/M̄ and DT/R̄ can identify a MINimum mode 80C88 HALT execution. During T2 of the system timing (while ALE is high), SS0, IO/M̄, and DT/R̄ go into a 111 state when the 80C88 is executing a software HALT. These signals cannot be tied directly to the S̄2̄/S̄T̄ŌP̄, S1 and S0 inputs since they are not guaranteed to go into a passive state prior to their 111 state.

These signals can be decoded during the time ALE is high to indicate a software HALT execution. The Harris HD-6440 latch 3:8 decoder/driver can be used for this purpose (See Figure 4). IO/M̄, DT/R̄, SS0 are connected directly to the three address lines of the HD-6440.

The ALE signal from the 80C86/88 is connected to the HD-6440 Ḡ2̄ and L2 pins. The falling edge of ALE latches the states of IO/M̄, DT/R̄, and SS0 and enables the corresponding HD-6440 output (Y7), which is connected to the 82C85 S̄2̄/S̄T̄ŌP̄ pin. S0 and S1 should be tied high. Once a HALT state (111) has been recognized by the HD-6440, the low-going action of Y7 will stop the 82C85.

Slow Mode

When continuous operation is critical but power consumption remains a concern, the 82C85 SLOW mode operation provides a lower frequency at the CLK and CLK50 outputs (crystal/EFI frequency divided by 768). The frequency of PLCK is unaffected. The SLOW mode allows the CPU and the system to operate at a reduced rate which, in turn, reduces system power.

For example, the operating power for the 80C86 or 80C88 CPU is 10 mA/MHz of clock frequency. When the SLOW mode is used in a typical 5 MHz system, CLK and CLK50 run at approximately 20 kHz. At this reduced frequency, the average operating current of the CPU drops to 200 microamps. Adding the 80C86/88 500 microamps standby current brings the total current to 700 microamps.

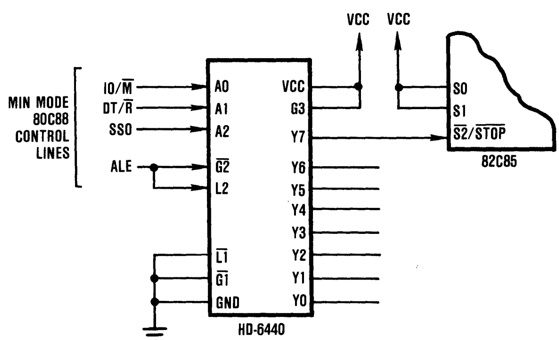


FIGURE 4. AUTOMATIC STOP-ON-HALT WITH MINIMUM MODE 80C88

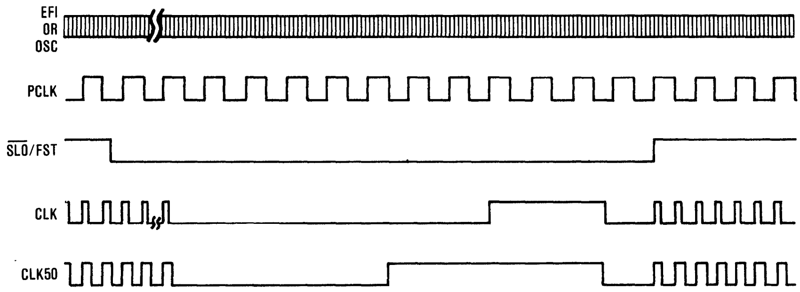


FIGURE 5. SLO/FST TIMING OVERVIEW

While the CPU and peripherals run slower and the 82C85 CLK and CLK50 outputs switch at a reduced frequency, the main 82C85 oscillator is still running at the maximum frequency (determined by the crystal or EFI input frequency). Since CMOS power is directly related to operating frequency, 82C85 power supply current will typically be reduced by 25-35%.

Clock Slow/Fast Operation

The SLO/FST input determines whether the CLK and CLK50 outputs run at full speed (crystal or EFI frequency divided by 3) or at slow speed (crystal or EFI frequency divided by 768) (See Figure 5). When in the SLOW mode, 82C85 stop-clock and stop-oscillator functions operate in the same manner as in the FAST mode.

Internal logic requires that the SLO/FST pin be held low for at least 195 oscillator or EFI clock pulses before the SLOW mode command is recognized. This requirement eliminates unwanted FAST-to-SLOW mode frequency changes which could be caused by glitches or noise spikes.

To guarantee FAST mode recognition, the SLO/FST pin must be held high for at least 3 OSC or EFI pulses. The 82C85 will begin FAST mode operation on the next PCLK edge after FAST command recognition. Proper CLK and CLK 50 phase relationships are maintained and minimum pulse width specifications are met.

FAST-to-SLOW or SLOW-to-FAST mode changes will occur on the next rising or falling edge of PCLK. It is important to remember that the transition time for operating freqeuncy changes, which are dependent upon PCLK, will vary with the 82C85 oscillator or EFI frequency.

Slow Mode Control

The 82C55A programmable peripheral interface can be used to provide control of the SLO/FST pin by connecting a port pin of the 82C55A directly to the SLO/FST pin (See Figure 1). With the port pin configured as an output, software control of the SLO/FST pin is provided by simply writing a logical one (FAST mode) or logical zero (SLOW Mode) to the corresponding port. PORT C is well-suited for this function due to it's bit set and reset capabilities.

Since PCLK continues to run at a frequency equal to the oscillator or EFI frequency divided by 6, it can be used by other devices in the system which need a fixed high frequency clock. For example, PCLK could be used to clock an 82C54 programmable interval timer to produce a real-time clock for the system or as a baud rate generator to maintain serial data communications during SLOW mode operation.

Oscillator

The oscillator circuit of the 82C85 is designed primarily for use with an external parallel resonant, fundamental mode crystal from which the basic operating frequency is derived. The crystal frequency should be selected at three times the required CPU clock. X1 and X2 are the two crystal input connections. The output of the oscillator is buffered and available at the OSC output (pin 18) for generation of other system timing signals.

For the most stable operation of the oscillator (OSC) output circuit, two capacitors (C1=C2) are recommended. Capacitors C1 and C2 are chosen such that their combined capacitance matches the load capacitance as specified by the crystal manufacturer. This insures operation within the frequency tolerance specified by the crystal manufacturer.

The crystal/capacitor configuration and the formula used to determine the capacitor values are shown in Figure 6. Crystal Specifications are shown in Table 3. For additional information on crystal operation, see Harris publication Tech Brief 47.

$$CT = \frac{C1 \cdot C2}{C1 + C2} \quad \text{(Including stray capacitance)}$$

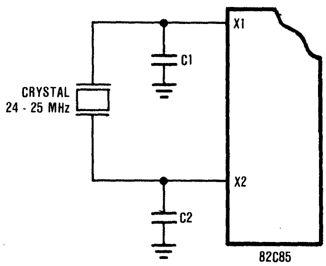


FIGURE 6. 82C85 CRYSTAL CONNECTION

TABLE 3. CRYSTAL SPECIFICATIONS

PARAMETER	TYPICAL CRYSTAL SPECIFICATION
Frequency	2.4 to 25 MHz
Type of Operation	Parallel Resonent, Fund. Mode
Load Capacitance	20 or 32 pF
R_{SERIES} (Max)	35Ω (f = 24 MHz, CL = 32 pF)
	66Ω (f = 24 MHz, CL = 20 pF)

Frequency Source Selection

The F/C̄ input is a strapping pin that selects either the crystal oscillator or the EFI input as the source frequency for clock generation. If the EFI input is selected as the source, the oscillator section (OSC output) can be used independently for another clock source. If a crystal is not used, then crystal input X1 (pin 23) must be tied to VCC or GND and X2 (pin 22) should be left open. If the EFI mode is not used, then EFI (pin 20) should be tied to VCC or GND.

Clock Generator

The clock generator consists of two synchronous divide-by-three counters with special clear inputs that inhibit the counting. One counter generates a 33% duty cycle waveform (CLK) and the other generates a 50% duty cycle waveform (CLK50). These two counters are negative-edge synchronized, with the low-going transitions of both waveforms occurring on the same oscillator transition. The CLK and CLK50 output frequencies are one-third of the base input frequency when S̄L̄Ō/FST is high and are equal to the base input frequency divided by 768 when S̄L̄Ō/FST is low.

The CLK output is a 33% duty cycle clock signal designed to drive the 80C86 and 80C88 microprocessors directly. CLK50 has a 50% duty cycle output synchronous with CLK, designed to drive coprocessors and peripherals requiring a 50% duty cycle clock. When S̄L̄Ō/FST is high, CLK and CLK50 have output frequencies which are 1/3 that of EFI/OSC. When S̄L̄Ō/FST is low, CLK and CLK50 have output frequencies which are OSC (EFI) divided by 768.

PCLK is a peripheral clock signal with an output frequency equal the oscillator or EFI frequency divided by 6. PCLK has a 50% duty cycle. PCLK is unaffected by S̄L̄Ō/FST. When the 82C85 is placed in the STOP mode, PCLK will remain in it's current state (logic high or logic low) until a RESET or START command restarts the 82C85 clock circuitry. PCLK is negative-edge synchronized with CLK and CLK50.

Clock Synchronization

The clock synchronization (CSYNC) input allows the output clocks to be synchronized with an external event (such as another 82C85 or 82C84A clock signal). CSYNC going active causes all clocks (CLK, CLK50 and PCLK) to stop in the HIGH state.

It is necessary to synchronize the CSYNC input to the EFI clock external to the 82C85. This is accomplished with two flip-flops when synchronizing two 82C85s and with three flip-flops when synchronizing an 82C85 to an 82C84A (See Figure 7). Multiple external flip-flops are necessary to minimize the occurence of metastable (or indeterminate) states.

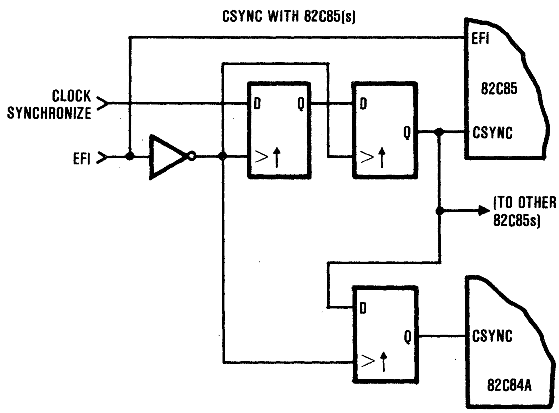


FIGURE 7. 82C85 AND 82C84A CSYNC SYNCHRONIZATION METHODS

Ready Synchronization

Two READY inputs (RDY1, RDY2) are provided to accommodate two system busses. Each READY input is qualified by ($\overline{AEN1}$ and $\overline{AEN2}$, respectively). The $\overline{AEN}$ signals validate their respective RDY signals.

Synchronization is required for all asynchronous active-going edges of either RDY input to guarantee that the RDY set up and hold times are met. Inactive-going edges of RDY in normally ready systems do not require synchronization but must satisfy RDY setup and hold as a matter of proper system design.

The $\overline{ASYNC}$ input defines two modes of READY synchronization operation. When $\overline{ASYNC}$ is LOW, two stages of synchronization are provided for active READY input signals. Positive-going asynchronous READY inputs will first be synchronized to flip-flop one at the rising edge of CLK (requiring a setup time TR1VCH) and then synchronized to flip-flop two at the next falling edge of CLK, after which time the READY output will go HIGH.

Negative-going asynchronous READY inputs will be synchronized directly to flip-flop two at the falling edge of CLK, after which time the READY output will go inactive. This mode of operation is intended for use by asynchronous (normally not ready) devices in the system which cannot be guaranteed by design to meet the required RDY setup timing (TR1VCL) on each bus cycle.

When $\overline{ASYNC}$ is high or left open, the first READY flip-flop is bypassed in the READY synchronization logic. READY inputs are synchronized by flip-flop two on the falling edge of CLK before they are presented to the processor. This mode is available for synchronous devices that can be guaranteed to meet the required RDY setup time. $\overline{ASYNC}$ can be changed on every bus cycle to select the appropriate mode of synchronization for each device in the system.

Absolute Maximum Ratings

Supply Voltage .... +8.0 Volts
Input, Output or I/O Voltage Applied .... GND -0.5V to VCC +0.5V
Storage Temperature Range .... -65°C to +150°C
Maximum Package Power Dissipation .... 1 Watt
θ_{jc} .... 26°C/W (CERDIP Package), 31°C/W (LCC Package)
θ_{ja} .... 59°C/W (CERDIP Package), 64°C/W (LCC Package)
Gate Count .... 500 Gates
Junction Temperature .... +150°C
Lead Temperature (Soldering, Ten Seconds) .... +260°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +4.5V to +5.5V
Operating Temperature Range
C82C85 .... 0°C to +70°C
I82C85 .... -40°C to +85°C
M82C85 .... -55°C to +125°C

D.C. Electrical Specifications

VCC = 5.0V 10%; TA = 0°C to +70°C (C82C85);
TA = -40°C to +85°C (I82C85);
TA = -55°C to +125°C (M82C85)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	Logical One Input Voltage	2.0 2.2		V V	C82C85, I82C85 M82C85
VIHR	Reset Input High Voltage	2.8		V	
VIL	Logical Zero Input Voltage		0.8	V	
$V_{T^+} - V_T$	Reset Input Hysteresis	0.25		V	
VOH	Logical One Output Voltage	VCC-0.4		V	IOH = -5.0 mA for CLK or CLK50 outputs IOH = -2.5 mA for all other outputs
VOL	Logical Zero Output Voltage		0.4	V	IOL = +5.0 mA for all outputs
II	Input Leakage Current	-1.0	1.0	μA	VIN = VCC or GND, Pins 11, 12, 13, 14, 15, 23
IBHH	Bus-hold High Leakage Current	-10	-200	μA	VIN = 3.0V; Pins 21, 11, 12, 13, 14, 15
ICCSB	Standby Power Supply Current		100	μA	82C85 in HALT state with oscillator stopped
ICCOP	Operating Power Supply Current		30 50	mA mA	Crystal Frequency = 15 MHz, outputs open Crystal Frequency = 25 MHz, outputs open
ICCSLOW	Slow Mode Operating Current		1.5	mA/MHz	Outputs Open; $\overline{SLO}$/FST = 0; START = 1; Other inputs - VIN = VCC or GND

Capacitance

T_A = 25°C. VCC = GND = 0V; VIN = +5V or GND

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
CIN*	Input Capacitance	5	pF	Frequency = 1MHz

* Guaranteed and sampled, but not 100% tested.

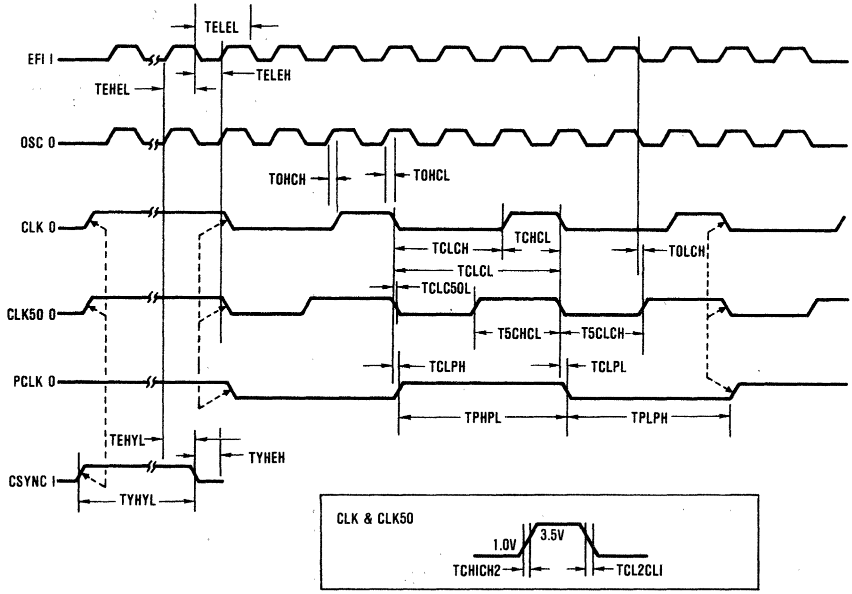
A. C. Electrical Specifications

VCC = 5V ± 10%
TA= 0°C to +70°C (C82C85); TA = -40°C to +85°C (I82C85);
TA = -55°C to +125°C (M82C85)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
TIMING REQUIREMENTS					
TEHEL	External Frequency HIGH Time	15		ns	90%-90% V_{IN}
TELEH	External Frequency LOW Time	15		ns	10%-10% V_{IN}
TELEL	EFI or crystal period	40		ns	
TEFIDC	External Frequency Input duty cycle	45	55	%	
Fx	Crystal Frequency	2.4	25	MHz	
TR1VCL	RDY1, RDY2 Active Setup to CLK	35		ns	$\overline{ASYNC}$ = HIGH
TR1VCH	RDY1, RDY2 Active Setup to CLK	35		ns	$\overline{ASYNC}$ = LOW
TR1VCL	RDY1, RDY2 Inactive Setup to CLK	35		ns	
TCLR1X	RDY1, RDY2 Hold to CLK	0		ns	
TAYVCL	$\overline{ASYNC}$ Setup to CLK	50		ns	
TCLAYX	$\overline{ASYNC}$ Hold to CLK	0		ns	
TA1VR1V	$\overline{AEN1}$, $\overline{AEN2}$ Setup to RDY1, RDY2	15		ns	
TCLA1X	$\overline{AEN1}$, $\overline{AEN2}$ Hold to CLK	0		ns	
TYHEH	CSYNC Setup to EFI	10		ns	
TEHYL	CSYNC Hold to EFI	10		ns	
TYHYL	CSYNC Pulse Width	2TELEL		ns	
TI1HCL	$\overline{RES}$ Setup to CLK	65		ns	See Note 2
TSVCH	S0, S1, $\overline{S2}$/$\overline{STOP}$ Setup to CLK	35		ns	
TCHSV	S0, S1, $\overline{S2}$/$\overline{STOP}$ Hold to CLK	35		ns	
TRSVCH	$\overline{RES}$, START Setup to CLK	65		ns	Note 2
TSHSL	$\overline{RES}$ (low) or START (high) pulse width	TCLCL/3		ns	
TSFPC	$\overline{SLO}$/FST setup to PCLK	TEHEL + 100		ns	Note 2
TSTART	$\overline{RES}$ or START valid to CLK low	2TELEL + 2		ns	
TSTOP	$\overline{STOP}$ command valid to CLK high	2TCHCH + TRSVCH	3TCHCH + 34	ns	
TIMING RESPONSES					
TCLCL	CLK/CLK50 Cycle Period	125		ns	
TCHCL	CLK HIGH Time	(1/3 TCLCL)+ 2		ns	Fig. 12 & 13
TCLCH	CLK LOW Time	(2/3 TCLCL)-15		ns	Fig. 12 & 13
T5CHCL	CLK50 HIGH Time	(1/2 TCLCL)-7.5		ns	Fig. 12 & 13
T5CLCH	CLK50 LOW Time	(1/2 TCLCL)-7.5		ns	Fig. 12 & 13
TCH1CH2	CLK/CLK50 Rise Time		8	ns	1.0V to 3.5V
TCL2CL1	CLK/CLK50 Fall Time		8	ns	1.0 to 3.5V
TPHPL	PCLK HIGH Time	TCLCL-20		ns	
TPLPH	PCLK LOW Time	TCLCL-20		ns	
TRYLCL	Ready Inactive to CLK	-8		ns	Fig. 14 & 15 See Note 4
TRYHCH	Ready Active to CLK	2/3(TCLCL)-15		ns	Fig. 14 & 15 See Note 3
TCLIL	CLK to Reset Delay		40	ns	
TCLPH	CLK to PCLK HIGH Delay		22	ns	
TCLPL	CLK to PCLK LOW Delay		22	ns	
TOHCH	OSC to CLK HIGH Delay	-5	22	ns	
TOHCL	OSC to CLK LOW Delay	2	45	ns	
TOLCH	OSC LOW to CLK 50 HIGH Delay	-5	22	ns	
TOST	Start/Reset Valid to Clock LOW		2	ms	Typ. - See Note 8
TOLOH	Output Rise Time (except CLK)		15	ns	From 0.8V to 2.0V
TOHOL	Output Fall Time (except CLK)		12	ns	From 2.0V to 0.8V
TRST	RESET output HIGH Time	16xTCLCL		ns	
TCLC50L	CLK LOW to CLK50 LOW Skew		5	ns	

Notes:

1. Output signals switch between VOH and VOL unless otherwise specified.
2. Setup and hold necessary only to guarantee recognition at next clock.
3. Applies only to T3, TW states.
4. Applies only to T2 states.
5. All timing delays are measured at 1.5 volts unless otherwise noted.
6. Input signals must switch between VIL max - 0.4 and VIH min + 0.4 volts.
7. Timing measurements made with EFI duty cycle = 50%.
8. Oscillator start-up time depends on several factors including crystal frequency, crystal manufacturer, capacitive load, temperature, power supply voltage, etc. This parameter is given for information only.



NOTE: All Timing Measurements are Made At 1.5 Volts Unless Otherwise Noted

FIGURE 8. WAVEFORMS FOR CLOCKS.

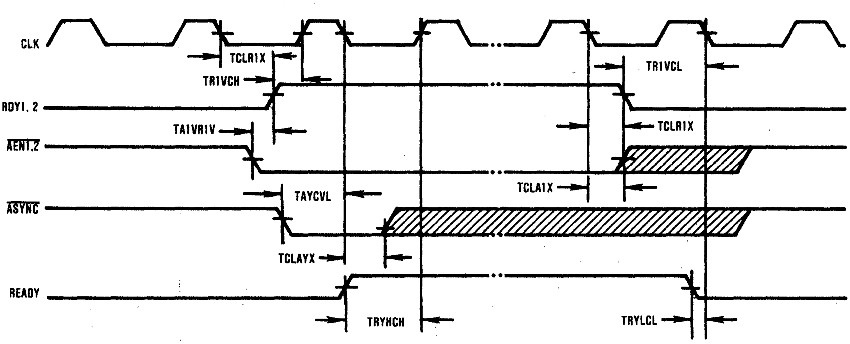


FIGURE 9. WAVEFORMS FOR READY SIGNALS (FOR ASYNCHRONOUS DEVICES)

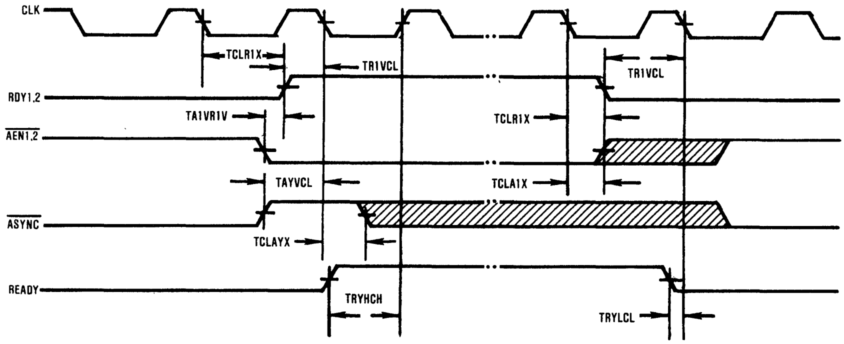


FIGURE 10. WAVEFORMS FOR READY SIGNALS (FOR SYNCHRONOUS DEVICES)

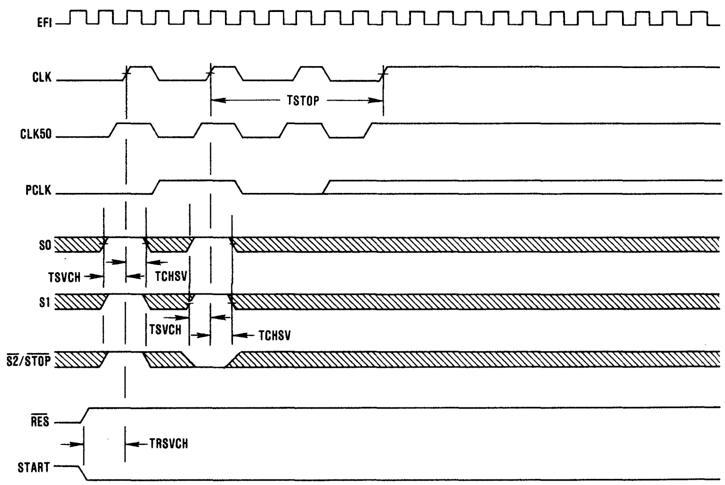


FIGURE 11. CLOCK STOP (F/$\overline{C}$ HIGH OR F/$\overline{C}$ LOW)

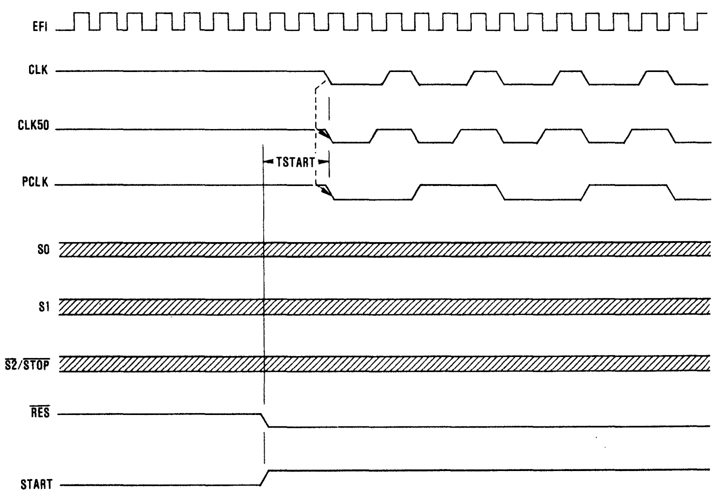


FIGURE 12. CLOCKS START (F/$\overline{C}$ HIGH)

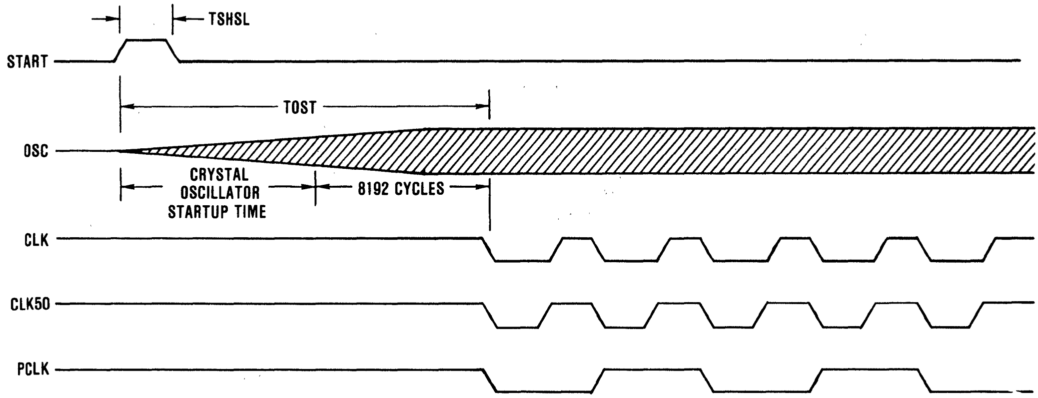


FIGURE 13. CLOCK START (F/C̄ LOW)

* NOTE: Start up count begins when the crystal oscillator reaches a suitable threshold level.

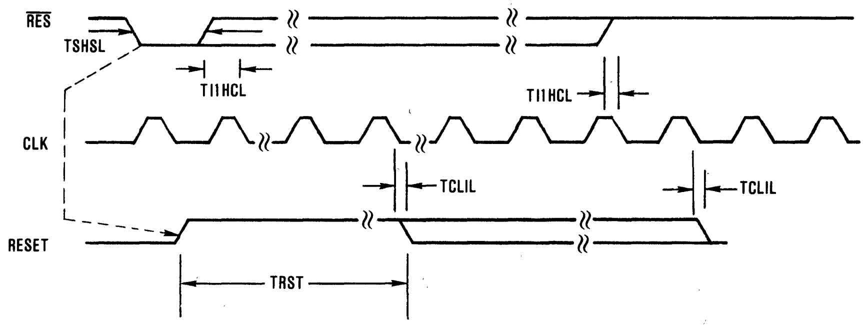


FIGURE 14. RESET TIMING (CLK RUNNING WITH F/C̄ LOW - OSC MODE) (CLK RUNNING-OR STOPPED WITH F/C̄ HIGH EFI MODE)

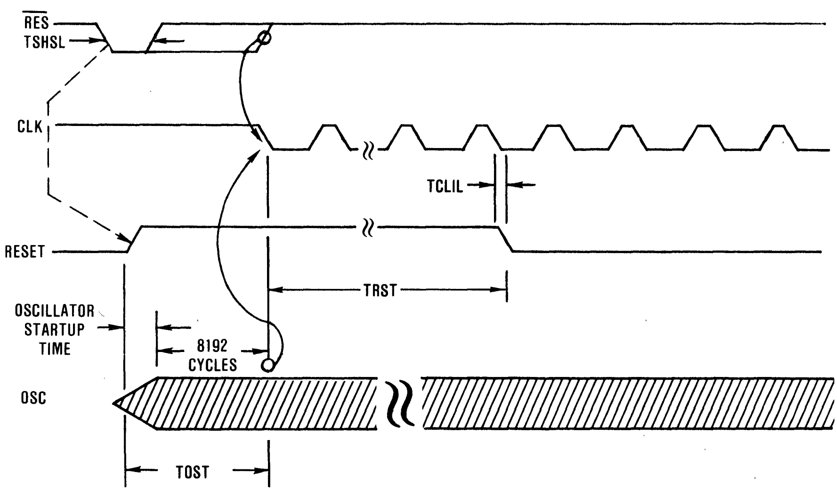
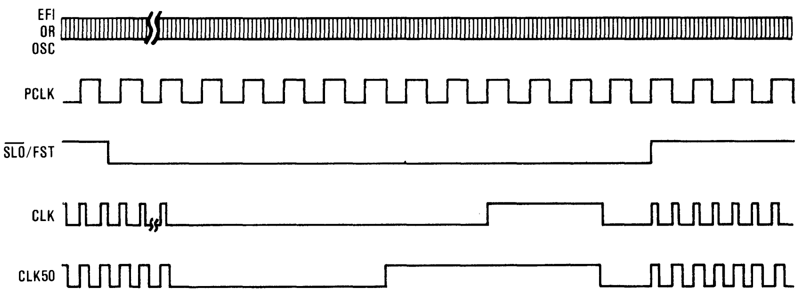


FIGURE 15. RESET TIMING OSCILLATOR STOPPED, F/C̄ LOW)

Note 1: CLK, CLK50, PCLK Remain in the High State until RES goes high and 8192 valid oscillator cycles have been registered by the 82C85 internal counter (TOST time period). After RES goes high and CLK, CLK50, POLY become active, the RESET output will remain high for a minimum of 16 CLK Cycles (TRST).



See Figure 16B for Detailed Timing
See Figure 16C for Detailed Timing

FIGURE 16A. $\overline{SLO}$/FST TIMING OVERVIEW.

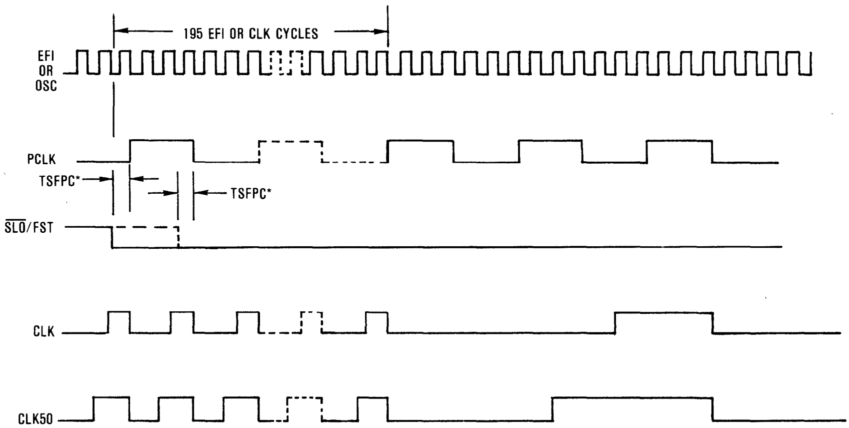
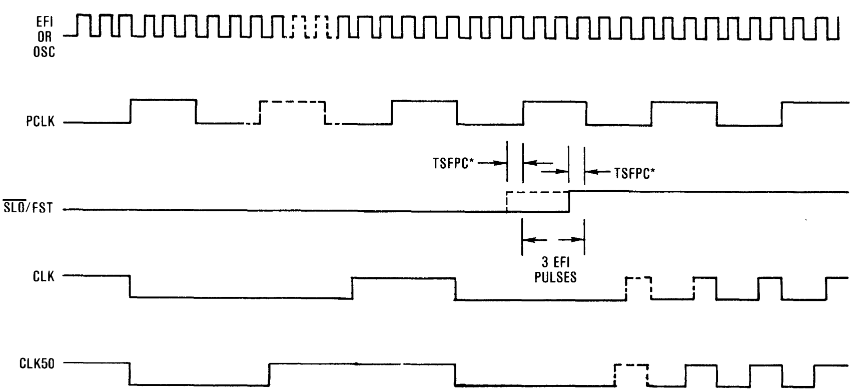


FIGURE 16B. FAST TO SLOW CLOCK MODE TRANSITION.



* If TSFPC is not met on one edge of PLCK, $\overline{SLO}$/FST will be recognized on the next edge of PCLK.

FIGURE 16C. SLOW TO FAST CLOCK MODE TRANSITION.

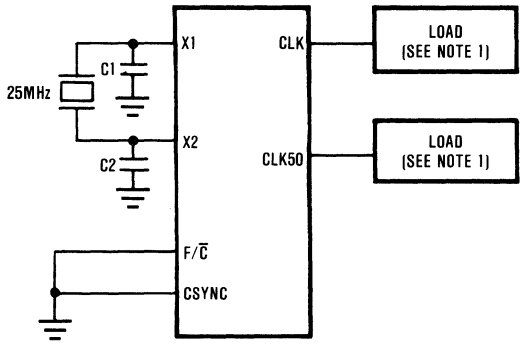


FIGURE 17. CLOCK HIGH AND LOW TIME (USING X1, X2)

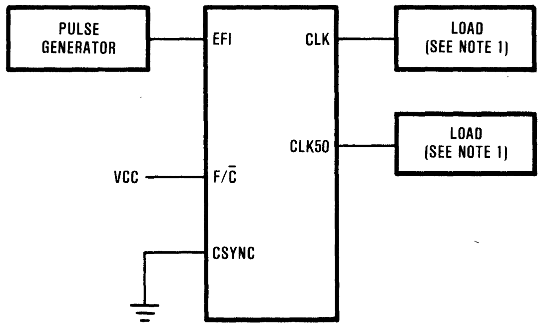


FIGURE 18. CLOCK HIGH AND LOW TIME (USING EFI)

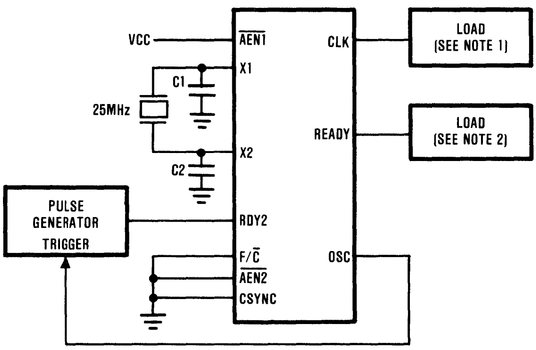


FIGURE 19. READY TO CLOCK (USING X1,X2)

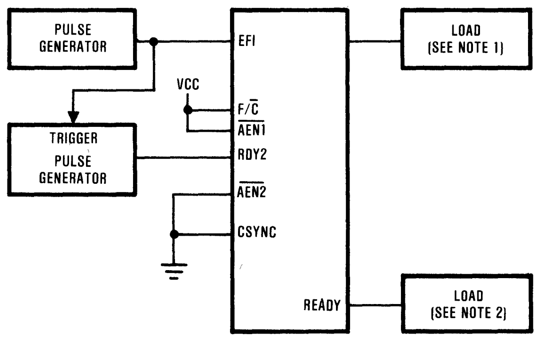
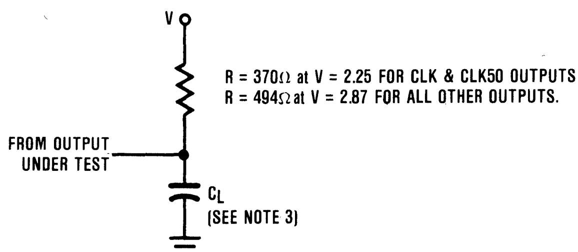


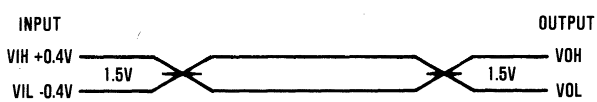
FIGURE 20. READY TO CLOCK (USING EFI)



NOTES:
1. C_L = 100 pF
2. C_L = 30 pF
3. C_L Includes probe and jig capacitance

FIGURE 21. TEST LOAD MEASUREMENT CONDITIONS.

A.C. Testing Input, Output Waveform



A.C. TESTING: All A.C. parameters tested as per Test Circuits. Input rise and fall times are driven at 1ns/V.

HARRIS

82C86H/87H

CMOS Octal Bus Transceivers

Features

- Full Eight-Bit Bi-directional Bus Interface
- Industry Standard 8286/8287 Compatible Pinout
- "H" Designates High Drive CMOS Bus Transceiver
  - B Side: 20mA
  - A Side: 12mA
- Three-State Outputs
- Gated Inputs
  - Reduce Operating current
  - Eliminate Pull-Up/Down Resistors
- Propagation Delay
  - 82C86H .... 32ns Max.
  - 82C87H .... 30ns Max.
- A.C. Specifications Guaranteed at Rated C_L
  - B Side .... C_L = 300pF
  - A Side .... C_L = 100pF
- Single 5V Power Supply
- Power Supply Current .... 10μA Max. Standby
- Wide Operating Temperature Ranges:
  - C82C86H/C82C87H .... 0°C to +70°C
  - I82C86H/I82C87H .... -40°C to +85°C
  - M82C86H/M82C87H .... -55°C to +125°C

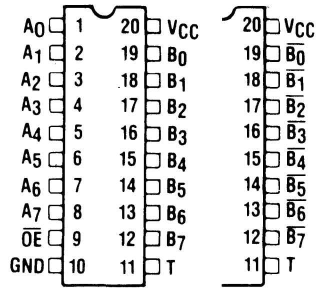
Description

The 82C86H/82C87H are octal bus transceivers manufactured using a self-aligned silicon gate CMOS process (SAJI IV). These circuits provide a full eight-bit bi-directional bus interface in a 20-pin package. The Transmit (T) control determines the data direction. The active low enable (OE) allows simple interface to the 80C86, 80C88 and other microprocessors. The outputs of the 82C86H are non-inverting while the 82C87H outputs are inverting. The 82C86H and 82C87H have gated inputs, eliminating the need for pull-up/down resistors and reducing overall system operating power dissipation.

Pinouts

TOP VIEW

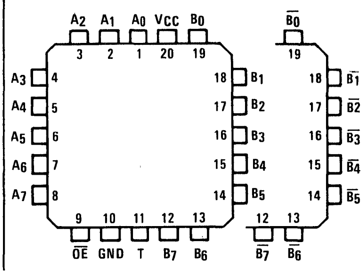
82C86H 82C87H



LCC/PLCC

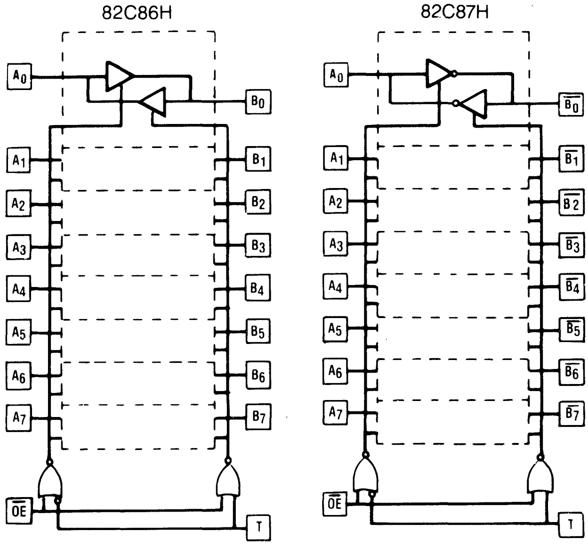
TOP VIEW

82C86H 82C87H



Functional Diagram

82C86H 82C87H



PIN NAMES

A_0–A_7	Local Bus Data I/O Pins
$\overline{B_0}$–$\overline{B_7}$ B_0–B_7	System Bus Data I/O Pins
T	Transmit Control Input
$\overline{OE}$	Active Low Output Enable

Truth Table

T	$\overline{OE}$	A	B
X	H	Hi-Z	Hi-Z
H	L	I	O
L	L	O	I

H = Logic One
L = Logic Zero
I = Input Mode
O = Output Mode
X = Don't Care
Hi-Z = High Impedance

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage .... +8.0 Volts
Input, Output or I/O Voltage Applied .... GND -0.5V to VCC +0.5V
Storage Temperature Range .... -65°C to +150°C
Maximum Package Power Dissipation .... 1 Watt
θ_{jc} .... 18°C/W (CERDIP Package), 23°C/W (LCC Package)
θ_{ja} .... 73°C/W (CERDIP Package), 78°C/W (LCC Package)
Gate Count .... 265 Gates
Junction Temperature .... +150°C
Lead Temperature (Soldering, Ten Seconds) .... +260°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +4.5V to +5.5V
Operatiing Temperature Range
C82C86H/C82C87H .... 0°C to +70°C
I82C86H/I82C87H .... -40°C to +85°C
M82C86H/M82C87H .... -55°C to +125°C

D.C. Electrical Specifications

VCC = 5.0V ± 10%; T_A = 0°C to +70°C (C82C86H/C82C87H);
T_A = -40°C to +85°C (I82C86H/I82C87H);
T_A = -55°C to +125°C (M82C86H/M82C87H);

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	Logical One Input Voltage	2.0 2.2		V	C82C86H/C82C87H, I82C86H/I82C87H M82C86H/M82C87H (See Note 1)
VIL	Logical Zero Input Voltage		0.8	V	
VOH	Logical One Output Voltage B Outputs A Outputs A or B Outputs	 3.0 3.0 VCC -0.4		 V V V	 IOH = -8mA IOH = -4mA IOH = -100μA
VOL	Logical Zero Output Voltage B Outputs A Outputs		 0.45 0.45	 V V	 IOL = 20mA IOL = 12mA
II	Input Leakage Current	-10	10	μA	VIN = GND or VCC DIP Pins 9, 11
IO	Output Leakage Current	-10	10	μA	VO = GND or VCC OE ≥ VCC - 0.5V DIP Pins 1-8, 12-19
ICCSB	Standby Power Supply Current		10	μA	VIN = VCC or GND VCC = 5.5V Outputs Open
ICCOP	Operating Power Supply Current		1	mA/MHz	T_A = +25°C, VCC = 5V, Typical (See Note 2).

NOTES: 1. VIH is measured by applying a pulse of magnitude = VIH min to one data input at a time and checking the corresponding device output for a valid logical one during valid input high time. Control pins (T, $\overline{OE}$) are tested separately with all device data input pins at VCC -0.4V.
2. Typical ICCOP = 1mA/MHz of read/write cycle time. (Example: 1.0μs read/write cycle time = 1mA).

Capacitance

T_A = 25°C; VCC = GND = 0V; VIN = +5V or GND

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
CIN	Input Capacitance B Inputs A Inputs	 17 12	 pF pF	F = 1MHz T_A = 25°C VIN or VOUT = VCC or GND

A.C. Electrical Specifications

VCC = 5.0V ± 10%; T_A = 0°C to +70°C (C82C86H/C82C87H), (C82C86H-5/C82C87H-5);
T_A - FREQ · 1MHz T_A = -40°C to +85°C (I82C86H/I82C87H), (I82C86H-5/I82C87H-5);
T_A = -55°C to +125°C (M82C86H-5/M82C87H-5)

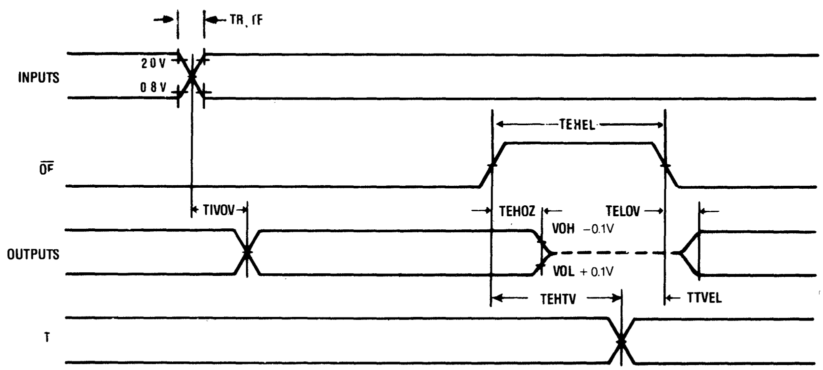
SYMBOL	PARAMETER	MIN	MAX [4] 82C86H/87H	MAX [4] 82C86H/87H-5	UNITS	TEST CONDITIONS
TIVOV	Input to Output Delay					See Notes 1,2
	Inverting	5	30	35	ns	
	Non-Inverting	5	32	35	ns	
TEHTV	Transmit-Receive Hold Time	5			ns	See Notes 1,2
TTVEL	Transmit/Receive Setup Time	10			ns	See Notes 1,2
TEHOZ	Output Disable Time	5	30	35	ns	See Notes 1,2
TELOV	Output Enable Time	10	50	65	ns	See Notes 1,2
TR, TF	Input Rise/Fall Times		20	20	ns	See Notes 1,2
TEHEL	Minimum Output Enable High Time				ns	See Note 3
	82C86H/87H	30				
	82C86H/87H-5	35				

NOTE 1: All A.C. Parameters tested as per test circuits and definitions in Figures 1-5. Input rise and fall times are driven at 1 ns/V.

NOTE 2: Input test signals must switch between VIL − 0.4V and VIH + 0.4V.

NOTE 3: A system limitation only when changing direction. Not a measured parameter.

NOTE 4: 82C86H and 82C87H are available in commercial and industrial temperature ranges only. 82C86H-5 and 82C87H-5 are available in commercial, industrial and military temperature ranges.



All timing measurements are made at 1.5V unless otherwise noted.

Figure 1
82C86H/82C87H Timing Relationships

A.C. Test Circuit

A SIDE OUTPUT

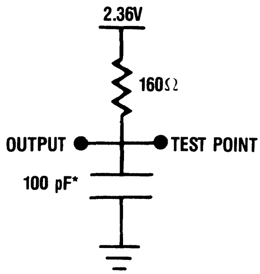


Figure 2a
Switching
Load Circuit

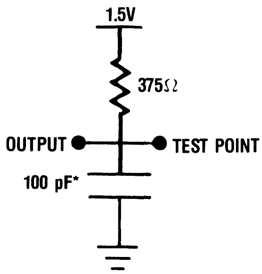


Figure 3a
TELOV
Output High Enable
Load Circuit

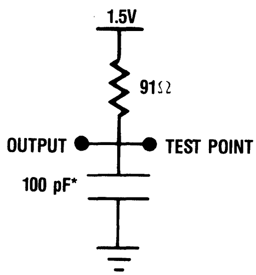


Figure 4a
TELOV
Output Low Enable
Load Circuit

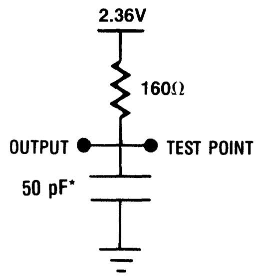


Figure 5a
TEHOZ
Output Low/High Disable
Load Circuit

B SIDE OUTPUT

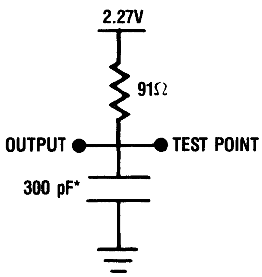


Figure 2b
Switching
Load Circuit

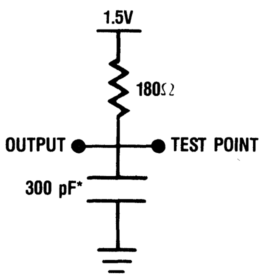


Figure 3b
TELOV
Output High Enable
Load Circuit

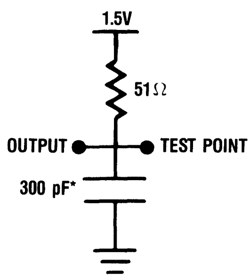


Figure 4b
TELOV
Output Low Enable
Load Circuit

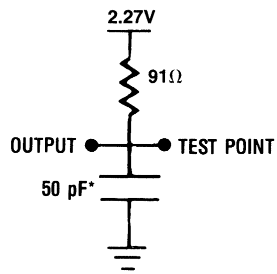


Figure 5b
TEHOZ
Output Low/High Disable
Load Circuit

*Includes jig and stray capacitance.

Decoupling Capacitors

The transient current required to charge and discharge the 300 pF load capacitance specified in the 82C86H/87H data sheet is determined by

$$I = C_L\,(dv/dt)$$

Assuming that all outputs change state at the same time and that dv/dt is constant;

$$I = C_L \frac{(VCC \times 80\%)}{t_R/t_F}$$

where t_R = 20 ns, VCC = 5.0volts, C_L = 300 pF on each of eight outputs.

$$I = (8 \times 300 \times 10^{-12}) \times (5.0V \times 0.8)/(20 \times 10^{-9})$$

$$= 480\ mA$$

This current spike may cause a large negative voltage spike on V_{CC}, which could cause improper operation of the device. To filter out this noise, it is recommended that a 0.1 μF ceramic disc capacitor be placed between V_{CC} and GND at each device, with placement being as near to the device as possible.

GATED INPUTS

During normal system operation of a latch, signals on the bus at the device inputs will become high impedance or make transitions unrelated to the operation of the latch. These unrelated input transitions switch the input circuitry and typically cause an increase in power dissipation in CMOS devices by creating a low resistance path between V_{CC} and GND when the signal is at or near the input switching threshold. Additionally, if the driving signal becomes high impedance ("float" condition), it could create and indeterminate logic state at the inputs and cause a disruption in device operation.

The Harris 82C8X series of bus drivers eliminates these conditions by turning off data inputs when data is latched (STB = logic zero for the 82C82/83H) and when the device is disabled(OE = logic one for the 82C86H/87H). These gated inputs disconnect the input circuitry from the V_{CC} and ground power supply pins by turning off the upper P-channel and lower N-channel (see Figure 6a, 6b). No current flow from V_{CC} to GND occurs during input transitions and invalid logic states from floating inputs are not transmitted. The next stage is held to a valid logic level internal to the device.

D.C. input voltage levels can also cause an increase in I_{CC} if these input levels approach the minimum V_{IH} or maximum V_{IL} conditions. This is due to the operation of the input circuitry in its linear operating region (partially conducting state). The 82C8X series gated inputs mean that this condition will occur only during the time the device is in the transparent mode (STB = logic one). I_{CC} remains below the maximum I_{CC} standby specification of 10 μA during the time inputs are disabled, thereby greatly reducing the average power dissipation of the 82C8X series devices.

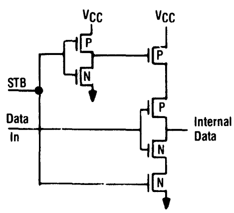


Figure 6a
82C82/83H

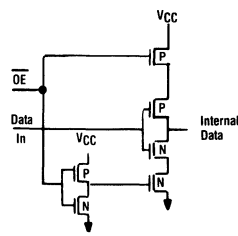


Figure 6b
82C86H/87H Gated Inputs

HARRIS

82C88

CMOS Bus Controller

Features

- Compatible with Bipolar 8288
- Performance Compatible with:
  - 80C86/80C88 (5/8 MHz)
  - 80186/80188 (6/8 MHz)
  - 8086/8088 (5/8 MHz)
  - 8089
- Provides Advanced Commands for Multi-Master Busses
- Three-State Command Outputs
- Bipolar Drive Capability
- Fully TTL Compatible
- Scaled SAJI IV CMOS Process
- Single 5V Power Supply
- Low Power Operation
  - ICCSB .... $10\mu A$
  - ICCOP 1mA/MHz
- Wide Operating Temperature Ranges:
  - C82C88 .... 0°C to +70°C
  - I82C88 .... -40°C to +85°C
  - M82C88 .... -55°C to +125°C

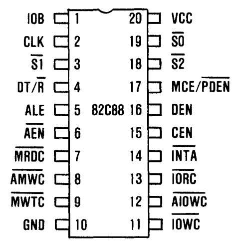
Description

The Harris 82C88 is a high performance CMOS Bus Controller manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). The 82C88 provides the control and command timing signals for 80C86, 80C88, 8086, 8088, 8089, 80186, and 80188 based systems. The high output drive capability of the 82C88 eliminates the need for additional bus drivers.

Static CMOS circuit design insures low operating power. The Harris advanced SAJI process results in performance equal to or greater than existing equivalent products at a significant power savings.

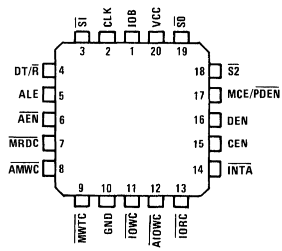
Pinouts

TOP VIEW

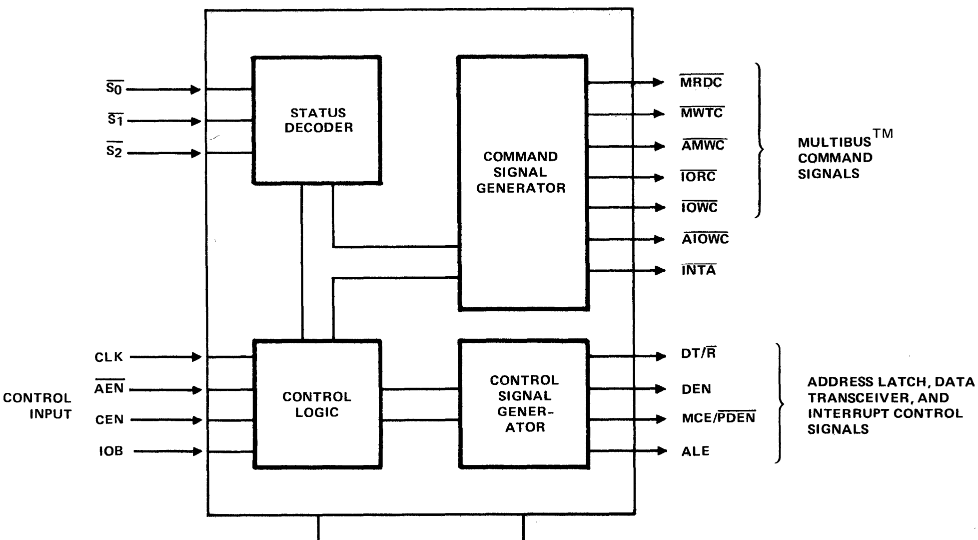


LCC/PLCC

TOP VIEW



Functional Diagram



™Multibus is an INTEL Corporation trademark

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Pin Description

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
V_{CC}	20		VCC: The +5V power supply pin. A 0.1μF capacitor between pins 10 and 20 is recommended for decoupling.
GND	10		GROUND.
$\overline{S_0}$, $\overline{S_1}$ $\overline{S_2}$	19, 3 18	I	STATUS INPUT PINS: These pins are the input pins from the 80C86, 8086/88/8089 processors. The 82C88 decodes these inputs to generate command and control signals at the appropriate time. When Status pins are not in use (passive), command outputs are held HIGH (See Table 1.)
CLK	2	I	CLOCK: This is a CMOS compatible input which receives a clock signal from the 82C84A or 82C85 clock generator and serves to establish when command/control signals are generated.
ALE	5	O	ADDRESS LATCH ENABLE: This signal serves to strobe an address into the address latches. This signal is active HIGH and latching occurs on the falling (HIGH to LOW) transition. ALE is intended for use with transparent D type latches, such as the 82C82/82C83H.
DEN	16	O	DATA ENABLE: This signal serves to enable data transceivers onto either the local or system data bus. This signal is active HIGH.
DT/$\overline{R}$	4	O	DATA TRANSMIT/RECEIVE: This signal establishes the direction of data flow through the transceivers. A HIGH on this line indicates Transmit (write to I/O or memory) and a LOW indicates Receive (read from I/O memory).
$\overline{AEN}$	6	I	ADDRESS ENABLE: $\overline{AEN}$ enables command outputs of the 82C88 Bus Controller a minimum of 110ns (250ns maximum) after it becomes active (LOW). $\overline{AEN}$ going inactive immediately three-states the command output drivers. $\overline{AEN}$ does not affect the I/O command lines if the 82C88 is in the I/O Bus mode (IOB tied HIGH).
CEN	15	I	COMMAND ENABLE: When this signal is LOW all 82C88 command outputs and the DEN and $\overline{PDEN}$ control outputs are forced to their Inactive state. When this signal is HIGH, these same outputs are enabled.
IOB	1	I	INPUT/OUTPUT BUS MODE: When the IOB is strapped HIGH the 82C88 functions in the I/O Bus mode. When it is strapped LOW, the 82C88 functions in the System Bus mode (See I/O Bus and System Bus sections).
$\overline{AIOWC}$	12	O	ADVANCED I/O WRITE COMMAND: The $\overline{AIOWC}$ issues an I/O Write Command earlier in the machine cycle to give I/O devices an early indication of a write instruction. Its timing is the same as a read command signal. $\overline{AIOWC}$ is active LOW.
$\overline{IOWC}$	11	O	I/O WRITE COMMAND: This command line instructs an I/O device to read the data on the data bus. The signal is active LOW.
$\overline{IORC}$	13	O	I/O READ COMMAND: This command line instructs an I/O device to drive its data onto the data bus. This signal is active LOW.
$\overline{AMWC}$	8	O	ADVANCED MEMORY WRITE COMMAND: The $\overline{AMWC}$ issues a memory write command earlier in the machine cycle to give memory devices an early indication of a write instruction. Its timing is the same as a read command signal. $\overline{AMWC}$ is active LOW.
$\overline{MWTC}$	9	O	MEMORY WRITE COMMAND: This command line instructs the memory to record the data present on the data bus. This signal is active LOW.
$\overline{MRDC}$	7	O	MEMORY READ COMMAND: This command line instructs the memory to drive its data onto the data bus. $\overline{MRDC}$ is active LOW.
$\overline{INTA}$	14	O	INTERRUPT ACKNOWLEDGE: This command line tells an interrupting device that its interrupt has been acknowledged and that it should drive vectoring information onto the data bus. This signal is active LOW.
MCE/$\overline{PDEN}$	17	O	This is a dual function pin. MCE (IOB IS TIED LOW) Master Cascade Enable occurs during an interrupt sequence and serves to read a Cascade Address from a master 82C59A Priority Interrupt Controller onto the data bus. The MCE signal is active HIGH. $\overline{PDEN}$ (IOB IS TIED HIGH): Peripheral Data Enable enables the data bus transceiver for the I/O bus that DEN performs for the system bus. $\overline{PDEN}$ is active LOW.

Functional Description

Command and Control Logic

The command logic decodes the three 80C86,8086,80C88, 8088,80186,80188 or 8089 status lines ($\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$,) to determine what command is to be issued (see Table 1).

Table 1. Command Decode Definition

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	Processor State	82C88 Command
0	0	0	Interrupt Acknowledge	$\overline{INTA}$
0	0	1	Read I/O Port	$\overline{IORC}$
0	1	0	Write I/O Port	$\overline{IOWC}$, $\overline{AIOWC}$
0	1	1	Halt	None
1	0	0	Code Access	$\overline{MRDC}$
1	0	1	Read Memory	$\overline{MRDC}$
1	1	0	Write Memory	$\overline{MWTC}$, $\overline{AMWC}$
1	1	1	Passive	None

I/O Bus Mode

The 82C88 is in the I/O Bus mode if the IOB pin is strapped HIGH. In the I/O Bus mode, all I/O command lines $\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{INTA}$) are always enabled (i.e., not dependent on $\overline{AEN}$). When an I/O command is initiated by the processor, the 82C88 immediately activates the command lines using $\overline{PDEN}$ and DT/$\overline{R}$ to control the I/O bus transceiver. The I/O command lines should not be used to control the system bus in this configuration because no arbitration is present. This mode allows one 82C88 Bus Controller to handle two external busses. No waiting is involved when the CPU wants to gain access to the I/O bus. Normal memory access requires a "Bus Ready" signal ($\overline{AEN}$ LOW) before it will proceed. It is advantageous to use the IOB mode if I/O or peripherals dedicated to one processor exist in a multi-processor system.

System Bus Mode

The 82C88 is in the System Bus mode if the IOB pin is strapped LOW. In this mode, no command is issued until a specified time period after the $\overline{AEN}$ line is activated (LOW). This mode assumes bus arbitration logic will inform the bus controller (on the $\overline{AEN}$ line) when the bus is free for use. Both memory and I/O commands wait for bus arbitration. This mode is used when only one bus exists. Here, both I/O and memory are shared by more than one processor.

Command Outputs

The advanced write commands are made available to initiate write procedures early in the machine cycle. This signal can be used to prevent the processor from entering an unnecessary wait state.

The command outputs are:

$\overline{MRDC}$ - Memory Read Command
$\overline{MWTC}$ - Memory Write Command
$\overline{IORC}$ - I/O Read Command
$\overline{IOWC}$ - I/O Write Command
$\overline{AMWC}$ - Advanced Memory Write Command
$\overline{AIOWC}$ - Advanced I/O Write Command
$\overline{INTA}$ - Interrupt Acknowledge

$\overline{INTA}$ (Interrupt Acknowledge) acts as an I/O read during an interrupt cycle. Its purpose is to inform an interrupting device that its interrupt is being acknowledged and that it should place vectoring information onto the data bus.

Control Outputs

The control outputs of the 82C88 are Data Enable (DEN), Data Transmit/Receive (DT/$\overline{R}$) and Master Cascade Enable/Peripheral Data Enable (MCE/$\overline{PDEN}$). The DEN signal determines when the external bus should be enabled onto the local bus and the DT/$\overline{R}$ determines the direction of data transfer. These two signals usually go to the chip select and direction pins of a transceiver.

The MCE/$\overline{PDEN}$ pin changes function with the two modes of the 82C88. When the 82C88 is in the IOB mode (IOB HIGH), the $\overline{PDEN}$ signal serves as a dedicated data enable signal for the I/O or Peripheral System bus.

Interrupt Acknowledge and MCE

The MCE signal is used during an interrupt acknowledge cycle if the 82C88 is in the System Bus mode (IOB LOW). During any interrupt sequence, there are two interrupt acknowledge cycles that occur back to back. During the first interrupt cycle no data or address transfers take place. Logic should be provided to mask off MCE during this cycle. Just before the second cycle begins the MCE signal gates a master Priority Interrupt Controller's (PIC) cascade address onto the processor's local bus where ALE (Address Latch Enable) strobes it into the address latches. On the leading edge of the second interrupt cycle, the addressed slave PIC gates an interrupt vector onto the system data bus where it is read by the processor.

If the system contains only one PIC, the MCE signal is not used. In this case, the second Interrupt Acknowledge signal gates the interrupt vector onto the processor bus.

Address Latch Enable and Halt

Address Latch Enable (ALE) occurs during each machine cucle and serves to strobe the current address into the 82C82/82C83H address latches. ALE also serves to strobe the status ($\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$,) into a latch for halt state decoding.

Command Enable

The Command Enable (CEN) input acts as a command qualifier for the 82C88. If the CEN pin is high, the 82C88 functions normally. If the CEN pin is pulled LOW, all command lines are held in their inactive state (not 3-state). This feature can be used to implement memory partitioning and to eliminate address conflicts between system bus devices and resident bus devices.

Absolute Maximum Ratings

Supply Voltage	+8.0 Volts
Input, Output or I/O Voltage Applied	GND -0.5V to VCC +0.5V
Storage Temperature Range	-65^oC to $+150^oC$
Maximum Package Power Dissipation	1 Watt
θ_{jc}	$26^oC/W$ (CERDIP package), $31^oC/W$ (LCC package)
θ_{ja}	$76^oC/W$ (CERDIP package), $81^oC/W$ (LCC package)
Gate Count	100 Gates
Junction Temperature	$+150^oC$
Lead Temperature (Soldering, Ten Seconds)	$+260^oC$

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied.

Operating Conditions

Operating Voltage Range	+4.5V to +5.5V
Operating Temperature Range	
C82C88	0^oC to $+70^oC$
I82C88	-40^oC to $+85^oC$
M82C88	-55^oC to $+125^oC$

D.C. Electrical Specifications

VCC = 5.0V ± 10%; $T_A = 0^oC$ to $+70^oC$ (C82C88); $T_A = -40^oC$ to $+85^oC$ (I82C88); $T_A = -55^oC$ to $+125^oC$ (M82C88)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	Logical One Input Voltage	2.0 2.2		V V	C82C88,I82C88 M82C88
VIL	Logical Zero Input Voltage		0.8	V	
VIHC	CLK Logical One Input Voltage	0.7 VCC		V	
VILC	CLK Logical Zero Input Voltage		0.2 VCC	V	
VOH	Output High Voltage Command Outputs	3.0 VCC -0.4		V V	IOH = -8.0mA IOH = -2.5mA
	Output High Voltage Control Outputs	3.0 VCC -0.4		V V	IOH = -4.0mA IOH = -2.5mA
VOL	Output Low Voltage Command Outputs		0.5	V	IOL = +20.0mA
	Output Low Voltage Control Outputs		0.4	V	IOL = +8.0mA
II	Input Leakage Current	-1.0	1.0	μA	VIN = GND or VCC except $\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$, DIP Pins 1-2, 6, 15
IBHH	Input Leakage Current-Status Bus	-50	-300	μA	VIN = 2.0V $\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$ (See Note 1)
IO	Output Leakage Current	-10.0	10.0	μA	VO = GND or VCC DIP Pins 7-9, 11-14
ICCSB	Standby Power Supply		10	μA	VCC = 5.5V VIN = VCC or GND Outputs Open
ICCOP	Operating Power Supply Current		1	mA/MHz	VCC = 5.5V Outputs Open (See Note 2)

NOTES: 1: IBHH should be measured after raising the VIN on $\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$ to VCC and then lowering to 2.0V.
2: ICCOP = 1mA/MHz of CLK cycle time (TCLCL)

Capacitance

$T_A = 25^oC$; VCC = GND = 0V; VIN = +5V or GND

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_{IN}	Input Capacitance	5	pF	FREQ = 1MHz Unmeasured pins returned to GND
C_{OUT}	Output Capacitance	15	pF	

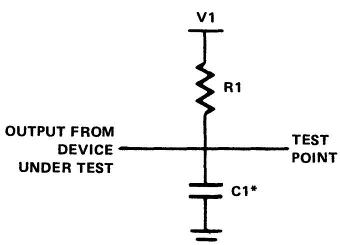
A.C. Electrical Specifications

VCC = +5V ±10%, GND = 0V: TA = 0°C to 70°C (C82C88)
TA = -40°C to +85°C (I82C88)
TA = -55°C to +125°C (M82C88)

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
TIMING REQUIREMENTS					
TCLCL	CLK Cycle Period	125		ns	
TCLCH	CLK Low Time	55		ns	
TCHCL	CLK High Time	40		ns	
TSVCH	Status Active Setup Time	35		ns	
TCHSV	Status Active Hold Time	10		ns	
TSHCL	Status Inactive Setup Time	35		ns	
TCLSH	Status Inactive Hold Time	10		ns	
TIMING RESPONSES					
TCVNV	Control Active Delay	5	45	ns	1
TCVNX	Control Inactive Delay	10	45	ns	1
TCLLH	ALE Active Delay (from CLK)		20	ns	1
TCLMCH	MCE Active Delay (from CLK)		25	ns	1
TSVLH	ALE Active Delay (from Status)		20	ns	1
TSVMCH	MCE Active Delay (from Status)		30	ns	1
TCHLL	ALE Inactive Delay	4	18	ns	1
TCLML	Command Active Dalay	5	35	ns	2
TCLMH	Command Inactive Delay	5	35	ns	2
TCHDTL	Direction Control Active Delay		50	ns	1
TCHDTH	Direction Control Inactive Delay		30	ns	1
TAELCH	Command Enable Time[1]		40	ns	3
TAEHCZ	Command Disable Time[2]		40	ns	4
TAELCV	Enable Delay Time	110	250	ns	2
TAEVNV	$\overline{AEN}$ to DEN		25	ns	1
TCEVNV	CEN to DEN, $\overline{PDEN}$		25	ns	1
TCELRH	CEN to Command		TCLML +10	ns	2
TLHLL	ALE High Time	TCLCH -10		ns	1

Note 1: TAELCH measurement is between 1.5V and 2.5V.
Note 2: TAEHCZ measured at 0.5V change in VO.

A.C. Test Circuit

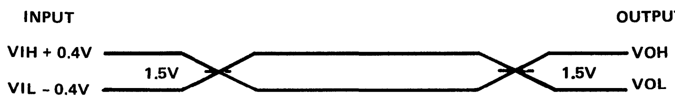


*Includes stray and jig capacitance

TEST CONDITION	IOH	IOL	V1	R1	C1
1	-4.0mA	+8.0mA	2.13V	220Ω	80pf
2	-8.0mA	+20.0mA	2.29V	91Ω	300pf
3	-8.0mA	—	1.5V	187Ω	300pf
4	-8.0mA	—	1.5V	187Ω	50pf

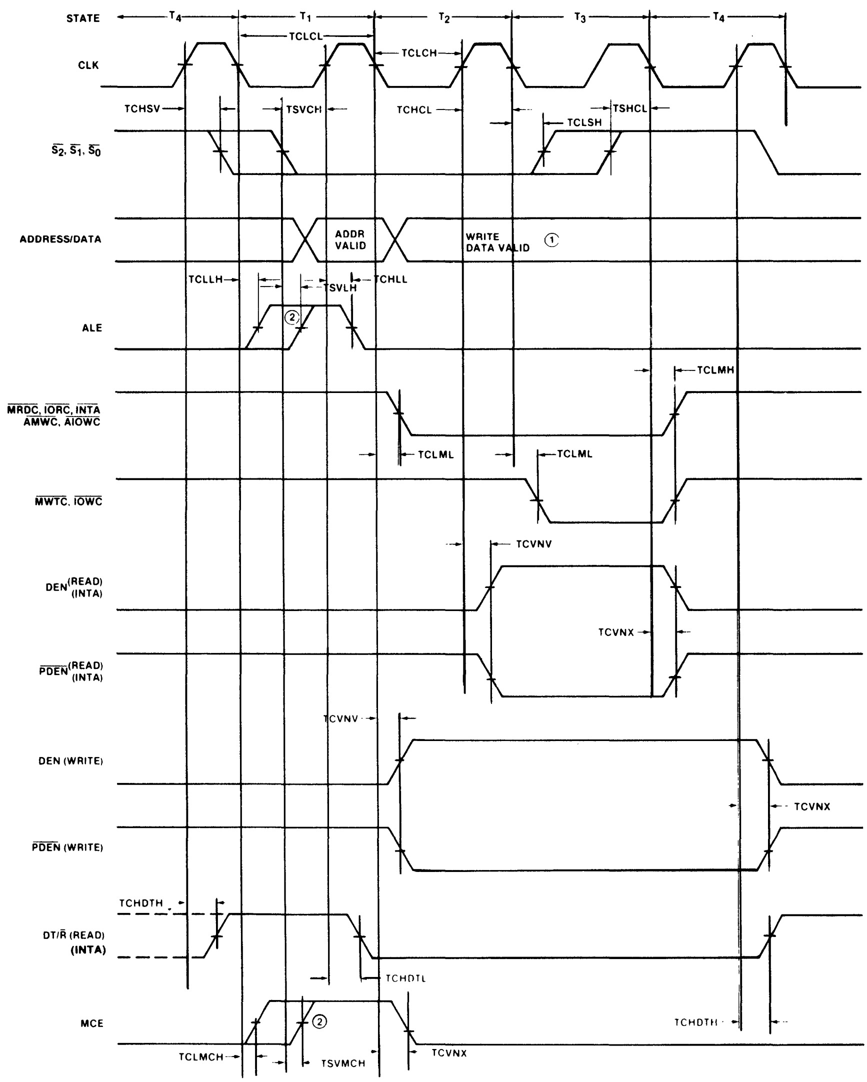
TEST CONDITION DEFINITION TABLE

A.C. Testing Input, Output Waveforms



A.C. Testing: All input signals (other than CLK) must switch between VIL -0.4V and VIH +0.4V. CLK must switch between 0.4V and 3.9V. Input rise and fall times are driven at 1ns/V.

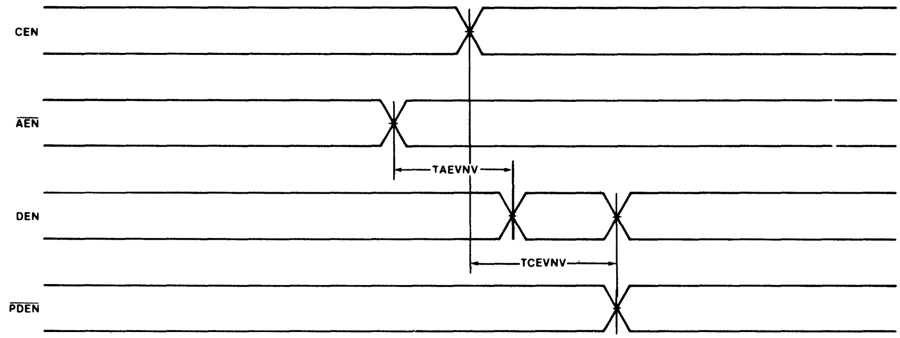
Waveforms



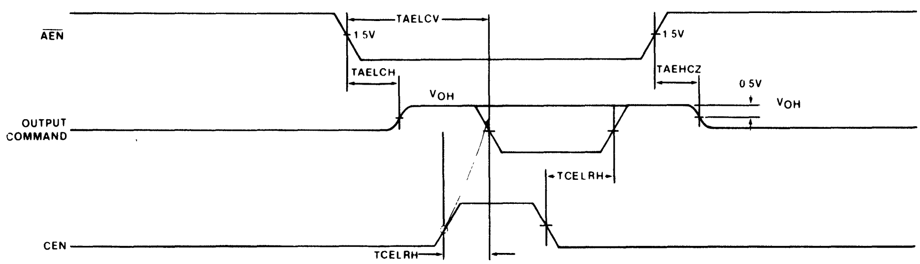
NOTES:
1 ADDRESS/DATA BUS IS SHOWN ONLY FOR REFERENCE PURPOSES
2 LEADING EDGE OF ALE AND MCE IS DETERMINED BY THE FALLING EDGE OF CLK OR STATUS GOING ACTIVE WHICHEVER OCCURS LAST
3 ALL TIMING MEASUREMENTS ARE MADE AT 1.5V UNLESS SPECIFIED OTHERWISE

Waveforms

DEN, $\overline{PDEN}$ QUALIFICATION TIMING



ADDRESS ENABLE ($\overline{AEN}$) TIMING (3-STATE ENABLE/DISABLE)



NOTE: CEN must be low or valid prior to T2 to prevent the command from being generated.

CMOS Bus Arbiter

Features

- Pin Compatible with Bipolar 8289
- Scaled SAJI IV CMOS Process
- Low Power Operation
  - ICCSB 10μA
  - ICCOP 1mA/MHz
- Compatible with 5MHz and 8MHz 80C86 and 80C88
- Provides Multi-Master System Bus Control and Arbitration
- Provides Simple Interface With 82C88/8288 Bus Controller
- Synchronizes 80C86/8086, 80C88/8088 Processors with Multi-Master Bus
- Bipolar Drive Capability, Fully TTL Compatible
- Four Operating Modes for Flexible System Configuration
- Wide Operating Temperature Ranges:
  - C82C89 .... 0°C to +70°C
  - I82C89 .... -40°C to +85°C
  - M82C89 .... -55°C to +125°C

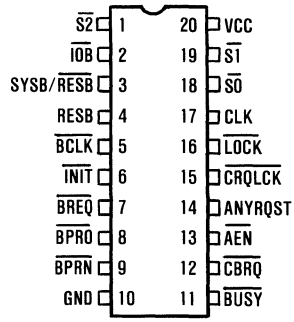
Description

The Harris 82C89 Bus Arbiter is manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). This circuit along with the 82C88 bus controller, provides full bus arbitration and control for multi-processor systems. The 82C89 is typically used in medium to large 80C86 or 80C88 systems where access to the bus by several processors must be coordinated. The 82C89 also provides high output current and capacitive drive to eliminate the need for additional bus buffering.

Static CMOS circuit design insures low operating power. The advanced Harris SAJI CMOS process results in performance equal to or greater than existing equivalent products at a significant power savings.

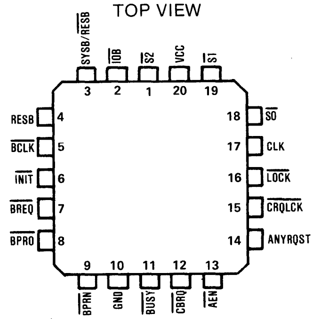
Pinouts

TOP VIEW



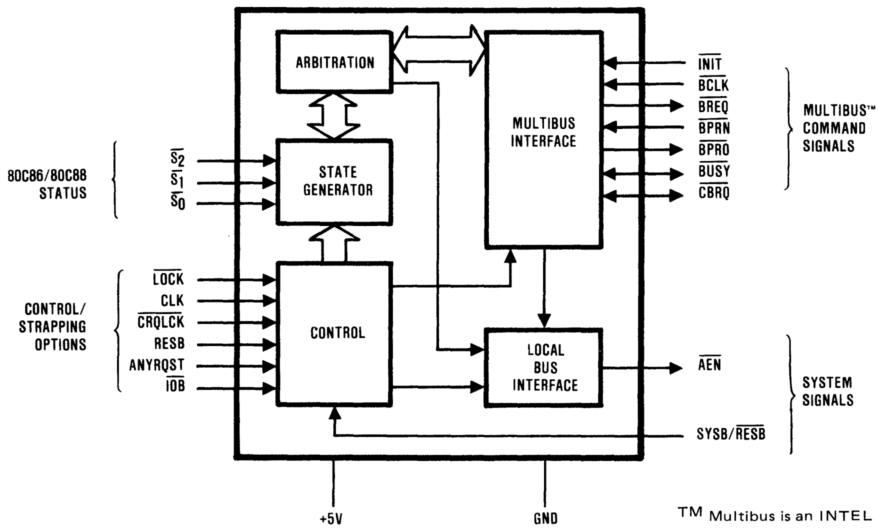
LCC/PLCC

TOP VIEW



3
CMOS 80C86 FAMILY

Functional Diagram



TM Multibus is an INTEL Corp trademark

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Pin Description

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
VCC	20		VCC: The +5V Power supply pin. A 0.1μF capacitor between pins 10 and 20 is recommended for decoupling.
GND	10		GROUND.
$\overline{S0}$, $\overline{S1}$, $\overline{S2}$	1, 18-19	I	STATUS INPUT PINS: The status input pins from an 80C86, 80C88 or 8089 processor. The 82C89 decodes these pins to initiate bus request and surrender actions. (See Table 1)
CLK	17	I	CLOCK: From the 82C84A or 82C85 clock chip and serves to establish when bus arbiter actions are initiated.
$\overline{LOCK}$	16	I	LOCK: A processor generated signal which when activated (low) prevents the arbiter from surrendering the multi-master system bus to any other bus arbiter, regardless of its priority.
$\overline{CRQLCK}$	15	I	COMMON REQUEST LOCK: An active low signal which prevents the arbiter from surrendering the multi-master system bus to any other bus arbiter requesting the bus through the $\overline{CBRQ}$ input pin.
RESB	4	I	RESIDENT BUS: A strapping option to configure the arbiter to operate in systems having both a multi-master system bus and a Resident Bus. Strapped high, the multi-master system bus is requested or surrendered as a function of the SYSB/$\overline{RESB}$ input pin. Strapped low, the SYSB/$\overline{RESB}$ input is ignored.
ANYRQST	14	I	ANY REQUEST: A strapping option which permits the multi-master system bus to be surrendered to a lower priority arbiter as if it were an arbiter of higher priority (i.e., when a lower priority arbiter requests the use of the multi-master system bus, the bus is surrendered as soon as it is possible). When ANYRQST is strapped low, the bus is surrendered according to Table 1. If ANYRQST is strapped high and $\overline{CBRQ}$ is activated, the bus is surrendered at the end of the present bus cycle. Strapping $\overline{CBRQ}$ low and ANYRQST high forces the 82C89 arbiter to surrender the multi-master system bus after each transfer cycle. Note that when surrender occurs $\overline{BREQ}$ is driven false (high).
$\overline{IOB}$	2	I	IO BUS: A strapping option which configures the 82C89 Arbiter to operate in systems having both an IO Bus (Peripheral Bus) and a multi-master system bus. The arbiter requests and surrenders the use of the multi-master system bus as a function of the status line, $\overline{S2}$. The multi-master system bus is permitted to be surrendered while the processor is performing IO commands and is requested whenever the processor performs a memory command. Interrupt cycles are assumed as coming from the peripheral bus and are treated as an IO command.
$\overline{AEN}$	13	O	ADDRESS ENABLE: The output of the 82C89 Arbiter to the processor's address latches, to the 82C88 Bus Controller and 82C84A or 82C85 Clock Generator. $\overline{AEN}$ serves to instruct the Bus Controller and address latches when to three-state their output drivers.
$\overline{INIT}$	6	I	INITIALIZE: An active low multi-master system bus input signal used to reset all the bus arbiters on the multi-master system bus. After initialization, no arbiters have the use of the multi-master system bus.
SYSB/$\overline{RESB}$	3	I	SYSTEM BUS/RESIDENT BUS: An input signal when the arbiter is configured in the System/Resident Mode (RESB is strapped high) which determines when the multi-master system bus is requested and multi-master system bus surrendering is permitted. The signal is intended to originate from a form of address-mapping circuitry, such as a decoder or PROM attached to the resident address bus. Signal transitions and glitches are permitted on this pin from φ1 of T4 to φ1 of T2 of the processor cycle. During the period from φ1 of T2 to φ1 of T4, only clean transitions are permitted on this pin (no glitches). If a glitch occurs, the arbiter may capture or miss it, and the multi-master system bus may be requested or surrendered, depending upon the state of the glitch. The arbiter requests the multi-master system bus in the System/Resident Mode when the state of the SYSB/$\overline{RESB}$ pin is high and permits the bus to be surrendered when this pin is low.

Pin Description

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
$\overline{CBRQ}$	12	I/O	COMMON BUS REQUEST: An input signal which instructs the arbiter if there are any other arbiters of lower priority requesting the use of the multi-master system bus. The $\overline{CBRQ}$ pins (open-drain output) of all the 82C89 Bus Arbiters which surrender to the multi-master system bus upon request are connected together. The Bus Arbiter running the current transfer cycle will not itself pull the $\overline{CBRQ}$ line low. Any other arbiter connected to the $\overline{CBRQ}$ line can request the multi-master system bus. The arbiter presently running the current transfer cycle drops its $\overline{BREQ}$ signal and surrenders the bus whenever the proper surrender conditions exist. Strapping $\overline{CBRQ}$ low and ANYRQST high allows the multi-master system bus to be surrendered after each transfer cycle. See the pin definition of ANYRQST.
$\overline{BCLK}$	5	I	BUS CLOCK: The multi-master system bus clock to which all multi-master system bus interface signals are synchronized.
$\overline{BREQ}$	7	O	BUS REQUEST: An active low output signal in the Parallel Priority Resolving Scheme which the arbiter activates to request the use of the multi-master system bus.
$\overline{BPRN}$	9	I	BUS PRIORITY IN: The active low signal returned to the arbiter to instruct it that it may acquire the multi-master system bus on the next falling edge of $\overline{BCLK}$. $\overline{BPRN}$ active indicates to the arbiter that it is the highest priority requesting arbiter presently on the bus. The loss of $\overline{BPRN}$ instructs the arbiter that it has lost priority to a higher priority arbiter.
$\overline{BPRO}$	8	O	BUS PRIORITY OUT: An active low output signal used in the serial priority resolving scheme where $\overline{BPRO}$ is daisy-chained to $\overline{BPRN}$ of the next lower priority arbiter.
$\overline{BUSY}$	11	I/O	BUSY: An active low open-drain multi-master system bus interface signal used to instruct all the arbiters on the bus when the multi-master system bus is available. When the multi-master system bus is available the highest requesting arbiter (determined by $\overline{BPRN}$) seizes the bus and pulls $\overline{BUSY}$ low to keep other arbiters off of the bus. When the arbiter is done with the bus, it releases the $\overline{BUSY}$ signal, permitting it to go high and thereby allowing another arbiter to acquire the multi-master system bus.

Functional Description

The 82C89 Bus Arbiter operates in conjunction with the 82C88 Bus Controller to interface 80C86, 80C88 processors to a multi-master system bus (both the 80C86 and 80C88 are configured in their max mode). The processor is unaware of the arbiter's existence and issues commands as though it has exclusive use of the system bus. If the processor does not have the use of the multi-master system bus, the arbiter prevents the Bus Controller (82C88), the data transceivers and the address latches from accessing the system bus (e.g. all bus driver outputs are forced into the high impedance state). Since the command sequence was not issued by the 82C88, the system bus will appear as "Not Ready" and the processor will enter wait states. The processor will remain in Wait until the Bus Arbiter acquires the use of the multi-master system bus whereupon the arbiter will allow the bus controller, the data transceivers, and the address latches to access the system. Typically, once the command has been issued and a data transfer has taken place, a transfer acknowledge (XACK) is returned to the processor to indicate "READY" from the accessed slave device. The processor then completes its transfer cycle. Thus the arbiter serves to multiplex a processor (or bus master) onto a multi-master system bus and avoid contention problems between bus masters.

Arbitration Between Bus Masters

In general, higher priority masters obtain the bus when a lower priority master completes its present transfer cycle. Lower priority bus masters obtain the bus when a higher priority master is not accessing the system bus. A strapping option (ANYRQST) is provided to allow the arbiter to surrender the bus to a lower priority master as though it were a master of higher priority. If there are no other bus masters requesting the bus, the arbiter maintains the bus so long as its processor has not entered the HALT State. The arbiter will not voluntarily surrender the system bus and has to be forced off by another master's bus request, the HALT State being the only exception. Additional strapping options permit other modes of operation wherein the multi-master system bus is surrendered or requested under different sets of conditions.

Priority Resolving Techniques

Since there can be many bus masters on a multi-master system bus, some means of resolving priority between bus masters simultaneously requesting the bus must be provided. The 82C89 Bus Arbiter provides several resolving techniques. All the techniques are based on a priority concept that at a given time one bus master will have priority above all the rest. There are provisions for using parallel priority resolving techniques, serial priority resolving techniques, and rotating priority techniques.

Parallel Priority Resolving

The parallel priority resolving technique uses a separate bus request line BREQ for each arbiter on the multi-master system bus, see Figure 1. Each BREQ line enters into a priority encoder which generates the binary address of the highest priority BREQ line which is active. The binary address is decoded by a decoder to select the corresponding BPRN (Bus Priority In) line to be returned to the highest priority requesting arbiter. The arbiter receiving priority (BPRN true) then allows its associated bus master onto the multi-master system bus as soon as it becomes available (i.e., the bus is no longer busy). When one bus arbiter gains priority over another arbiter it cannot immediately seize the bus, it must wait until the present bus transaction is complete. Upon completing its transaction the present bus occupant recognizes that it no longer has priority and surrenders the bus by releasing BUSY. BUSY is an active low "OR" tied signal line which goes to every bus arbiter on the system bus. When BUSY goes inactive (high), the arbiter which presently has bus priority (BPRN true) then seizes the bus and pulls BUSY low to keep other arbiters off of the bus. See waveform timing diagram, Figure 2. Note that all multi-master system bus transactions are synchronized to the bus clock (BCLK). This allows the parallel priority resolving circuitry or any other priority resolving scheme employed to settle.

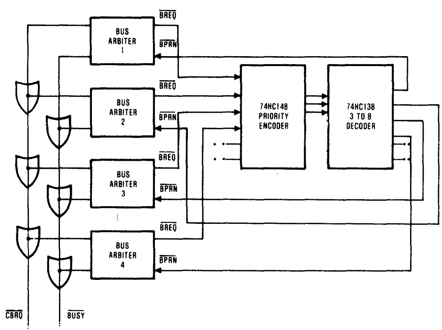
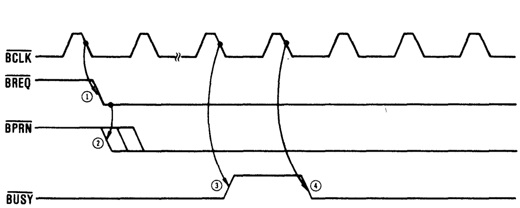


FIGURE 1. PARALLEL PRIORITY RESOLVING TECHNIQUE



NOTES:

① Higher priority bus arbiter requests the Multi-Master system bus.

② Attains priority.

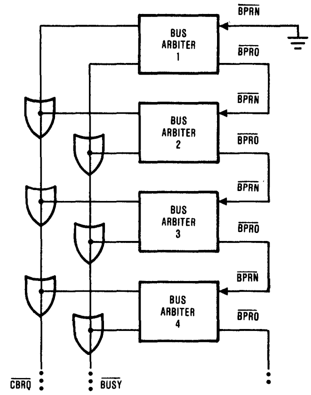
③ Lower priority bus arbiter releases BUSY.

④ Higher priority bus arbiter then acquires the bus and pulls BUSY down.

FIGURE 2. HIGHER PRIORITY ARBITER OBTAINING THE BUS FROM A LOWER PRIORITY ARBITER

Serial Priority Resolving

The serial priority resolving technique eliminates the need for the priority encoder-decoder arrangement by daisy-chaining the bus arbiters together, connecting the higher priority bus arbiter's BPRO (Bus Priority Out) output to the BPRN of the next lower priority. See Figure 3.



NOTE:

The number of arbiters that may be daisy-chained together in the serial priority resolving scheme is a function of BCLK and the propagation delay from arbiter to arbiter. Normally, at 10MHz only 3 arbiters may be daisy-chained.

FIGURE 3. SERIAL PRIORITY RESOLVING

Rotating Priority Resolving

The rotating priority resolving technique is similar to that of the parallel priority resolving technique except that priority is dynamically re-assigned. The priority encoder is replaced by a more complex circuit which rotates priority between requesting arbiters thus allowing each arbiter an equal chance to use the multi-master system bus, over time.

Which Priority Resolving Technique To Use

There are advantages and disadvantages for each of the techniques described above. The rotating priority resolving technique requires substantial external logic to implement while the serial technique uses no external logic but can accommodate only a limited number of bus arbiters before the daisy-chain propagation delay exceeds the multi-master's system bus clock (BCLK). The parallel priority resolving technique is in general a good compromise between the other two techniques. It allows for many arbiters to be present on the bus while not requiring too much logic to implement.

82C89 Modes Of Operation

There are two types of processors for which the 82C89 will provide support: An Input/Output processor (i.e. an NMOS 8089 IOP) and the 80C86, 80C88. Consequently, there are two basic operating modes in the 82C89 bus arbiter. One, the IOB (I/O Peripheral Bus) mode, permits the processor access to both an I/O Peripheral Bus and a multi-master system bus. The second, the RESB (Resident Bus mode), permits the processor to communicate over both a Resident Bus and a multi-master system bus. An I/O Peripheral Bus is a bus where all devices on that bus, including memory, are treated as I/O devices and are addressed by I/O commands. All memory commands are directed to another bus, the multi-master system bus. A Resident Bus can issue both memory and I/O commands, but it is a distinct and separate bus from the multi-master system bus. The distinction is that the Resident Bus has only one master, providing full availability and being dedicated to that one master.

The $\overline{\text{IOB}}$ strapping option configures the 82C89 Bus Arbiter into the $\overline{\text{IOB}}$ mode and the strapping option RESB configures it into the RESB mode. It might be noted at this point that if both strapping options are strapped false, the arbiter interfaces the processor to a multi-master system bus only (see Figure 4). With both options strapped true, the arbiter interfaces the processor to a multi-master system bus, a Resident Bus, and an I/O Bus.

In the $\overline{\text{IOB}}$ mode, the processor communicates and controls a host of peripherals over the Peripheral Bus. When the I/O Processor needs to communicate with system memory, it does so over the system memory bus. Figure 5 shows a possible I/O Processor system configuration.

The 80C86 and 80C88 processors can communicate with a Resident Bus and a multi-master system bus. Two bus controllers and only one Bus Arbiter would be needed in such a configuration as shown in Figure 6. In such a system configuration the processor would have access to

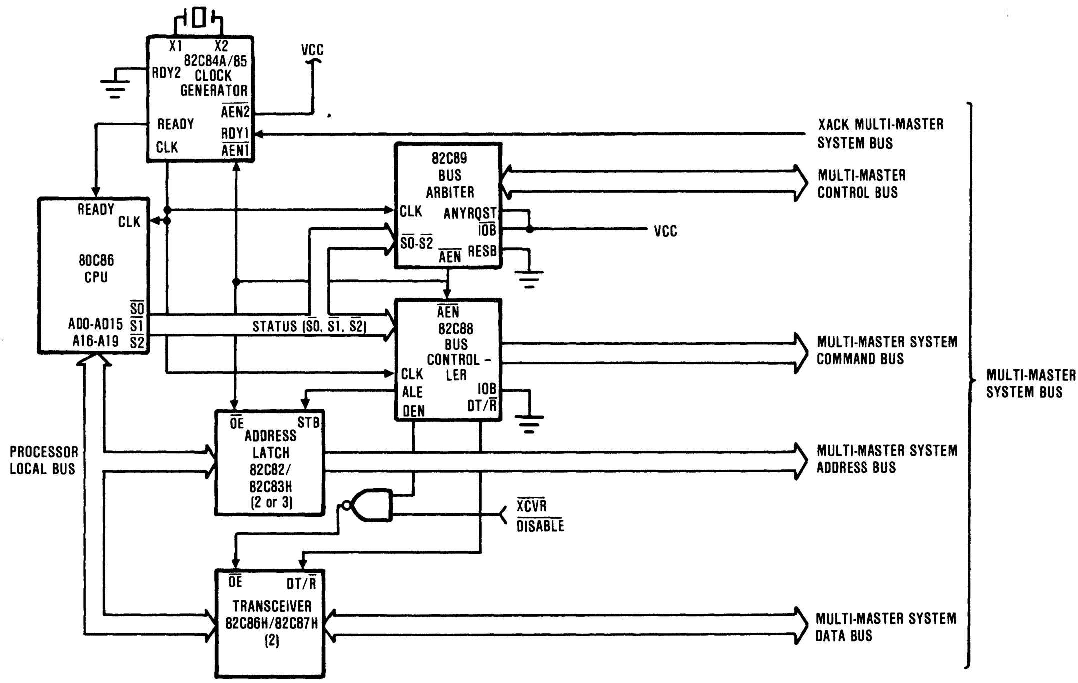


FIGURE 4. TYPICAL MEDIUM COMPLEXITY CPU SYSTEM

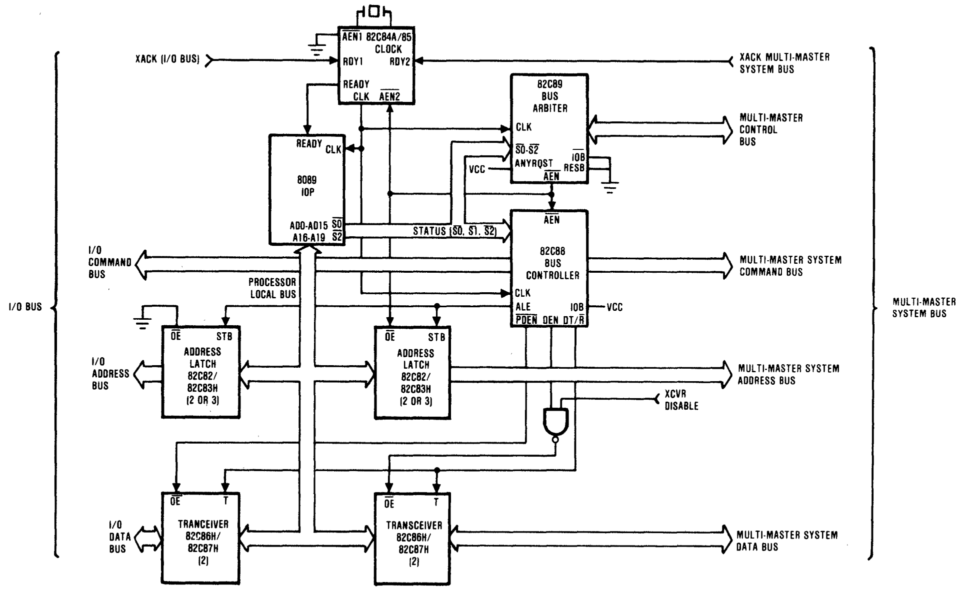


FIGURE 5. TYPICAL MEDIUM COMPLEXITY IOB SYSTEM

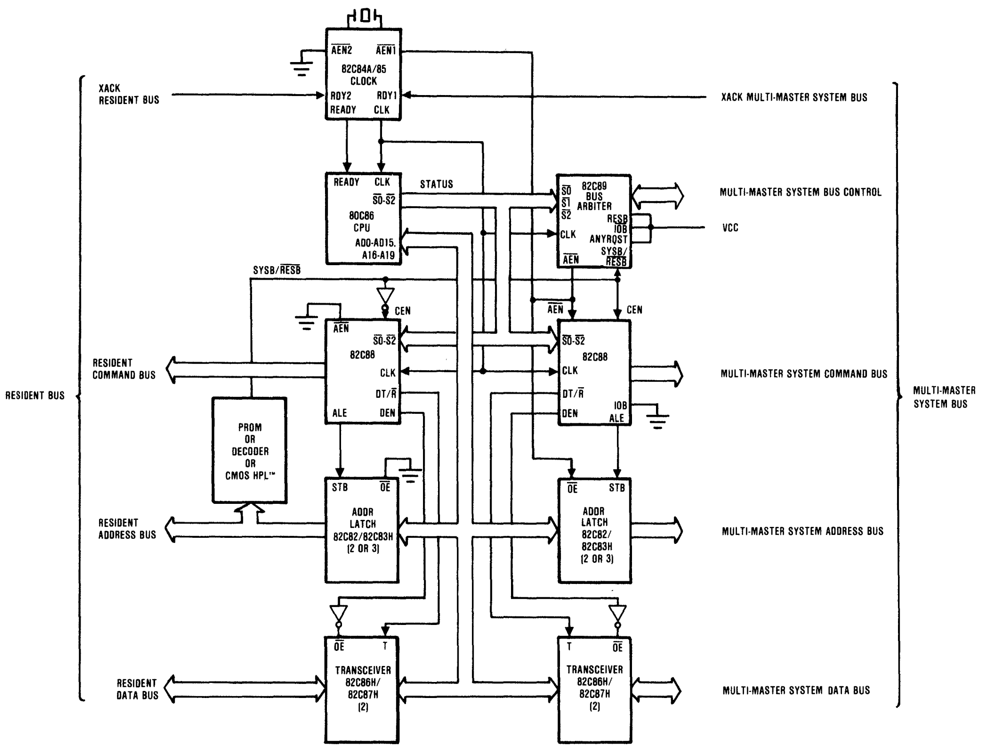


FIGURE 6. 82C89 BUS ARBITER SHOWN IN SYSTEM- RESIDENT BUS CONFIGURATION

* By adding another 82C89 arbiter and connecting its $\overline{AEN}$ to the 82C88 whose $\overline{AEN}$ is presently grounded. The processor could have access to two multi-master buses.

memory and peripherals of both busses. Memory mapping techniques are applied to select which bus is to be accessed. The SYSB/$\overline{RESB}$ input on the arbiter serves to instruct the arbiter as to whether or not the system bus is to be accessed. The signal connected to SYSB/$\overline{RESB}$ also enables or disables commands from one of the bus controllers.

A summary of the modes that the 82C89 has, along with its response to its status lines inputs, is shown in Table 1.

TABLE 1. SUMMARY OF 82C89 MODES, REQUESTING AND RELINQUISHING THE MULTI-MASTER SYSTEM BUS

STATUS LINES FROM 80C86 OR 80C88 OR 8088				IOB MODE ONLY $\overline{IOB}$ = LOW RESB = LOW	RESB MODE ONLY $\overline{IOB}$ = HIGH RESB = HIGH		IOB MODE RESB MODE $\overline{IOB}$ = LOW RESB = HIGH		SINGLE BUS MODE $\overline{IOB}$ = HIGH RESB = LOW
	$\overline{S2}$	$\overline{S1}$	$\overline{S0}$		SYSB/$\overline{RESB}$=High	SYSB/$\overline{RESB}$=Low	SYSB/$\overline{RESB}$=High	SYSB/$\overline{RESB}$=Low	
I/O COMMANDS	0	0	0	X	✓	X	X	X	✓
	0	0	1	X	✓	X	X	X	✓
	0	1	0	X	✓	X	X	X	✓
HALT	0	1	1	X	X	X	X	X	X
MEM COMMANDS	1	0	0	✓	✓	X	✓	X	✓
	1	0	1	✓	✓	X	✓	X	✓
	1	1	0	✓	✓	X	✓	X	✓
IDLE	1	1	1	X	X	X	X	X	X

NOTES:
1. X = Multi-Master System Bus is allowed to be Surrendered.
2. ✓ = Multi-Master System Bus is Requested.

MODE	PIN STRAPPING	MULTI-MASTER SYSTEM BUS REQUESTED**	MULTI-MASTER SYSTEM BUS SURRENDERED*
Single Bus Multi-Master Mode	$\overline{IOB}$ = High RESB = Low	Whenever the processor's status lines go active	HLT + TI • $\overline{CBRQ}$ + HPBRQ †
RESB Mode Only	$\overline{IOB}$ = High RESB = High	SYSB/$\overline{RESB}$ = High • ACTIVE STATUS	(SYSB/$\overline{RESB}$ = Low + TI) • $\overline{CBRQ}$ + HLT + HPBRQ
IOB Mode Only	$\overline{IOB}$ = Low RESB = Low	Memory Commands	(I/O Status + TI) • $\overline{CBRQ}$ + HLT + HPBRQ
IOB Mode RESB Mode	$\overline{IOB}$ = Low RESB = High	(Memory Command) • (SYSB/$\overline{RESB}$ = High)	((I/O Status Commands) + SYSB/$\overline{RESB}$ = LOW) • $\overline{CBRQ}$ + HPBRQ † + HLT

NOTES:
* $\overline{LOCK}$ prevents surrender of Bus to any other arbiter, $\overline{CRQLCK}$ prevents surrender of Bus to any lower priority arbiter.
** Except for HALT and Passive or IDLE Status.
† HPBRQ, Higher priority Bus request or $\overline{BPRN}$ = 1.
1. $\overline{IOB}$ Active Low.
2. RESB Active High.
3. + is read as "OR" and • as "AND"
4. TI = Processor Idle Status $\overline{S2}$, $\overline{S1}$, $\overline{S0}$ = 111
5. HLT = Processor Halt Status $\overline{S2}$, $\overline{S1}$, $\overline{S0}$ = 011

Absolute Maximum Ratings

Supply Voltage	+8.0 Volts
Input, Output or I/O Voltage Applied	GND -0.5V to VCC +0.5V
Maximum Package Power Dissipation	1 Watt
Storage Temperature Range	-65°C to +150°C
θ_{jc}	26°C/W (CERDIP package), 31°C/W (LCC package)
θ_{ja}	76°C/W (CERDIP package), 81°C/W (LCC package)
Gate Count	200 Gates
Junction Temperature	+150°C
Lead Temperature (Soldering, Ten Seconds)	+260°C

CAUTION: Stresses above those listed in the "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied.

Operating Conditions

Operating Voltage Range	+4.5V to +5.5V
Operating Temperature Range	
C82C89	0°C to +70°C
I82C89	-40°C to +85°C
M82C89	-55°C to +125°C

D.C. Electrical Specifications

VCC = 5.0V ± 10%; T_A = 0°C to +70°C (C82C89); T_A = -40°C to +85°C (I82C89); T_A = -55°C to +125°C (M82C89)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	Logical One Input Voltage	2.0 2.2		V V	C82C89, I82C89 M82C89
VIL	Logical Zero Input Voltage		0.8	V	
VIHC	CLK Logical One Input Voltage	0.7 VCC		V	
VILC	CLK Logical Zero Input Voltage		0.2 VCC	V	
V_{OL}	Output Low Voltage $\overline{BUSY}$, $\overline{CBRQ}$ $\overline{AEN}$ $\overline{BPRO}$, $\overline{BREQ}$		 0.45 0.45 0.45	 V V V	 I_{OL} = 20mA I_{OL} = 16mA I_{OL} = 10mA
V_{OH}	Output High Voltage $\overline{BUSY}$, $\overline{CBRQ}$	Open-Drain			
	All other Outputs	3.0 VCC -0.4		V V	I_{OH} = -2.5mA I_{OH} = -100μA
II	Input Leakage Current	-1.0	1.0	μA	VIN = GND or VCC DIP Pins 1-6, 9, 14-19
IO	I/O Leakage	-10.0	10.0	μA	VO = GND orVCC DIP Pins 11-12
ICCSB	Standby Power Supply Current		10	μA	VCC = 5.5V VIN = VCC or GND Outputs Open
ICCOP	Operating Power Supply Current		1	mA/MHz	VCC = 5.5V Outputs Open See Note 1

NOTE 1: Maximum current defined by CLK or BCLK, whichever has the highest operating frequency

Capacitance

T_A = 25°C, V_{CC} = GND = 0V; V_{IN} = +5V or GND

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_{IN}	Input Capacitance	5	pF	FREQ = 1MHz Unmeasured pins returned to GND
C_{OUT}	Output Capacitance	15	pF	

A.C. Electrical Specifications

VCC = +5V ±10%, GND = 0V: T_A = 0°C to 70°C (C82C89)
T_A = -40°C to +85°C (I82C89)
T_A = -55°C to +125°C (M82C89)

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
TCLCL	CLK Cycle Period	125		ns	Note 3
TCLCH	CLK Low Time	55		ns	
TCHCL	CLK High Time	35		ns	
TSVCH	Status Active Setup	65	TCLCL-10	ns	
TSHCL	Status Inactive Setup	50	TCLCL-10	ns	
THVCH	Status Active Hold	10		ns	
THVCL	Status Inactive Hold	10		ns	
TBYSBL	BUSY↑↓ Setup to BCLK↓	20		ns	
TCBSBL	CBRQ↑↓ Setup to BCLK↓	20		ns	
TBLBL	BCLK Cycle Time	100		ns	
TBHCL	BCLK High Time	30	0.65(TBLBL)	ns	
TCLLL1	LOCK Inactive Hold	10		ns	
TCLLL2	LOCK Active Setup	40		ns	
TPNBL	BPRN↑↓ to BCLK Setup Time	15		ns	
TCLSR1	SYSB/RESB Setup	0		ns	
TCLSR2	SYSB/RESB Hold	30		ns	
TIVIH	Initialization Pulse Width	3 TBLBL+ 3 TCLCL		ns	
TBLBRL	BCLK to BREQ Delay↓↑		35	ns	
TBLPOH	BCLK to BPRO↓↑		40	ns	Note 1 and 3
TPNPO	BPRN↓↑ to BPRO↓↑ Delay		25	ns	Note 1 and 3
TBLBYL	BCLK to BUSY Low		60	ns	Note 3
TBLBYH	BCLK to BUSY Float		35	ns	Note 2 and 3
TCLAEH	CLK to AEN High		65	ns	Note 3
TBLAEL	BCLK to AEN Low		40	ns	Note 3
TBLCBL	BCLK to CBRQ Low		60	ns	Note 3
TRLCRH	BCLK to CBRQ Float		35	ns	Note 2 and 3
TOLOH	Output Rise Time		20	ns	From 0.8V to 2.0V Note 4
TOHOL	Output Fall Time		12	ns	From 2.0V to 0.8V Note 4
TILIH	Input Rise Time		20	ns	From 0.8V to 2.0V
TIHIL	Input Fall Time		20	ns	From 2.0V to 0.8V

NOTES:
1. BCLK generates the first BPRO wherein subsequent BPRO changes lower in the chain are generated through BPRON.
2. Measured at 0.5V above GND.
3. All A.C. parameters tested as per test circuits in Figures 7—9. Input rise and fall times are driven at 1ns/V.
4. Except BUSY and CBRQ.

A.C. Test Circuits

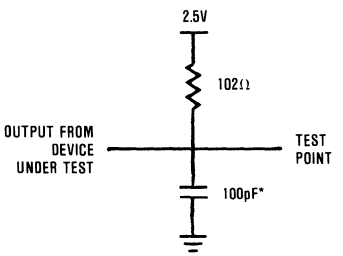


FIGURE 7.
BUSY, CBRQ LOAD CIRCUIT

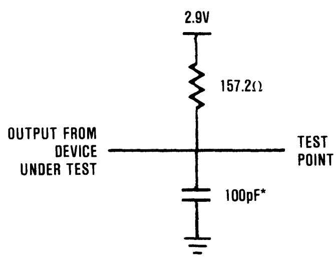


FIGURE 8.
AEN LOAD CIRCUIT

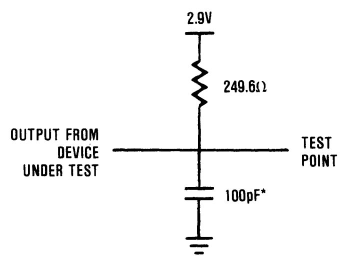


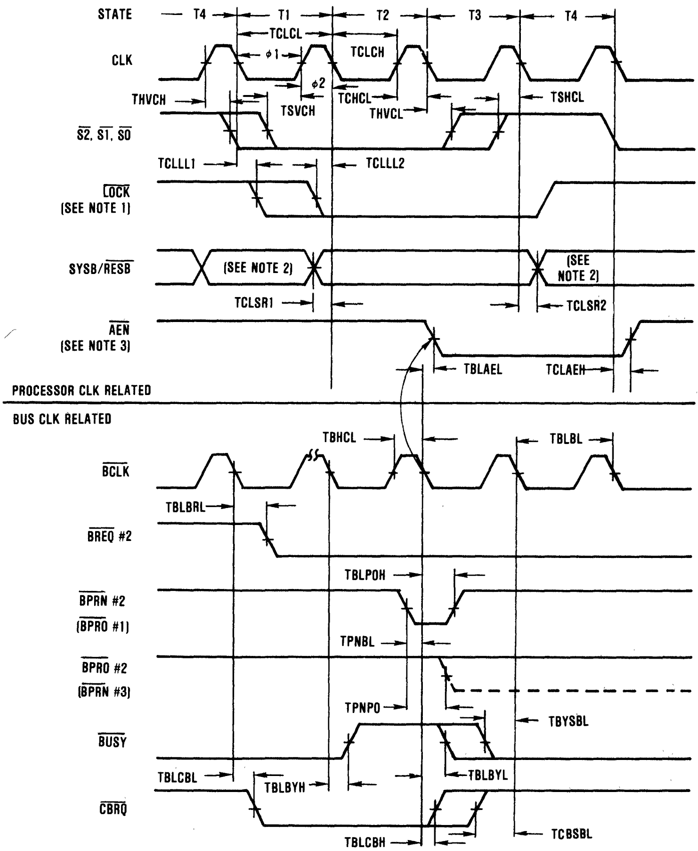
FIGURE 9.
BPRO, BREQ LOAD CIRCUIT

*Includes stray and jig capacitance

A.C. Testing Input, Output Waveforms

A.C. Testing: Inputs are driven at VIH +0.4V for a logic "1" and VIL -0.4V for a logic "0". The clock is driven at 4.1V and 0.4V. Timing measurements are made at 1.5V for both a logic "1" and "0".

Waveforms



NOTES:

1. Lock active can occur during any state, as long as the relationships shown above with respect to the CLK are maintained. LOCK inactive has no critical time and can be asynchronous. CRQLCK has no critical timing and is considered an asynchronous input signal.
2. Glitching of SYSB/RESB is permitted during this time. After $\phi 2$ of T1, and before $\phi 1$ of T4, SYSB/RESB should be stable to maintain system efficiency.
3. AEN leading edge is related to BCLK, trailing edge to CLK. The trailing edge of AEN occurs after bus priority is lost.

ADDITIONAL NOTES:

The signals related to CLK are typical processor signals, and do not relate to the depicted sequence of events of the signals referenced to BCLK. The signals shown related to the BCLK represent a hypothetical sequence of events for illustration. Assume 3 bus arbiters of priorities 1,2 and 3 configured in serial priority resolving scheme (as shown in Figure 3). Assume arbiter 1 has the bus and is holding BUSY low. Arbiter #2 detects its processor wants the bus and pulls low BREQ #2. If BPRN #2 is high (as shown), arbiter #2 will pull low CPRQ line. CBRQ signals to the higher priority arbiter #1 that a lower priority arbiter wants the bus. [A higher priority arbiter would be granted BPRN when it makes the bus request rather than having to wait for another arbiter to release the bus through CBRQ]. *Arbiter #1 will relinquish the multi-master system bus when it enters a state not requiring it (see Table 1), by lowering its BPRO #1 (tied to BPRN #2) and releasing BUSY. Arbiter #2 now sees that is has priority from BPRN #2 being low and releases CBRQ. As soon as BUSY signifies the bus is available (high), arbiter #2 pulls BUSY low on next falling edge of BCLK. Note that if arbiter #2 didn't want the bus at the time it received priority, it would pass priority to the next lower priority arbiter by lowering its BPRO #2 [TPNPO].

*Note that even a higher priority arbiter which is acquiring the bus through BPRN will momentarily drop CBRQ until it has acquired the bus.

82C59A PRIORITY INTERRUPT CONTROLLER

By J. A. Goss

PAGE

82C59A CMOS PROGRAMMABLE INTERRUPT CONTROLLER

By J. A. Goss

Introduction

The Harris 82C59A is a CMOS Priority Interrupt Controller, designed to relieve the system CPU from the task of polling in a multi-level priority interrupt system. The 82C59A is compatible with microprocessors such as the 80C86, 80C88, 8086, 8088, 8080/85 and NSC800.

In the following discussion, we will look at the initialization and operation process for the 82C59A. We will focus our attention on 80C86/80C88-based systems. However, the information presented will also be applicable to use of the 82C59A in 8080 or 8085-based systems as well.

Let us look at the sequence of events that occur with the 82C59A during an interrupt request and service. In an 8080/85 based system:

(1) One or more of the INTERRUPT REQUEST lines (IR0 - IR7) are raised high, setting the corresponding bits in the Interrupt Request Register (IRR).

(2) The interrupt is evaluated in the priority resolver. If appropriate, an interrupt is sent to the CPU via the INT line (pin 17).

(3) The CPU acknowledges the interrupt by sending a pulse on the $\overline{INTA}$ line. Upon reception of this pulse, the 82C59A responds by forcing the opcode for a call instruction (0CDH) onto the data bus.

(4) A second $\overline{INTA}$ pulse is sent from the CPU. At this time, the device will respond by placing the lower byte of the address of the appropriate service routine onto the data bus. This address is derived from ICW1.

(5) A final (third) pulse of $\overline{INTA}$ occurs, and the 82C59A responds by placing the upper byte of the address onto the data bus. This address is taken from ICW2.

(6) The three byte call instruction is then complete. If the AEOI mode has been chosen, the bit set during the first $\overline{INTA}$ pulse in the ISR is reset at the end of the third $\overline{INTA}$ pulse. Otherwise, it will not get reset until an appropriate EOI command is issued to the 82C59A.

For 80C86- and 80C88-based systems:

(1) and (2) same as above.

(3) The CPU responds to the interrupt request by pulsing the $\overline{INTA}$ line twice. The first pulse sets the appropriate ISR bit and resets the IRR bit while the second pulse causes the interrupt vector to be placed on the data bus. This byte is composed of the interrupt number in bits 0 through 2, and bits 3 through 7 are taken from bits 3 - 7 of ICW2.

(4) The interrupt sequence is complete. If using the AEOI mode, the bit set earlier in the ISR will be reset. Otherwise, the interrupt controller will await an appropriate EOI command at the end of the interrupt service routine.

1.0 Glossary of Terms for the 82C59A

1.1 Automatic End of Interrupt (AEOI):

When the 82C59A is programmed to operate in the Automatic EOI mode, the device will produce its own End-of-Interrupt (EOI) at the trailing edge of the last Interrupt Acknowledge pulse ($\overline{INTA}$) from the CPU. Using this mode of operation frees the software (service routines) from needing to send an EOI manually to the 82C59A.

However, using the Automatic EOI mode will upset the priority structure of the 82C59A. When the AEOI is generated, the bit that was set in the In-Service Register (ISR) to indicate which interrupt is being serviced, will be cleared. Because of this, while an interrupt is being serviced there will be no record in the ISR that it is being serviced. Unless interrupts are disabled by the CPU, there is a risk that interrupt requests of lower or equal priority will interrupt the current request being serviced. If this mode of operation is not desired, interrupts should not be re-enabled by the CPU when executing interrupt service routines.

1.2 Automatic Rotation:

During normal operation of the 82C59A, we have an assigned order of priorities for the IR lines. There are however, instances when it might be useful to assign equal priorities to all interrupts. Once a particular interrupt has been serviced, all other equal priority interrupts should have an opportunity to be serviced before the original peripheral can be serviced again. This priority equalization can be achieved through Automatic Rotation of priorities.

Assume, for example, that the assigned priorities of interrupts has IR0 as the highest priority interrupt and IR7 as the lowest. Figure 1A shows interrupt requests occuring on IR7 as well as IR3. Because IR3 is of higher priority, it will be serviced first. Upon completion of the servicing of IR3, rotation occurs and IR3 then becomes the lowest priority interrupt. IR4 will now have the highest priority (see Figure 1B).

There are two methods in which Automatic Rotation can be implemented. First, if the 82C59A is operating in the AEOI mode as described above, the 82C59A can be programmed for "Rotate in Automatic EOI mode". This is done by writing a command word to OCW2. The second method occurs when using normal EOIs. When an EOI is issued by the service routine, the software can specify that rotation be performed.

	IR7	IR6	IR5	IR4	IR3	IR2	IR1	IR0
IRR STATUS	1	0	0	0	1	0	0	0
PRIORITY	7	6	5	4	3	2	1	0
	LOWEST PRIORITY							HIGHEST PRIORITY

FIGURE 1A. IR PRIORITIES (BEFORE ROTATION)

	IR7	IR6	IR5	IR4	IR3	IR2	IR1	IR0
ISR STATUS	1	0	0	0	0	0	0	0
PRIORITY	3	2	1	0	7	6	5	4

HIGHEST PRIORITY ... LOWEST PRIORITY

FIGURE 1B. IR PRIORITIES (AFTER ROTATION)

1.3 Buffered Mode:

When using the 82C59A in a large system, it may be necessary to use bus buffers to guarantee data integrity and guard against bus contention.

By selecting buffered mode when initializing the device, the $\overline{SP}/\overline{EN}$ pin (pin 16) will generate an enable signal for the buffers whenever the data outputs from the 82C59A are active. In this mode, the dual function $\overline{SP}/\overline{EN}$ pin can no longer be used for specifying whether a particular 82C59A is being used as a master or a slave in the system. This specification must be made through setting the proper bit in ICW4 during the device initialization.

1.4 Cascade Mode:

More than one 82C59A can be used in a system to expand the number of priority interrupts to a maximum of 64 levels without adding any additional hardware. This method of expansion is known as "cascading". An example of cascading 82C59As is shown in Figure 2.

In a cascaded interrupt scheme, a single 82C59A is utilized as the "master" interrupt controller. As many as 8 "slave" 82C59As can be connected to the IR inputs of the "master" 82C59A. Each of these slaves can support up to 8 interrupt inputs, yielding 64 possible prioritized interrupts.

When in cascade mode, the determination of whether a device is a master or a slave can take either of two forms. The state of the $\overline{SP}/\overline{EN}$ pin will select "master" or "slave" mode for a device when the buffered mode is not being used. Should buffered mode be used, then it is necessary that bit D2 (M/S) of ICW4 be set to indicate if the particular 82C59A is being used as a "master" or "slave" interrupt controller in the system.

The CAS0-2 pins on the interrupt controllers serve to provide a private bus for the cascaded 82C59As. These lines allow the "master" to inform the slaves which is to be serviced for a particular interrupt.

1.5 End of Interrupt (EOI):

When an interrupt is recognized and acknowledged by the CPU, its corresponding bit will be set in the In-Service Register (ISR). If the AEOI mode is in use, the bit will be cleared automatically through the interrupt acknowledge signal from the CPU. However, if AEOI is not in effect, it is the task of software to notify the 82C59A when servicing of an interrupt is completed. This is done by issuing an End-of-Interrupt (EOI).

There are 2 different types of EOIs that can be issued to the device; non-specific EOI and specific EOI. In most cases, when the device is operating in a mode that does not disturb the fully nested mode such as Special Fully Nested Mode, we will issue a non-specific EOI. This form of the EOI will automatically reset the highest priority bit set in the ISR. This is because for full nested operation, the highest priority IS bit set is the last interrupt level acknowledged and serviced.

The "specific" EOI is used when the fully nested structure has not been preserved. The 82C59A may not be able to determine the last level acknowledged. Thus, the software must specify which interrupt level is to be reset. This is done by issuing a "specific" EOI.

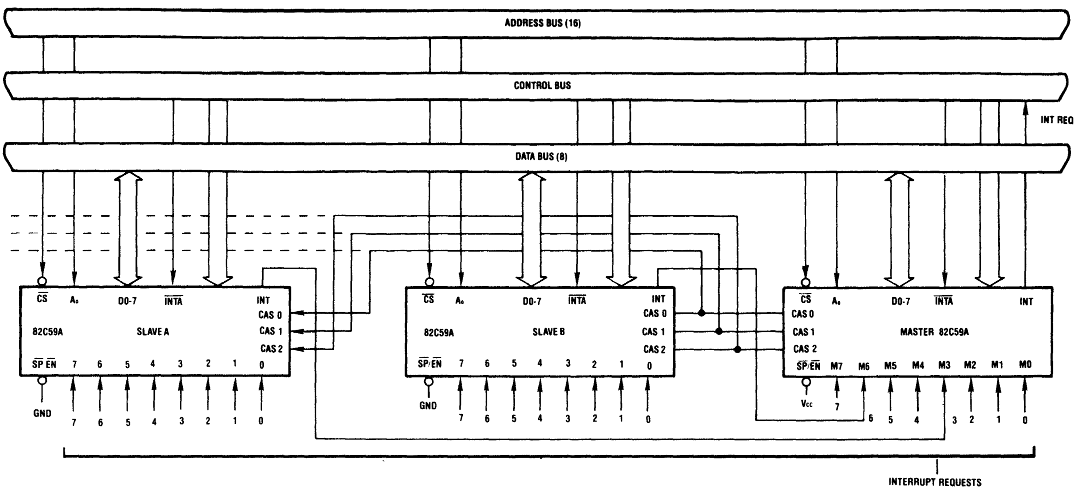


FIGURE 2. CASCADING THE 82C59A

1.6 Fully Nested Mode:

By default, the 82C59A operates in the Fully Nested Mode. It will remain in this mode until it is programmed otherwise. In the Fully Nested Mode, interrupts are ordered by priority from highest to lowest. Initially, the highest priority level is IR0 with IR7 having the lowest. This ordering can be changed through the use of priority rotation (see 1.2).

In the Fully Nested Mode, when an interrupt occurs, its corresponding bit will get set in the Interrupt Request Register (IRR). When the processor acknowledges the interrupt, the 82C59A will look to the IRR to determine the highest priority interrupt requesting service. The bit in the In-service Register (ISR) corresponding to this interrupt will then be set. This bit remains set until an EOI is sent to the 82C59A.

While an interrupt is being serviced, only higher priority interrupts will be allowed to interrupt the current interrupt being serviced. However, lower priority interrupts can be allowed to interrupt higher priority requests if the 82C59A is programmed for operation in the Special Mask Mode.

When using the 82C59A in an 80C86- or 80C88-based system, interrupts will automatically be disabled when the processor begins servicing an interrupt request. The current address and the state of the flags in the processor will be pushed onto the stack. The interrupt-enable flag is then cleared. To allow interrupts to occur at this point, the STI instruction can be used. Upon exiting the service routine using the IRET instruction, execution of the program is resumed at the point where the interrupt occured, and the flags are restored to their original values, thus re-enabling interrupts.

A configuration in which the Fully Nested structure is not preserved occurs when one or more of the following conditions occur:

(a) The Automatic EOI mode is being used.

(b) The Special Mask Mode is in use.

(c) A slave 82C59A has a master that is not programmed to the Special Fully Nested Mode.

Cases (a) and (b) differ from case (c) in that the 82C59A would allow lower priority interrupt requests the opportunity to be serviced before higher priority interrupt requests.

1.7 Master:

When using multiple 82C59As in a system, one 82C59A has control over all other 82C59As. This is known as the "master" interrupt controller. Communication between the master and the other (slave) 82C59As occurs via the CAS0 - 2 lines. These lines form a private bus between the multiple 82C59As. Also, the INT lines from the slaves are routed to the master's IR input pin(s). See Figure 2.

1.8 Slave:

A "slave" 82C59A in a system is controlled by a master 82C59A. There is but one "master" in the system, but there can be up to 8 slave 82C59As. The INT outputs from the slaves act as inputs to the master through it's IR inputs. Communications between the master and slaves occurs via the CAS0 - 2 lines. See Figure 2.

1.9 Special Fully Nested Mode:

The Special Fully Nested Mode (SFNM) is used in a system having multiple 82C59As where it is necessary to preserve the priority of interrupts within a slave 82C59A. Only the master is programmed for the Special Fully Nested Mode through ICW4. This mode is similar to the Fully Nested Mode with the following exceptions:

(a) When an interrupt from a particular slave is being serviced, additional higher priority interrupts from that slave can cause an interrupt to the master. Normally, a slave is masked out when its request is in service.

(b) When exiting the Interrupt Service routine, the software should first issue a non-specific EOI to the slave. The In-service Register (ISR) should then be read and checked to see if its contents are zero. If the register is empty, the software should then write a non-specific EOI to the master. Otherwise, a second EOI need not be written because there are interrupts from that slave still being processed.

NOTE: Because the Master 82C59A and its slave 82C59As must be in Fully Nested Mode for this mode to be functional, we could not utilize Automatic EOIs. These would disturb the Fully Nested structure, as described in section 1.6.

1.10 Special Mask Mode:

The Special Mask Mode is utilized in order to allow interrupts from all other levels (higher and lower as well) to interrupt the IR level that is currently being serviced. Invoking this mode of operation will disturb the fully nested priority structure.

Generally, the Special Mask Mode is selected during the servicing of an interrupt. The software should first set the bit corresponding to the IR level being serviced, in the Interrupt Mask Register (OCW1). The Special Mask Mode and interrupts should then be enabled. This will allow any of the IR levels except for those masked off by OCW1 to interrupt the IR level currently being serviced.

Because this disturbs the Fully Nested Structure, it is required that a Specific EOI be issued when servicing interrupts while the Special Mask Mode is in effect. Before exiting the original interrupt routine, the Special Mask Mode should be disabled.

1.11 Specific Rotation:

By issuing the proper command word to OCW2, the priority structure of the 82C59A can be dynamically altered. The command word written to OCW2 would specify which is to be the lowest priority IR level.

This specific rotation can be accomplished one of two ways. The first is through a specific EOI. The software can specify that rotation is to be applied to the IR level provided with the EOI. The second method is a simple "set priority" command, in which the lowest priority level is specified with the command word.

2.0 *Initialization Control Words*

The following section gives a description of the Initialization Control Words (ICW) used for configuring the 82C59A Interrupt controller. There are four (4) control words used for initialization of the 82C59A. These ICWs must be programmed in the proper sequence beginning with ICW1. If at any time during the course of operation the configuration of the 82C59A needs to be changed, the user must again write out the control words to the device in their proper order. The initialization sequence is shown in Figure 3.

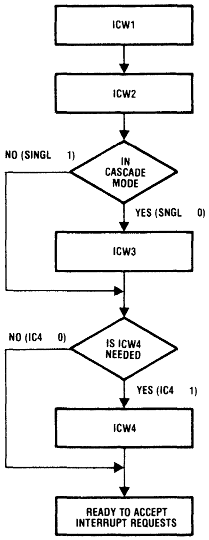


FIGURE 3. 82C59A INITIALIZATION SEQUENCE

ICW1: The 82C59A recognizes the first Initialization Control Word (ICW) written to it based on two criteria: (1) the A0 line from the address bus must be a zero, and (2) the D4 bit must be a one. If the D4 bit is set to a zero, we would be programming either OCW2 or OCW3 (these are explained later). The function of ICW1 is to tell the 82C59A how it is being used in the system (i.e. Single or cascaded, edge or level triggered interrupts etc.).

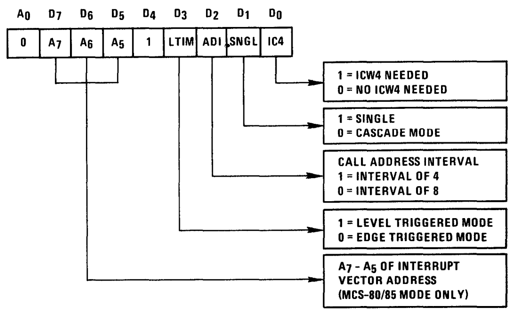
ICW2: This control word is always issued directly after ICW1. When addressing this ICW, the A0 line from the address bus must be a one (high). ICW2 is utilized in providing the CPU with information on where to vector to in memory when servicing an interrupt.

ICW3: This control word is issued only if the SNGL (D1) bit of ICW1 has been programmed with a zero. When addressing this word, the A0 line from the CPU must be high (1). This control word is for cascaded 82C59A's. It allows the master and slave 82C59As to communicate via the CAS0-2 lines. With the master, this word indicates which IR lines have slaves connected to them. For the slave 82C59A(s), this word indicates to which IR line on the master it is connected.

ICW4: Issuance of this ICW is selectable through the IC4 (D0) bit of ICW4. If ICW4 is to be written to the 82C59A, A0 from the CPU must be high (1) when writing to it. This word needs to be written only when the 82C59A is operating in modes other than the default modes. Instances when we would want to write to ICW4 are one or more of the following: An 80C86(80C88) processor is being used, buffered outputs (D0-D7) are to be used, Automatic EOIs are desired, or the Special Fully Nested mode is to be used.

2.1 ICW1:

ICW1 is the first control word that is written to the 82C59A during the initialization process.. To access this word, the value of A0 must be a zero (0) in the addressing, and bit D4 of ICW1 must be a one (1). The format of the command word is as follows:



* NOTE: This is an address bit, and not part of the ICW.

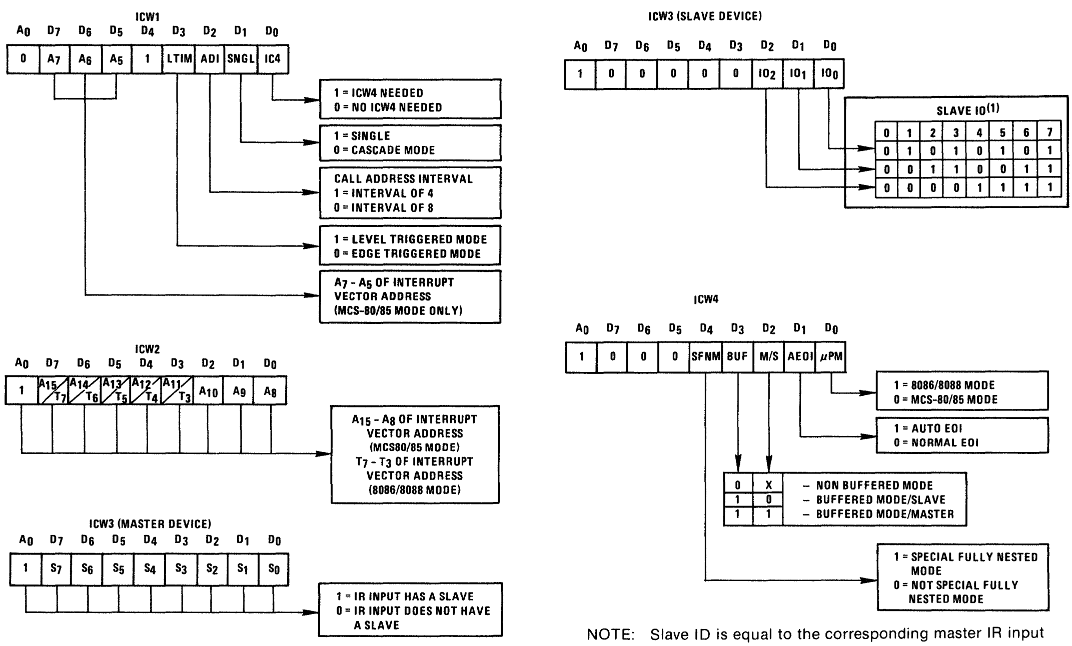
FIGURE 4. ICW1 FORMAT

D7 thru D5 - A7, A6, A5: These bits are used in the 8080/85 mode to form a portion of the low byte call address. When using the 4 byte address interval, all 3 bits are utilized. When using the 8 byte interval, only bits A7 and A6 are used. Bit A5 becomes a "don't care" bit. If using an 80C86(80C88) system, the value of these bits can be set to either a one or zero.

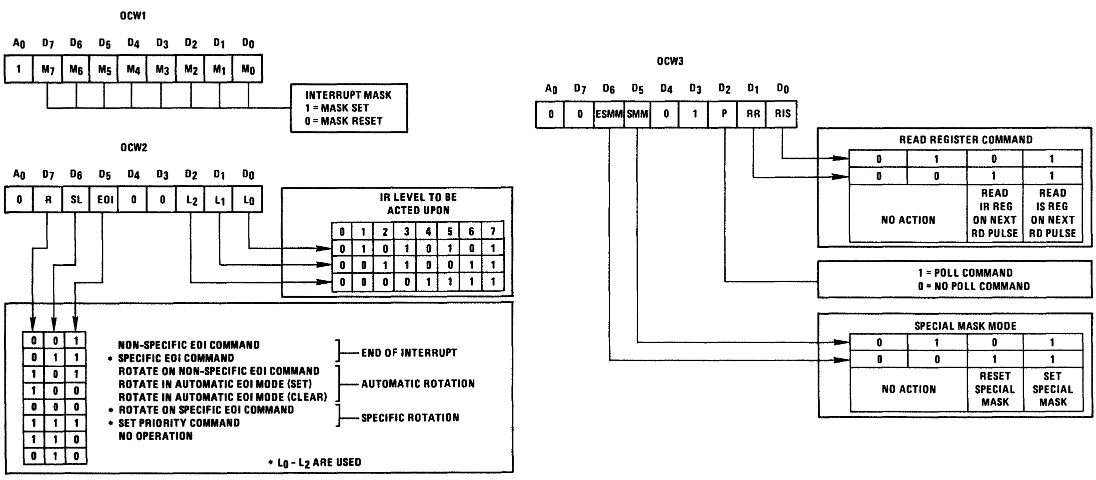
D3 - LTIM:

0: The 82C59A will operate in an edge triggered mode. An interrupt request on one of the IR lines (IR0 - IR7) is recognized by a low to high transition on the pin. The IR signal must remain high at least until the falling edge of the first $\overline{\text{INTA}}$ pulse. Subsequent interrupts on the IR pin(s) will not occur until another low-to-high transition occurs.

1: Sets up the 82C59A to operate in the level triggered mode. Interrupts occur when a "high" level is detected on one or more of the IR pins. The interrupt request must be removed from this pin before the EOI command is issued by the CPU. Otherwise, the 82C59A will see the IR line still in a high state, and consider this to be another interrupt request.



82C59A INITIALIZATION COMMAND WORD FORMAT



82C59A OPERATION COMMAND WORD FORMAT

D2 - ADI: Call Address Interval (for 8080/8085 use only). If using the 82C59A in an 80C86/88 based system, the value of this bit can be either a 0 or a 1.

0 : The address interval generated by the 82C59A is 8 bytes. This option provides compatiblity with the RST interrupt vectoring in 8080/8085 systems since the vector locations are 8 bytes apart. This vector will be combined with the values specified in bits D7 and D6 of ICW1. The addresses generated are shown in Table 1.

TABLE 1. ADDRESS INTERVAL (8 BYTES)

D7	D6	D5	D4	D3	D2	D1	D0	
A7	A6	1	1	1	0	0	0	IR7
A7	A6	1	1	0	0	0	0	IR6
A7	A6	1	0	1	0	0	0	IR5
A7	A6	1	0	0	0	0	0	IR4
A7	A6	0	1	1	0	0	0	IR3
A7	A6	0	1	0	0	0	0	IR2
A7	A6	0	0	1	0	0	0	IR1
A7	A6	0	0	0	0	0	0	IR0

1 : The address interval generated by the interrupt controller will be 4 bytes. This provides the user with a compact jump table for 8080/8085 systems. The interrupt number is effectively multiplied by four and combined with bits D7, D6 and D5 to form the lower byte of the call instruction generated and sent to the 8080 or 8085. Table 2 shows how these addresses are generated for the various Interrupt request (IR) levels.

TABLE 2. ADDRESS INTERVAL (4 BYTES)

D7	D6	D5	D4	D3	D2	D2	D0	
A7	A6	A5	1	1	1	0	0	IR7
A7	A6	A5	1	1	0	0	0	IR6
A7	A6	A5	1	0	1	0	0	IR5
A7	A6	A5	1	0	0	0	0	IR4
A7	A6	A5	0	1	1	0	0	IR3
A7	A6	A5	0	1	0	0	0	IR2
A7	A6	A5	0	0	1	0	0	IR1
A7	A6	A5	0	0	0	0	0	IR0

D1 - SNGL:

0 : This tells the 82C59A that more than one 82C59A is being used in the system, and it should expect to receive ICW3 following ICW2. How the particular 82C59A is being used in the system will be determined either through ICW4 for buffered mode, or through the $\overline{SP}/\overline{EN}$ pin for non-buffered mode operation.

1 : Tells the 82C59A that it is being used alone in the system. Therefore, there will be no need to issue ICW3 to the device.

D0 - IC4: Specifies to the 82C59A whether or not it can expect to receive ICW4. If this device is being used in an 80C86/ 80C88 system, ICW4 must be issued.

0 : ICW4 will not be issued. Therefore, all of the parameters associated with ICW4 will default to the zero (0) state. This should only be done when using the 82C59A in an 8080 or 8085 based system.

1 : ICW4 will be issued to the 82C59A.

2.2 ICW2:

ICW2 is the second control word that must be sent to the 82C59A. This byte is used in one of two ways by the 82C59A, depending on whether it is being used in an 8080/85 or an 80C86/88 based system.

When used in conjunction with the 8080/85 microprocessor, the value given to this register is taken as being the high byte of the address in the CALL instruction sent to the CPU.

D7	D6	D5	D4	D3	D2	D1	D0
A15	A14	A13	A12	A11	A10	A9	A8

FIGURE 5. ICW2 FORMAT

In an 80C86- or 80C88-based system, ICW2 is used to send the processor an interrupt vector. This vector is formed by taking the value of bits D7 through D3 and combining them with the interrupt request level to get an eight bit number. The processor will multiply this number by four and go to that absolute location in memory to find a starting address for the interrupt service routine corresponding to the interrupt request.

For example, if we set ICW2 to "00011000" and an interrupt is recognized on IR1, the vector sent to the 80C86(80C88) will be 00011001 (19H). The processor will then look to the memory location 64H to find the starting address of the corresponding interrupt service routine. It is the responsibility of the software to provide this address in the interrupt table.

D7	D6	D5	D4	D3	D2	D1	D0
A7	A6	A5	A4	A3	X	X	X

FIGURE 6. ICW2 FORMAT (80C86 MODE)

2.3 ICW3:

ICW3 is only issued when the SNGL bit in ICW1 has been set to zero. If not set, the next word written to the 82C59A will be interpreted as ICW4 if A0 = 1 and IC4 from ICW4 was set to one, or it could see it as one of the Operation Command Words based upon the state of the A0 line.

Like ICW2, this control word can be interpreted in two ways by the 82C59A. However the interpretation of this word depends on whether the 82C59A is being used as a "master" or a "slave" in the system. The definition of the particular devices role in the system is assigned through ICW4 (which will be discussed later), or through the state of the $\overline{SP}/\overline{EN}$ pin (pin 16).

82C59A as a MASTER:

If the given 82C59A is being used as a master, the eight (8) bits in this command word are used to indicate which of the IR lines are being driven by a slave 82C59A.

D7	D6	D5	D4	D3	D2	D1	D0
S7	S6	S5	S4	S3	S2	S1	S0

FIGURE 7. ICW3 FORMAT (MASTER)

D7 thru D0:

- 0 : The corresponding IR line to this bit is not being driven by a slave 82C59A. This line can however then be connected to the interrupt output of another interrupting device such as a UART. If there are unused bits in this byte because not all eight of the IR lines are used, set them to zero.
- 1 : The corresponding IR line to this bit is being driven by a slave 82C59A.

The bits in this command word are directly related to the IR lines. For example, to tell the 82C59A that there is a slave device connected to IR5 (pin 23), bit D5 of the command word should be set to a one (1).

82C59A as a SLAVE device:

When the device is being used as a slave device, we must use ICW3 to inform itself as to which IR line it will be connected to in the master. Therefore, only the three (3) least significant bits of ICW3 will be used to specify this value.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	IO2	IO1	IO0

FIGURE 8. ICW3 FORMAT (SLAVE)

These bits are coded as follows:

TABLE 3. SLAVE 'IDENTIFICATION' WITH ICW3

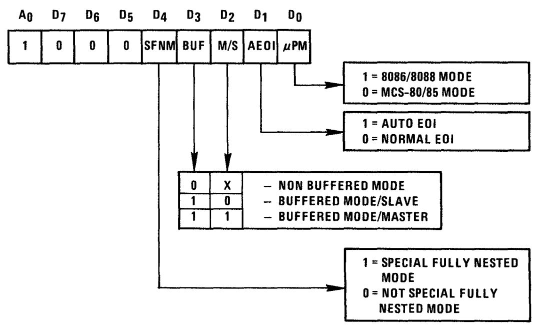
MASTER IR number	IO2	IO1	IO0
IR7	1	1	1
IR6	1	1	0
IR5	1	0	1
IR4	1	0	0
IR3	0	1	1
IR2	0	1	0
IR1	0	0	1
IR0	0	0	0

For example, if the INT output of a "slave" 82C59A is connected to the input pin IR5 on the "master" 82C59A, ICW3 of the "slave" would be programmed with the value 00000101b, or 05H. This informs the "slave" as to which priority level it holds with the "master".

D7 thru D3: These bits must be set to zeros (0) for proper operation of the device.

2.4 ICW4:

This control register is written to only when the IC4 bit is set in ICW1. The purpose of this command word is to set up the 82C59A to operate in a mode other than the default mode of operation. The default mode of operation is the same as if a value of 00H were to be written to ICW4 (i.e. all bits set to zero).



NOTE: Slave IO is equal to the corresponding master IR input

FIGURE 9. ICW4 FORMAT

D7 thru D5: These bits must be set to zero for proper operation.

D4 - SFNM: This bit is used in the selection of the Special Fully Nested Mode (SFNM) of operation. This mode should only be used when multiple 82C59As are cascaded in a system. It needs only to be programmed in the Master 82C59A in the system.

- 0 : Special Fully Nested Mode is not selected.
- 1 : Special Fully Nested Mode is selected.

D3 - BUF: This bit tells the 82C59A whether or not the outputs from the data pins (D0 - D7) will be buffered. If they are buffered, this bit will cause the $\overline{SP}/\overline{EN}$ pin to become an output signal that can be used to control the "enable" pin on a buffering device(s).

0 : The device will be used in a non-buffered mode. Therefore, (1) the M/S bit in ICW4 is a don't care, and (2) the $\overline{SP}/\overline{EN}$ pin becomes an input pin telling the device if it is being used as a master (pin 16 = High) or a slave (pin 16 = Low). For systems using a single 82C59A, the $\overline{SP}/\overline{EN}$ input should be tied high.

1 : The device is used in buffered mode. An enable output signal will be generated on pin 16, and the M/S bit will be used for determining whether the particular 82C59A is a "master" or a "slave".

D2 - M/S: This bit is of significance only when the BUF bit is set (BUF = 1). The purpose of this bit is to determine whether the particular 82C59A is being used as a "master" or a "slave" in the target system.

0 : The 82C59A is being used as a slave.

1 : The 82C59A is the master interrupt controller in the system.

D1 - AEOI: This bit is used to tell the 82C59A to automatically perform a non-specific End-of-Interrupt on the trailing edge of the last Interrupt Acknowledge pulse. Users should note that when this is selected, the nested priority interrupt structure is lost.

0 : Automatic End-of-Interrupt will not be generated.

1 : Automatic End-of-Interrupt will be generated on the trailing edge of the last Interrupt Acknowledge pulse.

D0 - μPM: This bit tells the Interrupt Controller which microprocessor is being used in the system. An 8080/8085, or an 80C86/80C88.

0 : The 82C59A will be used in an 8080/8085 based system.

1 : 82C59A to be used in the 80C86/88 mode of operation.

3.0 Operation Command Words

Once the Initialization Command Words, described in the previous section, have been written to the 82C59A, the device is ready to accept interrupt requests. While the 82C59A is operating, we have the ability to select various options that will put the device in different operating modes, by writing Operation Command Words (OCWs) to the 82C59A. These OCWs can be sent at any time after the device has been initialized and in any order. These words can be changed at any time as well. Note: If A0 = 0 and D4 of the command word = 1, the 82C59A will begin the ICW initialization sequence.

There are three different OCWs for the 82C59A. Each has a different purpose. The first control word (OCW1) is used for masking out interrupt lines that are to be inactive or ignored during operation. OCW2 is used to select from various priority resolution algorithms in the device. Finally, OCW3 is used for (1) controlling the Special Mask Mode, and (2) telling the 82C59A which Register will be read on the next RD pulse; the ISR (In-service Register) or the IRR (Interrupt Request Register).

3.1 OCW1:

This control word is used to set or clear the masking of the eight (8) interrupt lines input to the 82C59A. This control word performs this function via the Interrupt Mask Register (IMR). In it's initial state, the value of this register is 00H. In other words, all of the interrupt lines are enabled. Therefore, we need only write this control word when we wish to disable specific interrupt lines.

A direct mapping occurs between the bits in this control word and the actual interrupt pins on the device. For example bit 7 (D7) controls interrupt line IR7 (pin 25), bit 6 controls IR6, and so on.

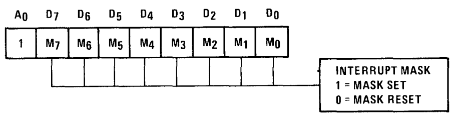


FIGURE 10. OCW1 FORMAT

Even though the user can mask off any of the IR lines, any interrupt occuring during that time will not be lost. The request for an interrupt is retained in the IRR; therefore when that IR is unmasked by issuing a new mask value to OCW1, the interrupt will be generated when it becomes the highest requesting priority.

D7 thru D0:

0 : When any of the bits in the control word are reset (0), the corresponding interrupt is enabled.

1 : By setting a bit(s) to a one in the control word, the corresponding interrupt line(s) is disabled.

For example, if the value 34H (00110100b) were written to OCW1, interrupts would be disabled from being serviced on lines IR2, IR4 and IR5.

3.2 OCW2:

In ICW4 bit D1 was used to specify whether the 82C59A should wait for an EOI (End of Interrupt) from the CPU, or generate its own EOI (Automatic EOI) . If bit D1 of ICW4 had been programmed to be a zero, OCW2 would be used for sending the EOI to the 82C59A. Conversely, if this bit had been set to a one, OCW2 would be used for specifying whether or not the 82C59A should perform a priority rotation on the interrupts when the AEOI is detected.

OCW2 has several EOI options. The EOI issued can be either specific or non-specific. For each of these EOIs, the user can specify whether or not priority rotation should be performed.

D7	D6	D5	D4	D3	D2	D1	D0
R	SL	EOI	0	0	L2	L1	L0

FIGURE 11.

R, SL, and EOI:

These three bits are used for specifying how the device should handle AEOIs, or for issuing one of several different EOIs. They are programmed as shown in the following table:

TABLE 4. ROTATE AND EOI MODES

R	SL	EOI	
0	0	1	Non-specific EOI command
0	1	1	* Specific EOI command
1	0	1	Rotate on non-specific EOI command
1	0	0	Rotate in Automatic EOI mode (set)
0	0	0	Rotate in Automatic EOI mode (clear)
1	1	1	Rotate on specific EOI command
1	1	0	* Set priority command
0	1	0	* No operation

*L0 - L2 are used

L2, L1, and L0:

These three bits of the control word are used in conjunction with the issuance of specific EOIs or when specifically establishing a different priority structure. The bits tell the 82C59A which interrupt level is to be acted upon. Therefore, the software needs to know which interrupt is being serviced by the 82C59A.

TABLE 5. INTERRUPT LEVEL TO ACT UPON

L2	L1	L0	
0	0	0	IR level 0
0	0	1	IR level 1
0	1	0	IR level 2
0	1	1	IR level 3
1	0	0	IR level 4
1	0	1	IR level 5
1	1	0	IR level 6
1	1	1	IR level 7

3.3 OCW3:

There are two main functions that OCW3 controls: (1) Interrupt Status, and (2) Interrupt Masking. Interrupt status can be checked by looking at the ISR or IRR registers, or by issuing a Poll Command to manually identify the highest priority interrupt requesting service.

D7	D6	D5	D4	D3	D2	D1	D0
0	ESMM	SMM	0	1	P	RR	RIS

FIGURE 12.

D7: Must be set to zero for proper operation of the 82C59A.

D6 - ESMM: Enable Special Mask Mode - The ESMM bit when enabled allows the SMM bit to set or clear the Special Mask Mode. When disabled, this bit causes the SMM bit to have no effect on the 82C59A.

0 : Disables the effect of the SMM bit.

1 : Enable the SMM bit to control the Special Mask Mode.

D5 - SMM: Special Mask Mode - The SMM bit isd used to enable or disable the Special Mask Mode. This bit will only affect the 82C59A when the ESMM bit is set to 1.

0 : Disable the Special Mask Mode.

1 : Put the 82C59A into the Special Mask Mode.

D4, D3: These bits are used to differentiate between OCW2, OCW3 and ICW1. To properly select OCW3, D4 must be set to zero and D3 must be set to one.

D2 - P: Poll Command - This bit is used to issue the poll command to the 82C59A. The next read of the 82C59A will cause a poll word to be returned which tells if an interrupt is pending, and if so, which is the highest requesting level.

NOTE: The poll command must be issued each time the poll operation is desired.

0 : No poll command issued to the 82C59A.

1 : Issue the poll command.

D1 - RR: Read Register - This bit is used to execute the "read register" command. When this bit is set, the 82C59A will look at the RIS bit to determine whether the ISR or IRR register is to be read. When issuing this command, the next instruction executed by the CPU should be an input from this same port to get the contents of the specified register.

0 : No "Read Register" command will be performed.

1 : The next input instruction by the CPU will read either the contents of the ISR or the IRR as specified by the RIS bit.

D0 - RIS: This bit is used in conjunction with the RR bit to select which register is to be read when the "Read Register" command is issued.

0 : The next input instruction will read the contents of the Interrupt Request Register (IRR).

1 : The next input instruction will read the contents of the In-Service Register (ISR).

The two registers that can be accessed through the Read Register command are used to determine which interrupts are requesting service, and which one(s) are currently being serviced.

The IRR bits get set when corresponding Interrupt requests are received. For instance, when IR4 is detected, bit D4 of the IRR will get set. When an interrupt acknowledge comes back from the CPU, the priority resolution logic will determine which interrupt request will be serviced. The corresponding bit in the In-service Register (ISR) will then be set. Clearing of the correct bits in the ISR occurs through out use of the AEOI, or by issuing an EOI to the device.

4.0 Addressing the 82C59A

There are two factors that must be taken into account when addressing the 82C59A in a system. To begin with, the 82C59A is accessed only when the $\overline{CS}$ pin (chip select) sees an active signal (low). This signal is generated using control circuitry in the system. Secondly, the various registers within the 82C59A are selected based upon the state of the A0 (address pin) as well as specific bits in the command words (i.e for ICW1, OCW2, and OCW3 A0 must be a zero).

The circuit in Figure 13 shows that the $\overline{CS}$ signal is generated using an HPL-82C338 Programmable Chip Select Decoder (PCSD). This device is being used as a 3-to-8 decoder. Note that the Gx inputs to the 82C338 have been programmed to be active low. The A, B, and C inputs to the 82C338 correspond to address lines AD2, AD3 and AD4 respectively, from the 80C88. The A0 input to the 82C59A is also taken from the CPUs address bus; AD0 is used. It should be noted that address line AD1 from the 80C88 is not being used in the addressing of this particular peripheral. This is done to allow other peripheral devices that require two address inputs for internal register selection, to use address lines AD0 and AD1 from the processor.

Because the AD1 address line from the 80C88 is not being used, the 82C59A will be addressed regardless of whether AD1 is high or low (1 or 0). The remainder of the address lines from the 80C88 can either be a zero or one when addressing the 82C59A. For the examples to be presented, it can be assumed that all unused address lines will be set to zero when addressing the 82C59A.

In Figure 13, output $\overline{Y6}$ from the HPL-82C338 is being used as the $\overline{CS}$ input to the 82C59A. This line is enabled when the inputs on A, B, and C are: A = 0, B = 1, and C = 1. Combining this with the A0 input to the 82C59A, we get the addresses 18H and 19H for accessing the 82C59A.

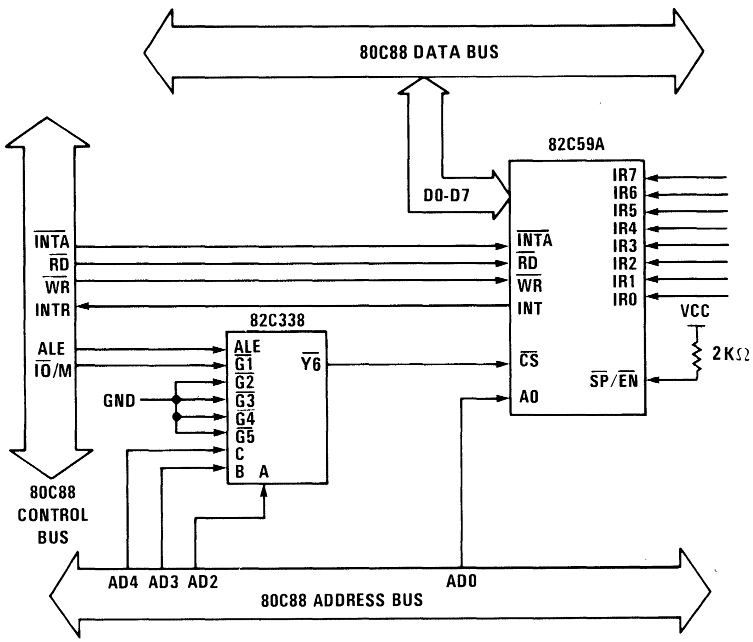


FIGURE 13. ADDRESSING THE 82C59A

5.0 Programming the 82C59A

As described earlier, there are two different types of command words that are used for controlling 82C59A operation; the Initialization Command Words (ICWs) and the Operation Command Words (OCWs). To properly program the 82C59A, it is essential that the ICWs be written first. When writing the ICWs to the 82C59A, they must be written in the following sequence:

(1) Write ICW1 to the 82C59A, A0 = 0.

(2) Write ICW2 to the 82C59A, A0 = 1.

(3) If using cascaded 82C59As in system, write ICW3 to the 82C59A, A0 = 1.

(4) If IC4 bit was set in ICW1, write ICW4 to the 82C59A.

NOTE: When using multiple 82C59As in the system (cascaded), each one must be initialized following the above sequence.

Once the 82C59A(s) has been configured through the ICWs, the OCWs can be used to select from the various operation mode options. These include: masking of interrupt lines, selection of priority rotation, issuance of EOIs, reading of the ISR andsor IRR, etc. These OCWs can be written to the 82C59A at any time during operation of the 82C59A. The various command words are identified by the state of selected bits in the words, rather than by the sequence that they are written to the 82C59A; as with the ICWs. Therefore, it is imperative that the fixed bit values in the command words be written as such to insure proper operation of the device(s).

5.1 Example 1: Single 82C59A

In Example 1, we are using a single 82C59A in a system to handle the interrupts caused by an HD-6406 Programmable Asynchronous Communications Interface. The system is driven using an 80C86 Microprocessor. The system configuration is shown in Figure 14. An assembly language listing for the software controlling this system can be found in Program Listing, Example 1, on page 15.

Interrupts are initiated by the HD-6406 anytime it receives data on its Serial Data In pin (SDI), or when it is ready to transmit more data via its Serial Data Out pin (SDO).

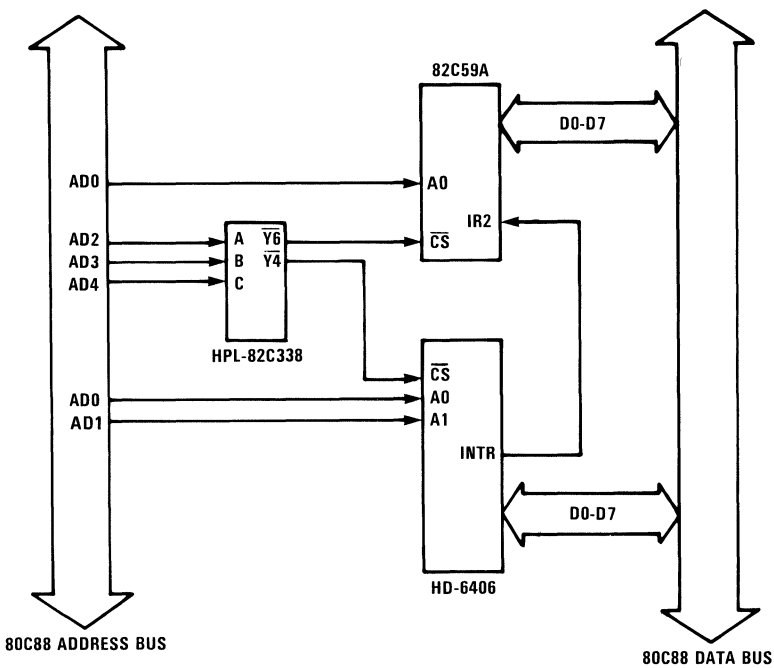


FIGURE 14. EXAMPLE 1: SINGLE 82C59A

5.2 Example 2: Cascaded 82C59As

Example 2 illustrates how we can use multiple 82C59As in Cascade Mode. Figure 15 shows the interconnections between the master and slave interrupt controllers. In this example, only one interrupt can occur. This is generated by the HD-6406 PACI. Except for the fact that this system is configured with a Master-Slave interrupt scheme, it is the same as that in Example 1. The software for this system is given in Program Listing, Example 2, on Page 20.

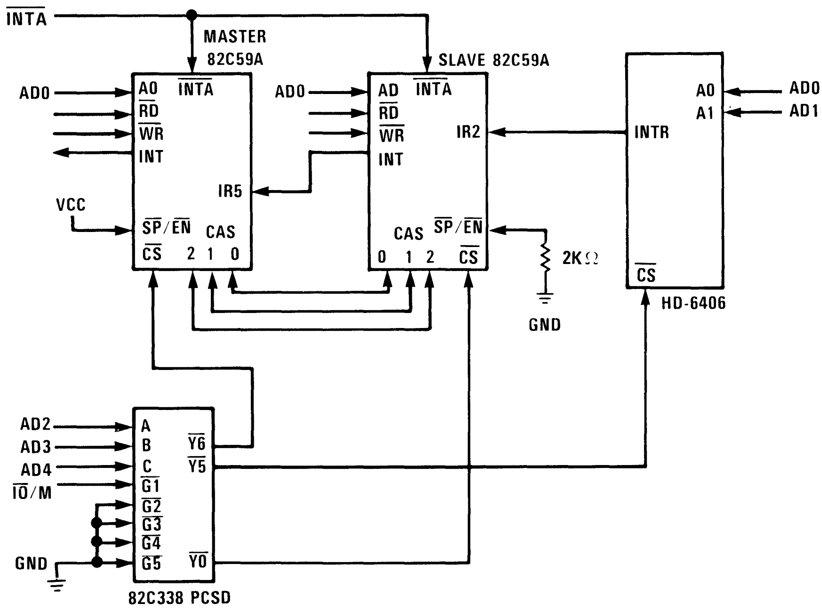


FIGURE 15. EXAMPLE 2: CASCADED 82C59As

6.0 Expansion Past 64 Interrupts

In some instances, it may be desirable to expand the number of available interrupts in a system past the maximum of 64 imposed when using cascaded 82C59As. The easiest way to accomplish this is through the use of the Poll command with the 82C59A. Figure 16 illustrates one example of how this expansion can be accomplished. Notice that we are using two 3-to-8 decoders (HPL-82C338 PCSDs) to address up to 16 82C59As. Selection of which decoder is active takes place using the G2 pin on the HPL-82C338. For one HPL-82C338, G2 has been programmed to be active low ($\overline{G2}$), while the other HPL-82C338 has been programmed for G2 to operate active high. This G2 input is driven by AD5 from the CPU's address bus.

With this type of interrupt structure, we are not using the INT and $\overline{INTA}$ lines from our processor (80C88 for this example). Because of this, no interrupts will break execution of the system software. Therefore, it is the task of the software to poll the various 82C59As in the system to see if any interrupts are pending. Once it has been established which interrupt requires servicing, the software can take appropriate action.

There are disadvantages to using the poll mode for the systems interrupt structure: (1) the overhead of polling each of the 82C59As reduces the systems efficiency, and (2) real-time interrupt servicing cannot be guaranteed.

There are several advantages to using the poll mode in this manner: (1) there can be more than 64 priority interrupts in the system, and (2) memory in the system is freed because no interrupt vector table is required.

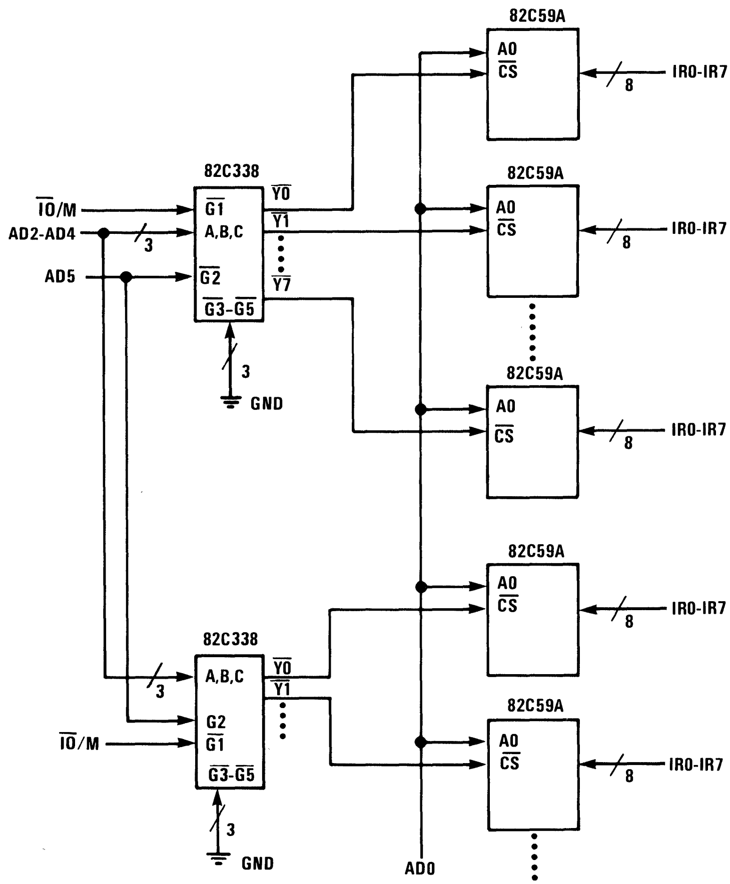


FIGURE 16. EXPANDING PAST 64 INTERRUPTS

PROGRAM LISTING, EXAMPLE 1

```
NAME            EXAMPLE_1
;  *************************************************************************
;  HARRIS SEMICONDUCTOR                                          AUG 5, 1985
;  P.O. Box 883
;  Melbourne, FL  32901
;
;  Microprocessor Applications
;  JAGoss
;
;  EXAMPLE #1:     System with a single 82C59A
;
;  *************************************************************************


;  The following are port addresses for the devices used in our example
;  system.  The devices that we will look at are the HD-6406 PACI, and the
;  two 82C59A Interrupt Controller.

;  ------ 6406 Register Addresses ------

UCR             EQU     11H             ;UART control register
BRSR            EQU     13H             ;Baud Rate Select Register
MCR             EQU     12H             ;Modem Control Register
USR             EQU     11H             ;UART Status Register
MSR             EQU     13H             ;Modem Status Register
TBR             EQU     10H             ;Transmit Buffer Register
RBR             EQU     10H             ;Receive Buffer Register

;  --------- 82C59A Addresses ----------

ICW1            EQU     18H
ICW2            EQU     19H
ICW4            EQU     19H
OCW1            EQU     19H
OCW2            EQU     18H

CARRIAGE_RETURN EQU     0DH
LINE_FEED       EQU     0AH
DR              EQU     80H             ;Mask for checking DATA READY
TBRE            EQU     40H             ;Mask for checking TRANSMIT BUFFER
                                        ;  REGISTER EMPTY


ASSUME          CS:DRIVER_59A,
&               DS:BUFFER_AREA,
&               SS:STACK_AREA
```

PROGRAM LISTING, EXAMPLE 1

```
DRIVER_59A      SEGMENT         PUBLIC
; ****************************************************************
; *                              MAIN                            *
; ****************************************************************

MAIN            PROC    NEAR

SET_UP:         MOV     AX,BUFFER_AREA  ;Set up the data segment
                MOV     DS,AX
                MOV     AX,STACK_AREA   ;Set up the stack segment
                MOV     SS,AX
                                        ;Set up the stack pointer
                MOV     SP,OFFSET STACK_AREA:TOP_OF_STACK

;  Set up the interrupt vector table

                MOV     AX,OFFSET INT_SERVICE_ROUTINE
                MOV     ISR_34,AX
                MOV     ISR_34[2],CS

;  Initialize the pointer into the data buffer.

                MOV     BX,OFFSET BUFFER
                XOR     DI,DI           ;Clear the index register

;  Initialize the 82C59A

                CALL    INIT_82C59A

;  Initialize the HD-6406 PACI

                CALL    INIT_6406

;  Wait for interrupts from the '59A...

                STI                     ;Set the interrupt enable flag.
WAIT_LOOP:      NOP
                JMP     WAIT_LOOP

                HLT
MAIN            ENDP
```

PROGRAM LISTING, EXAMPLE 1

```
INIT_82C59A     PROC    NEAR
; ***************************************************************
; *                     INIT_82C59A                           *
; ***************************************************************

;  We first want to write ICW1.  This will be used to set the
;  device for edge triggered interrupt detection and for use
;  in Single Mode.

BEGIN_59A:      MOV     AL,00010000B    ;Edge triggered, and single mode
                OUT     ICW1,AL

;  Now we will write out ICW2.  This gives the 59A information
;  about where to branch to in the interrupt table.

                MOV     AL,00100000B
                OUT     ICW2,AL

;  The final control word that is written in this sequence is ICW4.
;  This is used to specify that the device is to operate in 80C86/80C88
;  mode, with normal EOI's generated through software, and non-buffered
;  outputs are being fed back to the CPU.

                MOV     AL,00000001B
                OUT     ICW4,AL

;  To insure that interrupts will only be issued by the HD-6406 PACI,
;  we will write out an interrupt mask to the register OCW1.  This
;  mask will only allow interrupts from the specified lines.  In this
;  case on IR2 only, all others will be disabled.

                MOV     AL,11111011B    ;A zero in a bit means that the
                OUT     OCW1,AL         ; corresponding IR lines is enabled.

                RET
INIT_82C59A     ENDP


INIT_6406       PROC    NEAR
; ***************************************************************
; *                      INIT_6406                            *
; ***************************************************************

;  This routine sets up the HD-6406 to communicate with a dumb
;  terminal.  The device will generate an interrupt whenever
;  a key is pressed at the terminal.
```

PROGRAM LISTING, EXAMPLE 1

```
;  Set up for 8 data bits, 1 stop bit, and no parity.

BEGIN_6406:     MOV     AL,00111110B
                OUT     UCR,AL

;  Set up BRSR for 9600 bps, assuming that the target system uses
;  a 2.4576 MHz clock crystal.

                MOV     AL,00000110B
                OUT     BRSR,AL

;  Enable interrupts on the 6406, enable the receiver, and
;  select normal mode.

                MOV     AL,00100100B
                OUT     MCR,AL

                RET                             ;Return to the MAIN
INIT_6406       ENDP



INT_SERVICE_ROUTINE     PROC    NEAR
; ****************************************************************
; *                     INT_SERVICE_ROUTINE                      *
; ****************************************************************

ISR_START:      IN      AL,USR                  ;Find out what caused the interrupt.
                TEST    AL,DR                   ;Was it DATA READY ?
                JNZ     READ_DATA
                TEST    AL,TBRE                 ;Was it TRANSMIT BUFFER REG. EMPTY ?
                JNZ     PRINT_BUFFER            ;If so, then print next character

;  If this condition was not detected, then we have an erroneous
;  interrupt from the HD-6406.  Rather than servicing this, we will
;  simply return from the service routine to the MAIN.

ERROR:          JMP     ISR_EXIT

;  Read the data that is present in the Receive Buffer Register.

READ_DATA:      IN      AL,RBR
                MOV     [BX][DI],AL             ;Save the data in our buffer area.
                INC     DI                      ;Increment the index into the buffer.
                CMP     AL,CARRIAGE_RETURN
                JE      PRINT_LF

                JMP     ISR_EXIT                ;Exit the service routine.

;  Set up for writing the data out to the Transmit Buffer...

PRINT_LF:       MOV     AL,LINE_FEED
                MOV     [BX][DI],AL             ;Add a line feed to the buffer.
```

PROGRAM LISTING, EXAMPLE 1

```
                INC     DI
                OUT     TBR,AL
                MOV     CX,DI           ;Load tne buffer size into CX
                XOR     DI,DI           ;Set the index back to beginning
                                        ;  of the buffer.
                JMP     ISR_EXIT

;  Print out the contents of the buffer...

PRINT_BUFFER:   CMP     CX,0            ;Anything to print ?
                JNE     PRINT_CHAR      ;If so, then print it...
                JMP     ISR_EXIT        ;Else, ignore this interrupt...
PRINT_CHAR:     MOV     AL,[BX][DI]     ;Print the byte pointed to in buffer.
                OUT     TBR,AL
                INC     DI              ;Point to next character.
                LOOP    PRINT_CHAR      ;Print til end-of-buffer.

DONE_PRINTING:  XOR     DI,DI           ;Re-initialize pointer into buffer.

;  Exit from the service routine, sending out a non-specific EOI first.

ISR_EXIT:       MOV     AL,00100000B    ;Send out an End-of-Interrupt
                OUT     OCW2_S,AL       ;  to both master and slave.
                OUT     OCW2_M,AL
                IRET

INT_SERVICE_ROUTINE     ENDP
DRIVER_59A              ENDS


BUFFER_AREA     SEGMENT         PUBLIC
; **************************************************************
; *                          BUFFER_AREA                       *
; **************************************************************

                ORG     88H
ISR_34          DW      4 DUP(?)

                ORG     100H
BUFFER          DB      80 DUP(?)
BUFFER_AREA     ENDS


STACK_AREA      SEGMENT         PUBLIC
; **************************************************************
; *                          STACK_AREA                        *
; **************************************************************

STACK           DW      80H DUP(?)
TOP_OF_STACK    LABEL   WORD
STACK_AREA      ENDS
                END
```

PROGRAM LISTING, EXAMPLE 2

```
NAME            EXAMPLE_2
; ****************************************************************************
;  HARRIS SEMICONDUCTOR                                          AUG 27, 1985
;  P.O. Box 883
;  Melbourne, FL  32901
;
;  Microprocessor Applications
;  JAGoss
;
;  EXAMPLE #2:
;  Configure the system for two 82C59As (MASTER/SLAVE).  Interrupts are
;  generated for the slave by an HD-6406 PACI.
;
; ****************************************************************************

;  The following are port addresses for the devices used in our example
;  system.  The devices that we will look at are the HD-6406 PACI, and the
;  two 82C59A Interrupt Controllers.

;  ------ 6406 Register Addresses ------

UCR             EQU     11H             ;UART control register
BRSR            EQU     13H             ;Baud Rate Select Register
MCR             EQU     12H             ;Modem Control Register
USR             EQU     11H             ;UART Status Register
MSR             EQU     13H             ;Modem Status Register
TBR             EQU     10H             ;Transmit Buffer Register
RBR             EQU     10H             ;Receive Buffer Register

;  --------- 82C59A Addresses ----------

ICW1_M          EQU     18H             ;MASTER Interrupt Controller
ICW2_M          EQU     19H
ICW3_M          EQU     19H
ICW4_M          EQU     19H
OCW1_M          EQU     19H
OCW2_M          EQU     18H

ICW1_S          EQU     0H              ;SLAVE Interrupt Controller
ICW2_S          EQU     1H
ICW3_S          EQU     1H
ICW4_S          EQU     1H
OCW1_S          EQU     1H
OCW2_S          EQU     0H

CARRIAGE_RETURN EQU     0DH
LINE_FEED       EQU     0AH
DR              EQU     80H             ;Mask for checking DATA READY
TBRE            EQU     40H             ;Mask for checking TRANSMIT BUFFER
                                        ;  REGISTER EMPTY

ASSUME          CS:DRIVER_59A,
&               DS:BUFFER_AREA,
&               SS:STACK_AREA
```

PROGRAM LISTING, EXAMPLE 2

```
DRIVER_59A      SEGMENT         PUBLIC
; ************************************************************
; *                            MAIN                          *
; ************************************************************

MAIN            PROC    NEAR

SET_UP:         MOV     AX,BUFFER_AREA  ;Set up the data segment
                MOV     DS,AX
                MOV     AX,STACK_AREA   ;Set up the stack segment
                MOV     SS,AX
                                        ;Set up the stack pointer
                MOV     SP,OFFSET STACK_AREA:TOP_OF_STACK

;  Set up the interrupt vector table

                MOV     AX,OFFSET INT_SERVICE_ROUTINE
                MOV     ISR_34,AX
                MOV     ISR_34[2],CS

;  Initialize the pointer into the data buffer.

                MOV     BX,OFFSET BUFFER
                XOR     DI,DI           ;Clear the index register

;  Initialize the 82C59A

                CALL    INIT_82C59A

;  Initialize the HD-6406 PACI

                CALL    INIT_6406

;  Wait for interrupts from the '59A...

                STI                     ;Set the interrupt enable flag.
WAIT_LOOP:      NOP
                JMP     WAIT_LOOP

                HLT
MAIN            ENDP
```

PROGRAM LISTING, EXAMPLE 2

```
INIT 82C59A      PROC     NEAR
; ***********************************************************
; *                        INIT_82C59A                       *
; ***********************************************************

; -------------------- Configure the MASTER --------------------

;  We first want to write ICW1.  This will be used to set the
;  device for edge triggered interrupt detection and for use
;  in Cascade Mode.

BEGIN_59A:       MOV      AL,00010001B     ;Edge triggered, and cascade mode
                 OUT      ICW1_M,AL

;  Now we will write out ICW2.  This gives the 59A information
;  about where to branch to in the interrupt table.  In this example
;  however, this value is not used.  Interrupts will only be generated
;  by the slave 82C59A.

                 MOV      AL,00000000B
                 OUT      ICW2_M,AL

;  Write out ICW3 to the MASTER.  This tells the master which IR lines
;  have slaves connected to them.  In this case, interrupts come from
;  the slave only on IR5.  All other lines are not used.

                 MOV      AL,00100000B     ;SLAVE is only on IR5.
                 OUT      ICW3_M,AL

;  The final control word that is written in this sequence is ICW4.
;  This is used to specify that the device is to operate in 80C86/88
;  mode, with normal EOI's generated through software, and non-buffered
;  outputs are being fed back to the CPU.

                 MOV      AL,00000001B
                 OUT      ICW4_M,AL

; -------------------- Configure the SLAVE --------------------

;  First, set up the slave for edge triggered interrupts, cascade mode
;  and tell it that ICW4 is to be issued.

                 MOV      AL,00010001B
                 OUT      ICW1_S,AL

;  Write ICW2 to the slave.  When an interrupt occurs, the 82C59A will take
;  this value, add to it the interrupt number (IR2 = 20H + 2 = 22H) and
;  sends it to the processor.  The processor will then multiply this number
;  by four (4) to generate the address in the Interrupt table to look for
;  the address of the Interrupt Service Routine.

                 MOV      AL,20H           ;IR2 from the slave will cause the
                 OUT      ICW2_S,AL        ; CPU to vector 88H.
```

PROGRAM LISTING, EXAMPLE 2

```
;  Tell the slave which IR line on the master it is connected to.

                MOV     AL,00000101B    ;It drives IR5...
                OUT     ICW3_S,AL

;  Set up the slave for normal EOI's, and 80C86/88 mode.

                MOV     AL,00000001B
                OUT     ICW4_S,AL

;  Set up the mask register for both the master and the slave...

                MOV     AL,11011111B    ;Interrupts recognized only on IR5
                OUT     OCW1_M,AL

                MOV     AL,11111011B    ;Interrupt recognized only on IR2
                OUT     OCW1_S,AL

                RET
INIT_82C59A     ENDP


INIT_6406       PROC    NEAR
; *****************************************************************
; *                           INIT_6406                           *
; *****************************************************************

;  This routine sets up the HD-6406 to communicate with a dumb
;  terminal.  The device will generate an interrupt whenever
;  a key is pressed at the terminal.

;  Set up for 8 data bits, 1 stop bit, and no parity.

BEGIN_6406:     MOV     AL,00111111B
                OUT     UCR,AL

;  Set up BRSR for 9600 bps, assuming that the target system uses
;  a 2.4576 MHz clock crystal.

                MOV     AL,00000110B
                OUT     BRSR,AL

;  Enable interrupts on the 6406, enable the receiver, and
;  select normal mode.

                MOV     AL,00100100B
                OUT     MCR,AL

                RET                     ;Return to the MAIN
INIT_6406       ENDP
```

PROGRAM LISTING, EXAMPLE 2

```
DONE_PRINTING:  XOR     DI,DI           ;Re-initialize pointer into buffer.

; Exit from the service routine, sending out a non-specific EOI first.

ISR_EXIT:       MOV     AL,00100000B    ;Send out an End-of-Interrupt
                OUT     OCW2_S,AL       ; to both master and slave.
                OUT     OCW2_M,AL
                IRET

INT_SERVICE_ROUTINE     ENDP
DRIVER_59A              ENDS


BUFFER_AREA     SEGMENT         PUBLIC
; ****************************************************************
; *                          BUFFER_AREA                         *
; ****************************************************************

                ORG     88H
ISR_34          DW      4 DUP(?)
                ORG     100H
BUFFER          DB      80 DUP(?)

BUFFER_AREA     ENDS


STACK_AREA      SEGMENT         PUBLIC
; ****************************************************************
; *                          STACK_AREA                          *
; ****************************************************************

STACK           DW      80H DUP(?)
TOP_OF_STACK    LABEL   WORD
STACK_AREA      ENDS
                END
```

PAGE

DATA COMMUNICATIONS FAMILY

HARRIS

HD-4702

CMOS Programmable Bit Rate Generator

Features

- HD-4702 Provides 13 Commonly Used Bit Rates
- Uses a 2.4576MHz Crystal/Input for Standard Frequency Output (16 Times Bit Rate)
- TTL Compatible — Output Will Sink 1.6mA
- Low Power Dissipation .... 4.5mW Typ. @ 2.4576MHz
- Conforms to EIA RS-404
- One HD-4702 Controls up to Eight Transmission Channels
- Initialization Circuit Facilitates Diagnostic Fault Isolation
- On-Chip Input Pull-Up Circuit

Description

The HD-4702 Bit Rate Generator provides the necessary clock signals for digital data transmission systems, such as a UART. It generates 13 commonly used bit rates using an on-chip crystal oscillator or an external input. For conventional operation generating 16 output clock pulses per bit period, the input clock frequency must be 2.4576MHz (i.e. 9600 Baud x 16 x 16, since there is an internal ÷ 16 prescaler). A lower input frequency will result in a proportionally lower output frequency.

The HD-4702 can provide multi-channel operation with a minimum of external logic by having the clock frequency CO and the ÷ 8 prescaler outputs Q_0, Q_1, Q_2 available externally. All signals have a 50% duty cycle except 1800 Baud, which has less than 0.39% distortion.

The four rate select inputs (S0-S3) select which bit rate is at the output (Z). Table 1 lists select code and output bit rate. Two of the 16 for the HD-4702 do not select an internally generated frequency, but select an input into which the user can feed either a different frequency, or a static level (High or Low) to generate "ZERO BAUD".

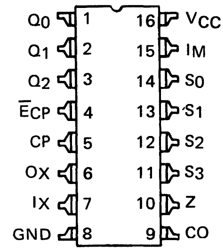
The bit rate most commonly used in modern data terminals (110, 150, 300, 1200, 2400 Baud) require that no more than one input be grounded for the HD-4702, which is easily achieved with a single 5-position switch.

The HD-4702 has an initialization circuit which generates a master reset for the scan counter. This signal is derived from a digital differentiator that senses the first high level on the CP input after the E_{CP} input goes low. When E_{CP} is high, selecting the crystal input, CP must be low. A high level on CP would apply a continuous reset. See Table 2.

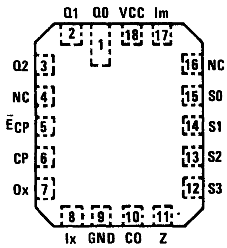
For the HD-4702, all inputs except I_X have on-chip pull-up circuits which provide TTL compatibility and eliminate the need to tie a permanently high input to V_{CC}.

Pinouts

TOP VIEW



LCC
TOP VIEW



Truth Tables

TABLE 1.
TRUTH TABLE FOR RATE SELECT INPUTS

S_3	S_2	S_1	S_0	OUTPUT RATE (Z)
L	L	L	L	MUX Input (I_M)
L	L	L	H	MUX Input (I_M)
L	L	I	L	50 Baud
L	L	H	H	75 Baud
L	H	L	L	134.5 Baud
L	H	L	H	200 Baud
L	H	H	L	600 Baud
L	H	H	H	2400 Baud
H	L	L	L	9600 Baud
H	L	L	H	4800 Baud
H	L	H	L	1800 Baud
H	L	H	H	1200 Baud
H	H	L	L	2400 Baud
H	H	L	H	300 Baud
H	H	H	L	150 Baud
H	H	H	H	110 Baud

NOTE: 1. 19200 Baud by connecting Q_2 to I_M.

TABLE 2.
CLOCK MODES AND INITIALIZATION

IX	ECP	CP	OPERATION
⊓⊓	H	L	Clocked from I_X
X	L	⊓⊓	Clocked from CP
X	H	H	Continuous Reset
X	L	⊓	Reset During 1st CP = High Time

NOTE: Actual output frequency is 16 times the indicated Output Rate, assuming a clock frequency of 2.4576MHz.

H = HIGH Level
L = LOW Level
X = Don't Care
⊓ = 1st HIGH Level Clock Pulse after E_{CP} goes LOW
⊓⊓ = Clock Pulse

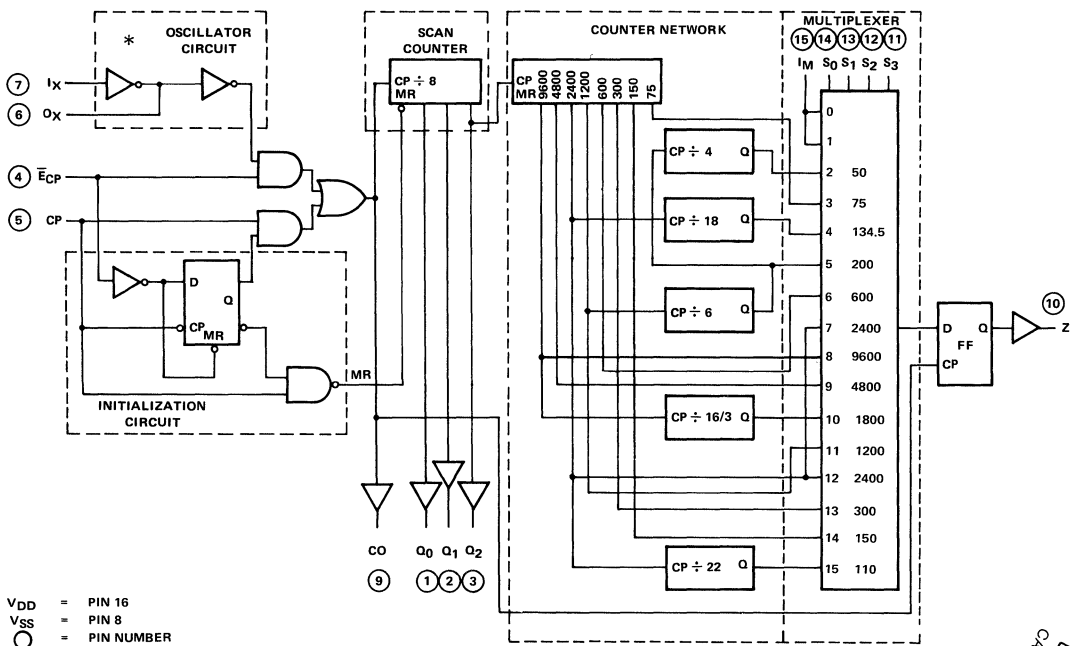
These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

Pin Description

PIN NUMBER	TYPE	SYMBOL	DESCRIPTION
16		V_{CC}	V_{CC}: is the +5V power supply pin. A 0.1μF capacitor between pins 16 and 8 is recommended for decoupling.
8		GND	GROUND
5	I	CP	EXTERNAL CLOCK INPUT
4	I	E_{CP}	EXTERNAL CLOCK ENABLE: A low signal on this input allows the baud rate to be generated from the CP input.
7	I	I_X	CRYSTAL INPUT
6	O	O_X	CRYSTAL DRIVE OUTPUT
15	I	I_M	MULTIPLEXED INPUT
11, 12, 13	I	S_0 - S_3	BAUD RATE SELECT INPUTS
9	O	CO	CLOCK OUTPUT
1, 2, 3	O	Q_0 - Q_2	SCAN COUNTER OUTPUTS
10	O	Z	BIT RATE OUTPUT

Block Diagram

HD-4702 ONLY



* See Table 3 for Crystal Specifications

Absolute Maximum Ratings

Supply Voltage .... +8.0 Volts
Input, Output or I/O Voltage Applied .... GND -0.3V to VCC +0.3V
Storage Temperature Range .... -65°C to +150°C
Maximum Package Power Dissipation .... 1 Watt
θ_{jc} .... 27°C/W (CERDIP Package), 32°C/W (LCC Package)
θ_{ja} .... 76°C/W (CERDIP Package), 81°C/W (LCC Package)
Gate Count .... 720 Gates
Junction Temperature .... +150°C
Lead Temperature (Soldering, Ten Seconds) .... +260°C

Operating Conditions

Operating Voltage Range .... +4.5V to +5.5V
Operating Temperature Range
HD-4702-9 .... -40°C to +85°C
HD-4702-2/8 .... -55°C to +125°C

Electrical Specifications D.C.: V_{CC} = 5V ± 10%; T_A = HD-4702-9 or HD-4702-2/-8 A.C.: V_{CC} = 5V; T_A = +25°C

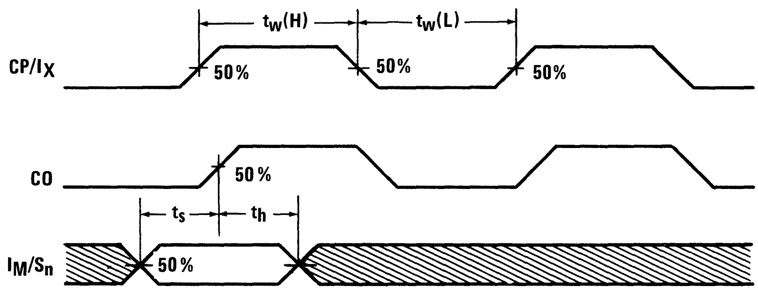
	SYMBOL	PARAMETER	HD-4702-2 MIN	HD-4702-2 TYP	HD-4702-2 MAX	HD-4702-9 MIN	HD-4702-9 TYP	HD-4702-9 MAX	UNITS	TEST CONDITIONS
D.C.	V_{IH}	Input High Voltage	V_{CC}70%			V_{CC}70%			V	
	V_{IL}	Input Low Voltage			30%			30%	V	
	V_{OH1}	Output High Voltage	V_{CC}-.05			V_{CC}-.05			V	$I_{OH} \leq -1\mu A$
	V_{OL1}	Output Low Voltage			0.05			0.05	V	I_{OL} L = 1μA
	I_{IH}	Input High Current	-1		+1	-1		+1	μA	$V_I = V_{CC}$, all other pins = OV
	I_{IL}	Input Low Current ① (all other inputs)		-30	-100		-30	-100	μA	
	I_{ILX}	(I_X Inputs)	-1		+1	-1		+1	μA	V_I = 0, all other pins = V_{CC}
	I_{OHX}	Output High Current (O_X)	-0.1			-0.1			mA	$V_{OUT} = V_{CC}$ -.5; Input at 0 or V_{CC} per Logic Function or Truth Table
	I_{OH1}	(all other outputs)	-1.0			-0.1			mA	V_{OUT} = 2.5V
	I_{OH2}	(all other outputs)	-0.3			-0.3			mA	$V_{OUT} = V_{CC}$ -.5
	I_{OLX}	Output Low Current (O_X)	0.1			0.1			mA	V_{OUT} = .4V
	I_{OL}	(all other outputs)	1.6			1.6			mA	V_{OUT} = .4V
	I_{CC}	Supply Current (Static) ①			1500			1500	μA	$E_{CP} = V_{CC}$, CP = 0, all other inputs = GND
					1000			1000	μA	ECP = V_{CC}, CP = 0, all other inputs = V_{CC}
A.C.	t_{PLH}	Propagation Delay,			300			300	ns	$C_L \leq$ 7pF on O_X ②
	t_{PHL}	I_X to CO			250			250	ns	
	t_{PLH}	Propagation Delay,			215			215	ns	C_L = 15pF on O_X ②
	t_{PHL}	CP to CO			195			195	ns	Transition Times $\leq$ 20ns
	t_{PLH}	Propagation Delay,			⑤			⑤	ns	
	t_{PHL}	CO to Qn							ns	
	t_{PLH}	Propagation Delay,			75			75	ns	
	t_{PHL}	CO to Z			65			65	ns	
	t_{TLH}	Output Transition			80			80	ns	
	t_{THL}	Time (except O_X)			40			40	ns	
	t_{PLH}	Propagation Delay,			350			350	ns	
	t_{PHL}	I_X to CO			275			275	ns	$C_L \leq$ 7pF on O_X ②
	t_{PLH}	Propagation Delay,			260			260	ns	C_L = 50pF Input
	t_{PHL}	CP to CO			220			220	ns	Transition Times $\leq$ 20ns
	t_{PLH}	Propagation Delay,			⑤			⑤	ns	
	t_{PHL}	CO to Qn							ns	
	t_{PLH}	Propagation Delay,			85			85	ns	
	t_{PHL}	CO TO Z			75			75	ns	
	t_{TLH}	Output Transition			160			160	ns	
	t_{THL}	Time (except O_X)			75			75	ns	
	t_s	Set-Up Time, Select to CO	350			350			ns	
	t_h	Hold Time, Select to CO	0			0			ns	$C_L \leq$ 7pF on O_X ②
	t_s	Set-Up Time, I_M to CO	350			350			ns	C_L = 15pF Input
	t_h	Hold Time, I_M to CO	0			0			ns	Transition Times $\leq$ 20ns
	t_WCP(L)	Minimum Clock Pulse-Width	120			120			ns	
	t_WCP(H)	Low and High ③ ④	120			120			ns	
	t_WCP(L)	Minimum IX Pulse Width	160			160			ns	
	t_WCP(H)	Low and High ④	160			160			ns	

NOTES: ① Input Current and Quiescent Power Supply Current are relatively higher for this device because of active pull-up circuits on all inputs except I_X. This is done for TTL compatibility.
② Propagation Delay (t_{PLH} and t_{PHL}) and Output Transistion Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-Up Times (t_s), Hold Times (t_h), and Minimum Pulse Width (t_w) do not vary with load capacitance.
③ The first High Level Clock Pulse after E_{CP} goes Low and must be at least 350ns long to guarantee reset of all Counters.
④ It is recommended that input rise and fall times to the Clock Inputs (CP, I_X) be less than 15μs.
⑤ For multichannel operation, Propagation Delay (CO to Q_n) plus Set-Up Time, Select to CO, is guaranteed to be ≤ 367ns.

Capatitance $T_A = +25^oC$; $V_{CC} = GND = 0V$; $V_{IN} = +5V$ or GND

SYMBOL	PARAMETER	TYPICAL	UNITS	CONDITIONS
C_{IN}	Input Capacitance	7	pF	Frequency = 1MHz
C_{OUT}	Output Capacitance	10	pF	Frequency = 1MHz

Switching Waveforms



NOTE: Set-Up and Hold Times are shown as positive values but may be specified as negative values.

A.C. Testing Input, Output Waveform

A.C. Testing: All Input signals must switch between VIL and VIH. Input Rise and fall times are driven at 1nsec per volt.

Applications

Single Channel Bit Rate Generator

Figure 1 shows the simplest application of the HD-4702. This circuit generates one of five possible bit rates as determined by the setting of a single pole, 5-position switch. The Bit Rate Output (Z) drives one standard TTL load or four low power Schottky loads over the full temperature range. The possible output frequencies correspond to 110, 150, 300, 1200, and 2400 Baud. For many low cost terminals, these five bit rates are adequate.

Simultaneous Generation of Several Bit Rates

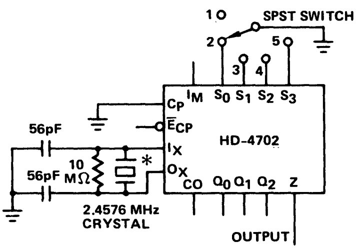
Figure 2 shows a simple scheme that generates eight bit rates on eight output lines, using one HD-4702 and one 93L34 Bit Addressable Latch. This and the following applications take advantage of the built-in scan counter (prescaler) outputs. As shown in the block diagram, these outputs (Q_0 to Q_2) go through a complete sequence of eight states for every half-period of the highest output frequency (9600 Baud). Feeding these Scan Counter Outputs back to the Select Inputs of the multiplexer causes the HD-4702 to interrogate sequentially eight different frequency signals. The 93L34 8-bit addressable Latch, addressed by the same Scan Counter Outputs, re-converts the multiplexed single Output (Z) of the HD-4702 into eight parallel output frequency signals. In the simple scheme of Figure 2, input S_3 is left open (HIGH) and the following bit rates are generated:

Q_0: 110 Baud	Q_1: 9600 Baud	Q_2: 4800 Baud
Q_3: 1800 Baud	Q_4: 1200 Baud	Q_5: 2400 Baud
Q_6: 300 Baud	Q_7: 150 Baud	

Other bit rate combinations can be generated by changing the Scan Counter to Selector interconnection or by inserting logic gates into this path.

19200 Baud Operation

Though a 19200 Baud signal is not internally routed to the multiplexer, the HD-4702 can be used to generate this bit rate by connecting the Q2 output to the IM input and applying select code. An additional 2-input NOR gate can be used to retain the "Zero Baud" feature on select code 1 for the HD-4702 (See Figure 3).



* See Table 3

SWITCH POSITION	HD-4702 BIT RATE
1	110 Baud
2	150 Baud
3	300 Baud
4	1200 Baud
5	2400 Baud

FIGURE 1. SWITCH SELECTABLE BIT RATE GENERATOR CONFIGURATION PROVIDING FIVE BIT RATES.

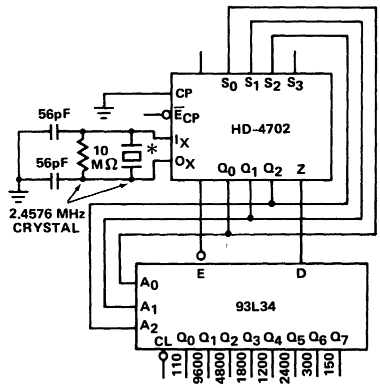


FIGURE 2. BIT RATE GENERATOR CONFIGURATION WITH EIGHT SIMULTANEOUS FREQUENCIES.

* See Table 3

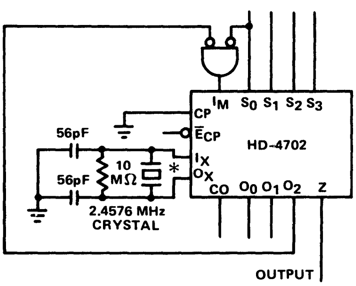


FIGURE 3. 19200 BAUD OPERATION

* See Table 3

TABLE 3. CRYSTAL SPECIFICATIONS

PARAMETERS	TYPICAL CRYSTAL SPEC
Frequency	2.4576MHz "AT" Cut
Series Resistance (Max)	250
Unwanted Modes	-6.0dB (Min)
Type of Operation	Parallel
Load Capacitance	32pF +0.5

HARRIS

HD-6402

CMOS Universal Asynchronous Receiver Transmitter (UART)

Features

- Operation Guaranteed from D.C. to 8.0MHz
- Low Power CMOS Design
- Programmable Word Length, Stop Bits and Parity
- Automatic Data Formatting and Status Generation
- Compatible with Industry Standard UARTs
- Single +5V Power Supply

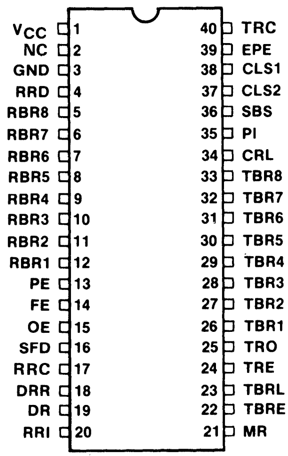
Description

The HD-6402 is a CMOS UART for interfacing computers or microprocessors to an asynchronous serial data channel. The receiver converts serial start, data, parity, and stop bits. The transmitter converts parallel data into serial form and automatically adds start, parity, and stop bits. The data word length can be 5, 6, 7 or 8 bits. Parity may be odd or even. Parity checking and generation can be inhibited. The stop bits may be one or two or one and one-half when transmitting 5 bit code.

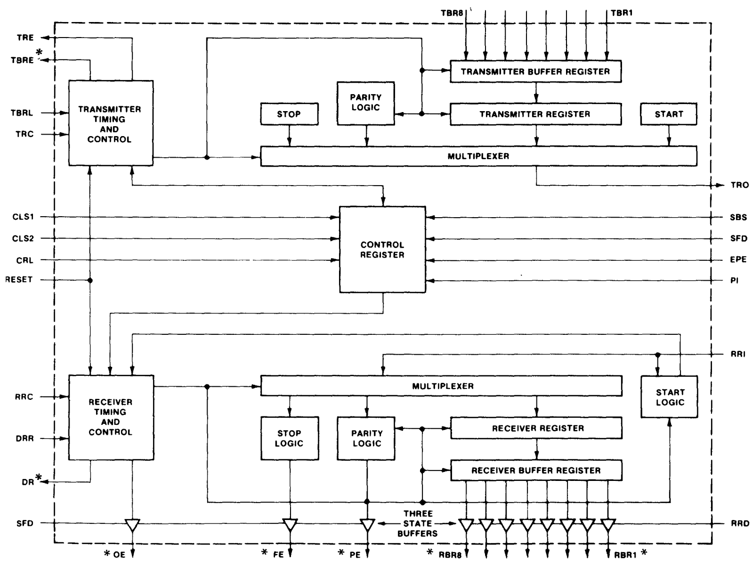
The HD-6402 can be used in a wide range of applications including modems, printers, peripherals and remote data acquisition systems. Utilizing the HARRIS advanced scaled SAJI IV CMOS process permits operation clock frequencies up to 8.0MHz (500K Baud). Power requirements, by comparison, are reduced from 300mW to 10mW. Status logic increases flexibility and simplifies the user interface.

Pinout

TOP VIEW



Functional Diagram



* These outputs are three state

Control Definition

CONTROL WORD — CHARACTER FORMAT

CLS2	CLS1	PI	EPE	SBS	START BIT	DATA BITS	PARITY BIT	STOP BITS
0	0	0	0	0	1	5	ODD	1
0	0	0	0	1	1	5	ODD	1.5
0	0	0	1	0	1	5	EVEN	1
0	0	0	1	1	1	5	EVEN	1.5
0	0	1	X	0	1	5	NONE	1
0	0	1	X	1	1	5	NONE	1.5
0	1	0	0	0	1	6	ODD	1
0	1	0	0	1	1	6	ODD	2
0	1	0	1	0	1	6	EVEN	1
0	1	0	1	1	1	6	EVEN	2
0	1	1	X	0	1	6	NONE	1
0	1	1	X	1	1	6	NONE	2
1	0	0	0	0	1	7	ODD	1
1	0	0	0	1	1	7	ODD	2
1	0	0	1	0	1	7	EVEN	1
1	0	0	1	1	1	7	EVEN	2
1	0	1	X	0	1	7	NONE	1
1	0	1	X	1	1	7	NONE	2
1	1	0	0	0	1	8	ODD	1
1	1	0	0	1	1	8	ODD	2
1	1	0	1	0	1	8	EVEN	1
1	1	0	1	1	1	8	EVEN	2
1	1	1	X	0	1	8	NONE	1
1	1	1	X	1	1	8	NONE	2

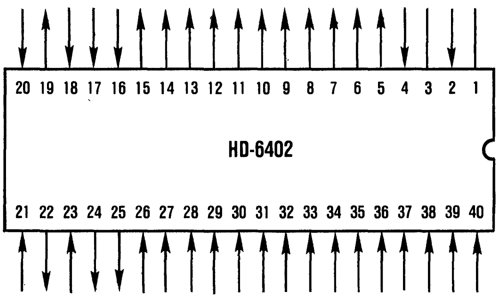
CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

Pin Description

PIN	TYPE	SYMBOL	DESCRIPTION
1		V_{CC} *	Positive Voltage Supply
2		NC	No connection
3		GND	Ground
4	I	RRD	A high level on RECEIVER REGISTER DISABLE forces the receiver holding outputs RBR1-RBR8 to a high impedance state.
5	O	RBR8	The contents of the RECEIVER BUFFER REGISTER appear on these three-state outputs. Word formats less than 8 characters are right justified to RBR1.
6	O	RBR7	See Pin 5-RBR8
7	O	RBR6	See Pin 5-RBR8
8	O	RBR5	See Pin 5-RBR8
9	O	RBR4	See Pin 5-RBR8
10	O	RBR3	See Pin 5-RBR8
11	O	RBR2	See Pin 5-RBR8
12	O	RBR1	See Pin 5-RBR8
13	O	PE	A high level on PARITY ERROR indicates received parity does not match parity programmed by control bits. When parity is inhibited this output is low.
14	O	FE	A high level on FRAMING ERROR indicates the first stop bit was invalid.

PIN	TYPE	SYMBOL	DESCRIPTION
15	O	OE	A high level on OVERRUN ERROR indicates the data received flag was not cleared before the last character was transferred to the receiver buffer register.
16	I	SFD	A high level on STATUS FLAGS DISABLE forces the outputs PE, FE, OE, DR, TBRE to a high impedance state.
17	I	RRC	The Receiver register clock is 16X the receiver data rate.
18	I	$\overline{DRR}$	A low level on DATA RECEIVED RESET clears the data received output DR to a low level.
19	O	DR	A high level on DATA RECEIVED indicates a character has been received and transferred to the receiver buffer register.
20	I	RRI	Serial data on RECEIVER REGISTER INPUT is clocked into the receiver register.
21	I	MR	A high level on MASTER RESET clears PE, FE, OE, and DR to a low level and sets the transmitter register empty (TRE) to a high level after 18 clock cycles. MR does not clear the receiver buffer register. This input must be pulsed at least once after power up.

*A 0.1μF decoupling capacitor from the VCC pin to the GND pin is recommended.



PIN	TYPE	SYMBOL	DESCRIPTION
22	O	TBRE	A high level on TRANSMITTER BUFFER REGISTER EMPTY indicates the transmitter buffer register has transferred its data to the transmitter register and is ready for new data.
23	I	TBRL	A low level on TRANSMITTER BUFFER REGISTER LOAD transfers data from inputs TBR1-TBR8 into the transmitter buffer register. A low to high transition on TBRL initiates data transfer to the transmitter register is busy, transfer is automatically delayed so that the two characters are transmitted end to end.
24	O	TRE	A high level on TRANSMITTER REGISTER EMPTY indicates completed transmission of a character including stop bits.
25	O	TRO	Character data, start data and stop bits appear serially at the TRANSMITTER REGISTER OUTPUT.
26	I	TRB1	Character data is loaded into the TRANSMITTER BUFFER REGISTER via inputs TBR1-TBR8. For character formats less than 8 bits the TBR8, 7, and 6 inputs are ignored corresponding to their programmed word length.
27	I	TBR2	See Pin 26 - TBR1.

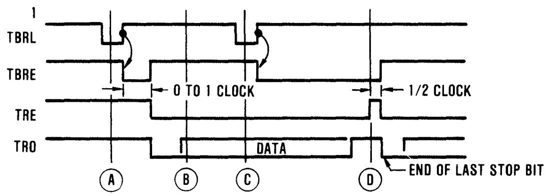
PIN	TYPE	SYMBOL	DESCRIPTION
28	I	TBR3	See Pin 26 - TBR1
29	I	TBR4	See Pin 26 - TBR1.
30	I	TBR5	See Pin 26 - TBR1.
31	I	TBR6	See Pin 26 - TBR1.
32	I	TBR7	See Pin 26 - TBR1.
33	I	TBR8	See Pin 26 - TBR1.
34	I	CRL	A high level on CONTROL REGISTER LOAD loads the control register.
35	I	PI	A high level on PARITY INHIBIT inhibits parity generation, parity checking and forces PE output low.
36	I	SBS	A high level on STOP BIT SELECT selects 1.5 stop bits for 5 character format and 2 stop bits for other lengths.
37	I	CLS2	These inputs program the CHARACTER LENGTH SELECTED (CLS1 low CLS2 low 5 bits) (CLS1 high CLS2 low 6 bits) (CLS1 low CLS2 high 7 bits) (CLS1 high CLS2 high 8 bits).
38	I	CLS1	See Pin 37 - CLS2.
39	I	EPE	When PI is low, a high level on EVEN PARITY ENABLE generates and checks even parity. A low level selects odd parity.
40	I	TRC	The TRANSMITTER REGISTER CLOCK is 16X the transmit data rate.

Transmitter Operation

The transmitter section accepts parallel data, formats the data and transmits the data in serial form on the Transmitter Register Output (TRO) terminal (See serial data format). Data is loaded from the inputs TBR1-TBR8 into the Transmitter Buffer Register by applying a logic low on the Transmitter Buffer Register Load (TBRL) input (A). Valid data must be present at least t_{set} prior to and t_{hold} following the rising edge of TBRL. If words less than 8 bits are used, only the least significant bits are transmitted. The character is right justified, so the least significant bit corresponds to TBR1 (B).

The rising edge of TBRL clears Transmitter Buffer Register Empty (TBRE). 0 to 1 Clock cycles later, data is transferred to the transmitter register, the Transmitter Register Empty (TRE) pin goes to a low state, TBRE is set high and serial data information is transmitted. The output data is clocked by Transmitter Register Clock (TRC) at a clock rate 16 times the data rate. A second low level pulse on TBRL loads data into the Transmitter Buffer Register (C). Data transfer to the transmitter register is delayed until transmission of the current data is complete (D). Data is automatically transferred to the transmitter register and transmission of that character begins one clock cycle later.

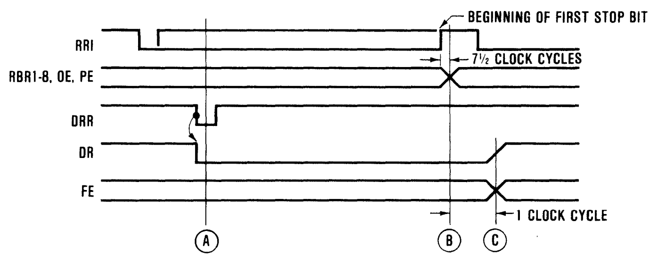
TRANSMITTER TIMING (NOT TO SCALE)



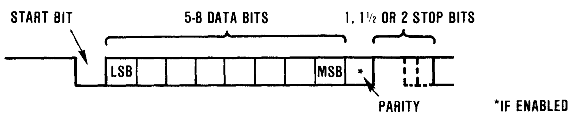
Receiver Operation

Data is received in serial form at the Receiver Register Input (RRI). When no data is being received, RRI must remain high. The data is clocked through the Receiver Register Clock (RRC). The clock rate is 16 times the data rate. A low level on Data Received Reset ($\overline{DRR}$) clears the Data Receiver (DR) line (A). During the first stop bit data is transferred from the receiver register to the Receiver Buffer Register (RBR) (B). If the word is less than 8 bits, the unused most significant bits will be a logic low. The output character is right justified to the least significant bit RBR1. A logic high on Overrun Error (OE) indicates overruns. An overrun occurs when DR has not been cleared before the present character was transferred to the RBR. One clock cycle later DR is reset to a logic high, and Framing Error (FE) is evaluated (C). A logic high on FE indicates an invalid stop bit was received, a framing error. A logic high on Parity Error (PE) indicates a parity error.

RECEIVER TIMING (NOT TO SCALE)

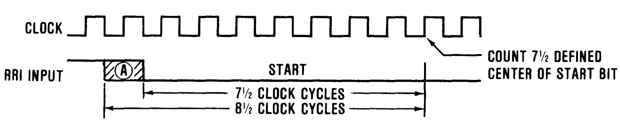


SERIAL DATA FORMAT



Start Bit Detection

The receiver uses a 16X clock timing. The start bit could have occurred as much as one clock cycle before it was detected, as indicated by the shaded portion (A). The center of the start bit is defined as clock count 7½. If the receiver clock is a symmetrical square wave, the center of the start bit will be located within ±½ clock cycle, ±1/32 bit or 3.125% giving a receiver margin of 46.875%. The receiver begins searching for the next start bit at the center of the first stop bit.



Absolute Maximum Ratings

Supply Voltage .... +8.0 Volts
Input, Output or I/O Voltage Applied .... GND - 0.5V to VCC + 0.5V
Storage Temperature Range .... -65°C to +150°C
Maximum Package Power Dissipation .... 1 Watt
θ_{jc} .... 25°C/W (CERDIP package)
θ_{ja} .... 70°C/W (CERDIP package)
Gate Count .... 1,643 Gates
Junction Temperature .... +150°C
Lead Temperature (Soldering, Ten Seconds) ...... +260°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +4.5V to +5.5V
Operating Temperature Ranges
HD-6402-9 .... -40°C to +85°C
HD-6402-2/-8 .... -55°C to +125°C

Electrical Specifications V_{CC} = 5.0V ± 10%, T_A = -40°C to +85°C (HD-6402R-9), T_A = -55°C to +125°C (HD-6402R-2/-8)

	SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
D.C.	V_{IH}	Logical "1" Input Voltage	2.0		V	HD-6402R-9
			2.2		V	HD-6402R-2/-8
	V_{IHC}	Logical "1" Clock Input Voltage	2.0		V	
	V_{ILC}	Logical "0" Clock Input Voltage		0.8	V	
	V_{IL}	Logical "0" Input Voltage		0.8	V	
	I_I	Input Leakage	-1.0	1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
	V_{OH}	Logical "1" Output Voltage	3.0		V	I_{OH} = -2.5mA
			VCC -0.4		V	I_{OH} = -100μA
	V_{OL}	Logical "0" Output Voltage		0.40	V	I_{OL} = +2.5mA
	I_O	Output Leakage	-1.0	1.0	μA	$0V \leq VO \leq V_{CC}$
	I_{CCSB}	Standby Current		100	μA	V_{IN} = GND or V_{CCI} V_{CC} = 5.5V, Output Open
	I_{CCOP}	Operating Supply Current*		2.0	mA	V_{CC} = 5.5V, Clock Freq. = 2MHz, V_{IN} = V_{CC} or GND, Outputs Open.

*Guaranteed , but not 100% tested.

Capacitance T_A = 25°C; V_{CC} = GND = 0V; V_{IN} = +5V or GND.

SYMBOL	PARAMETER	TYPICAL	UNITS	CONDITIONS
C_{IN}	Input Capacitance	8.0	pF	Freq. = 1MHz, Unmeasured pins returned to GND
C_{OUT}	Output Capacitance	10.0	pF	

Electrical Specifications V_{CC} = 5.0V ± 10%, T_A = -40°C to +85°C (HD-6402R-9), T_A = -55°C to +125°C (HD-6402R-2/-8)

	SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
A.C.	f_{CLOCK}	Clock Frequency	D.C.	2.0	MHz	
	t_{pw}	Pulse Widths CRL, DRR, TBRL	150		ns	C_L = 50pF
	t_{MR}	Pulse Width MR	150		ns	See Switching Time
	t_{SET}	Input Data Setup Time	50		ns	Waveforms 1, 2, 3
	t_{HOLD}	Input Data Hold Time	60		ns	
	t_{EN}	Output Enable Time		160	ns	

Absolute Maximum Ratings

Supply Voltage .... +8.0 Volts
Input, Output or I/O Voltage Applied .... GND - 0.5V to VCC + 0.5V
Storage Temperature Range .... -65°C to +150°C
Maximum Package Power Dissipation .... 1 Watt
θ_{jc} .... 25°C/W (CERDIP package)
θ_{ja} .... 70°C/W (CERDIP package)
Gate Count .... 1,643 Gates
Junction Temperature .... +150°C
Lead Temperature (Soldering, Ten Seconds) .... +260°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +4.5V to +5.5V
Operating Temperature Ranges
HD-6402-9 .... -40°C to +85°C
HD-6402-2/-8 .... -55°C to +125°C

Electrical Specifications VCC = 5.0V ± 10%, T_A = -40°C to +85°C (HD-6402-9), T_A = -55°C to +125°C (HD-6402-2/-8)

	SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
D.C.	V_{IH}	Logical "1" Input Voltage	2.0		V	HD-6402B-9
			2.2		V	HD-6402B-2/-8
	V_{IHC}	Logical "1" Clock Input Voltage	2.0		V	
	V_{ILC}	Logical "0" Clock Input Voltage		0.8	V	
	V_{IL}	Logical "0" Input Voltage		0.8	V	
	I_I	Input Leakage	-1.0	1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
	V_{OH}	Logical "1" Output Voltage	3.0		V	I_{OH} = -2.5mA
			VCC -0.4		V	I_{OH} = -100μA
	V_{OL}	Logical "0" Output Voltage		0.40	V	I_{OL} = +2.5mA
	I_O	Output Leakage	-1.0	1.0	μA	$0V \leq VO \leq V_{CC}$
	I_{CCSB}	Standby Current		100	μA	V_{IN} = GND or V_{CC} V_{CC} = 5.5V, Output Open
	I_{CCOP}	Operating Supply Current*		2.0	mA	V_{CC} = 5.5V, Clock Freq. 2MHz, V_{IN} = V_{CC} or GND Outputs Open

*Guaranteed but not 100% tested.

Capacitance T_A = 25°C; V_{CC} = GND = 0V; V_{IN} = +5V or GND.

SYMBOL	PARAMETER	TYPICAL	UNITS	CONDITIONS
C_{IN}	Input Capacitance	8.0	pF	Freq. = 1MHz, Unmeasured pins returned to GND
C_{OUT}	Output Capacitance	10.0	pF	

Electrical Specifications V_{CC} = 5.0V ± 10%, T_A = -40°C to +85°C (HD-6402-9), T_A = -55°C to +125°C (HD-6402-2/-8)

	SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
A.C.	f_{CLOCK}	Clock Frequency	D.C.	8.0	MHz	
	t_{pw}	Pulse Widths CRL, DRR, TBRL	75		ns	C_L = 50pF
	t_{MR}	Pulse Width MR	150		ns	See Switching Time
	t_{SET}	Input Data Setup Time	20		ns	Waveforms 1, 2, 3
	t_{HOLD}	Input Data Hold Time	20		ns	
	t_{EN}	Output Enable Time		35	ns	

Switching Waveforms

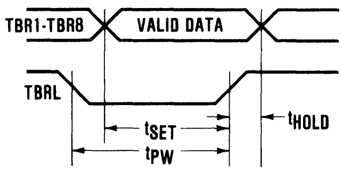


FIGURE 1.
DATA INPUT CYCLE

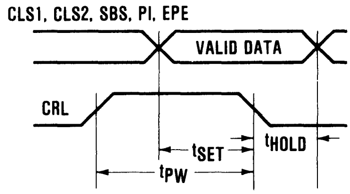


FIGURE 2.
CONTROL REGISTER LOAD CYCLE

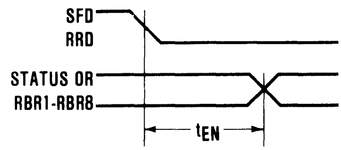
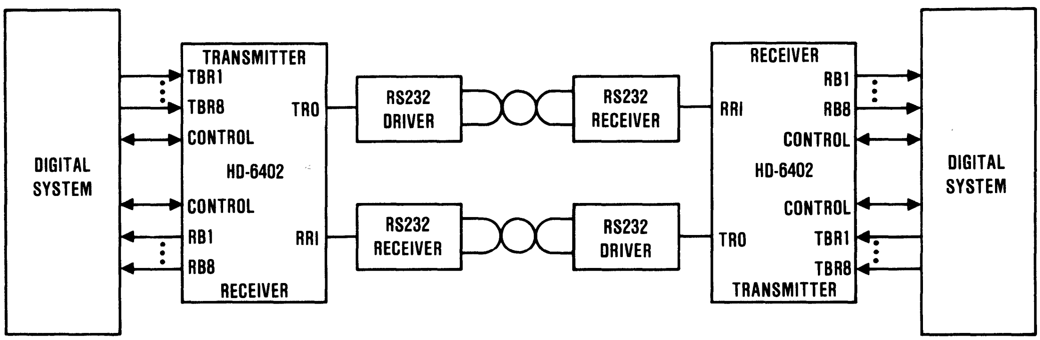


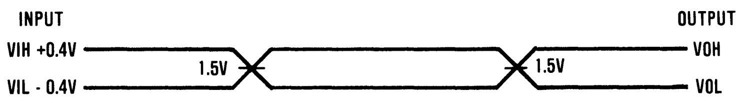
FIGURE 3.
STATUS FLAG OUTPUT ENABLE TIME OR DATA OUTPUT ENABLE TIME

Interfacing With The HD-6402



TYPICAL SERIAL DATA LINK

A.C. Testing Input, Output Waveform



A.C. Testing: All input signals must switch between VIL - 0.4V and VIH + 0.4V. Input rise and fall times are driven at 1ns/V.

HARRIS

HD-6406

CMOS Programmable Asynchronous Communication Interface

REFERENCE PAGE 4-56 FOR
APPLICATION NOTE 108

Features

- Single Chip UART/BRG
- DC to 16MHz Operation
- Crystal or External Clock Input
- On Chip Baud Rate Generator
  - 72 Selectable Baud Rates
- DMA or Vectored Interrupt Mode
- Maskable Interrupts
- Microprocessor Bus Oriented Interface
- Scaled SAJI IV CMOS Process
- Single 5V Power Supply
- Low Power — 1mA/MHz Typical
- Complete Modem Interface
- Line Break Generation and Detection
- Loopback and Echo Modes

Description

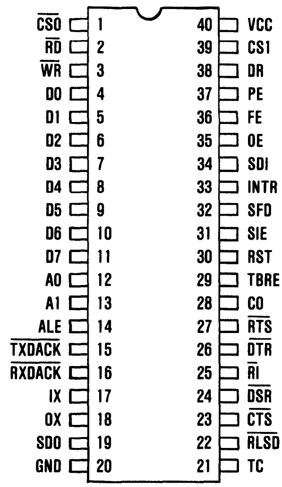
The HD-6406 (PACI) is a high performance programmable Universal Asynchronous Receiver/Transmitter (UART) and Baud Rate Generator (BRG) on a single chip. Utilizing Harris Semiconductor's advanced Scaled SAJI IV CMOS process, the PACI will support data rates from DC to 1Mbaud (0-16MHz clock). In addition to all standard UART functions, the PACI includes a complete Data Communications Equipment (DCE) interface.

Provision is made for DMA control of the PACI so that operation at the higher data rates is not hindered by slow microprocessor response times. An ALE control input permits direct interfacing to multiplexed data/address buses common to many microprocessors.

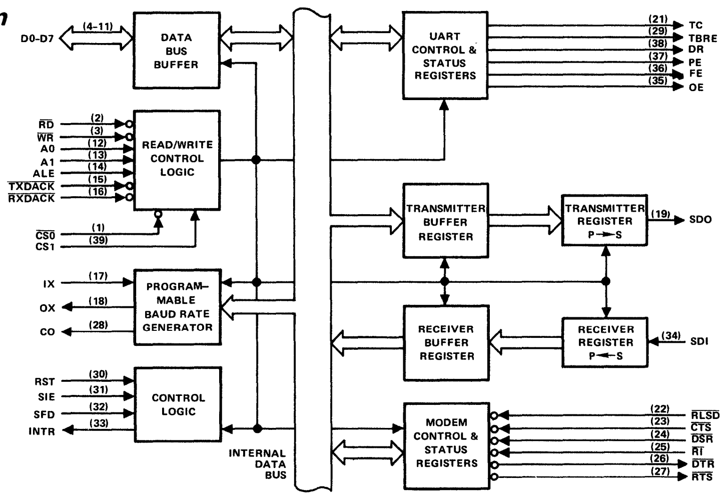
The interrupt structure of the PACI is user-programmable and can be configured to provide a single interrupt for any status change. A subsequent read of an internal status register will identify the source of the interrupt. If desired, the PACI can also provide separate hardware interrupt outputs for the receiver, transmitter and modem status changes. Separate error condition outputs can be used to pinpoint the exact cause of any detected error condition.

Pinout

TOP VIEW



Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow standard IC Handling Procedures.

Pin Description

PIN NUMBER	TYPE	SYMBOL	ACTIVE LEVEL	DESCRIPTION
1, 39	I	$\overline{\text{CS0}}$, CS1	Low, High	CHIP SELECTS: The chip select inputs act as enable signals for the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ input signals during all non-DMA bus operations.
2	I	$\overline{\text{RD}}$	Low	READ: The $\overline{\text{RD}}$ input causes data to be output to the data bus (D0-D7). The data output depends upon the state of the address inputs (A0, A1) during non-DMA operations. During DMA read operations ($\overline{\text{RXDACK}}$ true) the address inputs are ignored and the contents of the Receiver Buffer Register is output providing the DR bit in the Modem Status Register (MSR) is true.
3	I	$\overline{\text{WR}}$	Low	WRITE: The $\overline{\text{WR}}$ input causes data from the data bus (D0-D7) to be input to the PACI. Addressing and chip select action is the same as for read operations with the exception that $\overline{\text{TXDACK}}$ provides the select qualifier for DMA write operations providing the TBRE bit in the MSR is true.
4-11	I/O	D0-D7	High	DATA BITS 0-7: The Data Bus provides eight, 3-state input/output lines for the transfer of data, control and status information between the PACI and the CPU. For character formats of less than 8 bits, the corresponding D7, D6 and D5 are considered "don't cares" for data writes and are 0 for data reads. These lines are normally at their high impedance state except during read operations. D0 is the LSB and is the first serial data bit received or transmitted.
12, 13	I	A0, A1	High	ADDRESS 0, 1: The address lines select the various internal registers during CPU bus operations. Qualified DMA operations ignore the address inputs and access the appropriate receive or transmit buffer register.
14	I	ALE	High	ADDRESS LATCH ENABLE: ALE true enables the internal transparent address latches for the A0, A1 inputs. The address is latched when ALE goes false (low).
15	I	$\overline{\text{TXDACK}}$	Low	TRANSMIT DMA ACKNOWLEDGE: A true $\overline{\text{TXDACK}}$ notifies the PACI that a transmit DMA cycle has been granted. It acts as a chip select which enables the $\overline{\text{WR}}$ input to access the Transmitter Buffer Register when the TBRE bit is in the USR is true.
16	I	$\overline{\text{RXDACK}}$	Low	RECEIVE DMA ACKNOWLEDGE: A true $\overline{\text{RXDACK}}$ notifies the PACI that a receive DMA cycle has been granted. It acts as a chip select which enables the $\overline{\text{RD}}$ input to access the Receive Buffer Register when the DR bit in the USR is true.
17, 18	I, O	IX, OX		CRYSTAL/CLOCK: Crystal connections for the internal Baud Rate Generator. IX can also be used as an external clock input in which case OX should be left open.
19	O	SDO	High	SERIAL DATA OUTPUT: Serial data output from the PACI transmitter circuitry. A Mark (1) is high and a Space (0) is low. SD0 is held in the Mark condition when the transmitter is disabled with $\overline{\text{CTS}}$ false, RST true, when the Transmitter Register is empty, or when in the Loop Mode.
20		GND	Low	GROUND: Power supply ground connection.
21	O	TC	High	TRANSMISSION COMPLETE: TC goes true when a complete character, including stop bits, has been transmitted and TBRE is true. TC is reset with a data write to TBR, RST will set TC true.
22	I	$\overline{\text{RLSD}}$	Low	RECEIVE LINE SIGNAL DETECT: The logical state of this input is reflected in the $\overline{\text{RLSD}}$ bit of the Modem Status Register. Any change of state will cause an interrupt on INTR if INTEN and MIEN are true.
23	I	$\overline{\text{CTS}}$	Low	CLEAR TO SEND: The logical state of the $\overline{\text{CTS}}$ line is reflected in the CTS bit of the Modem Status Register. Any change of state of $\overline{\text{CTS}}$ causes INTR to be set true when INTEN and MIEN are true. A false level on $\overline{\text{CTS}}$ will inhibit transmission of data on the SD0 in the Mark (high) state. If $\overline{\text{CTS}}$ goes false during transmission, the current character being transmitted will be completed. $\overline{\text{CTS}}$ does not affect the Loop mode of operation.
24	I	$\overline{\text{DSR}}$	Low	DATA SET READY: The logical state of the $\overline{\text{DSR}}$ line is reflected in the Modem Status Register. Any change of state of DSR will cause INTR to be set if INTEN and MIEN are true. The state of this signal does not affect any other circuitry within the PACI.

Pin Description

PIN NUMBER	TYPE	SYMBOL	ACTIVE LEVEL	DESCRIPTION
25	I	$\overline{RI}$	Low	RING INDICATOR: The logical state of the $\overline{RI}$ line is reflected inn the Modem Status Register. Any change of state of $\overline{RI}$ will cause INTR to be set if INTEN and MIEN are true. The state of this signal does not affect any other circuitry within the PACI.
26	O	$\overline{DTR}$	Low	DATA TERMINAL READY: The $\overline{DTR}$ signal can be set (low) by writing a logic 1 to the appropriate bit in the Modem Control Register (MCR). This signal is cleared (high) by writing a logic 0 to the same bit in the MCR or whenever a RST (high) is applied to the PACI.
27	O	$\overline{RTS}$	Low	REQUEST TO SEND: The $\overline{RTS}$ signal can be set (low) by writing a logic 1 to the appropriate bit in the MCR. This signal is cleared (high) by writing a logic 0 to the same bit in the MCR or whenever a RST (high) is applied to the PACI.
28	O	CO		CLOCK OUT: This output is user programmable to provide either buffered IX output or a buffered Baud Rate Generator (16X) clock output. The buffered IX (Crystal or external clock source) output is provided when the BRSR bit 7 is set to a zero. Writing a logic one to BRSR bit 7 causes the CO output to provide a buffered version of the internal Baud Rate Generator clock which operates at sixteen times the programmed baud rate.
29	O	TBRE	High	TRAMSMITTER BUFFER REGISTER EMPTY: The TBRE output is set (high) whenever the Tranmitter Buffer Register (TBR) has transferred its data to the Transmit Register. Application of a RST to the PACI will also set the TBRE output. TBRE is cleared (low) whenever data is written to the TBR.
30	I	RST	High	RESET: The RST input forces the PACI into an "Idle" mode in which all serial data activities are suspended. The Modem Control Register (MCR) along with its associated outputs are cleared. The UART Status Register (USR) is cleared except for the TBRE and TC bits which are set. The PACI remains in an "Idle" state until programmed to resume serial data activities. The RST input is a Schmitt trigger input.
31	I	SIE	High	SINGLE INTERRUPT ENABLE: A true (high) level on the SIE input enables interrupts caused by the DR and TBRE status bits. This enables the user to utilize a single hardware interrupt signal (INTR) for any status change within the PACI.
32	I	SFD	High	STATUS FLAGS DISABLE: Holding the SFD input true (high) prevents the true state of the USR bits PE, OE, FE and TC from causing an interrupt. This control input, like the SIE input, enables the user to define what status changes will effect the INTR output.
33	O	INTR	High	INTERRUPT REQUEST: The INTR output is enabled by the INTEN bit in the Modem Control Register (MCR). The MIEN bit and the SIE and SFD control inputs selectively enable various status changes to provide an input to the INTR logic. Figure 9 shows an overall view of the relationship of these interrupt control signals.
34	I	SDI	High	SERIAL DATA INPUT: Serial data input to the PACI receiver circuits. A Mark (1) is high, and a Space (0) is low. Data inputs on SDI are disabled when operating in the loop mode, when RST is true or when the Receiver Enable (REN) bit in the MCR register is false.
35	O	OE	High	OVERRUN ERROR: A true level on the OE output indicates that the Receiver Buffer Register (RBR) was full when a character was received. Transfer to the RBR will not occur. OE is updated each time a character is transferred to the RBR. RST high will set OE low.
36	O	FE	High	FRAMING ERROR: A true level on the FE output indicates that there were invalid stop bits in the last received character. The FE output is updated each time a character is transferred to the RBR. RST high will reset FE.
37	O	PE	High	PARITY ERROR: PE is set true whenever the parity of a received character does not match the programmed parity. The PE output is updated each time a character is transferred to the RBR, PE is reset whenever RST is true or when no parity check is programmed.
38	O	DR	High	DATA READY: A true level indicates that a character has been received, transferred to the RBR and is ready for transfer to the CPU. DR is reset on a data read of the RBR or when RST is true.
40		VCC	High	VCC: +5 Volt positive power supply pin. A 0.1μF decoupling capacitor from VCC (pin 40) to GND (pin 20) is recommended.

Functional Description

RESET

During and after power-up, the PACI should be given a **RST high for at least two IX clock cycles** in order to initialize and drive the PACI's circuits to an idle mode until proper programming can be done. A high on RST causes the following events to occur:

- Resets the internal BRG circuits, clock counters and bit counters. The Baud Rate Select Register (BRSR) is not affected.
- Clears the UART Status Register (USR) except for TC and TBRE which are set. The Modem Control Register (MCR) is also cleared. All of the discrete lines, memory elements and miscellaneous logic associated with these register bits are also cleared or turned off. Note that the UART Control Register (UCR) is not affected.

Following removal of the reset condition (RST low), the PACI remains in the idle mode until programmed to its desired system configuration.

PROGRAMMING THE HD-6406 PACI

The complete functional definition of the PACI is programmed by the systems software. A set of control words (UCR, BRSR and MCR) must be sent out by the CPU to initialize the PACI to support the desired communication format. These control words will program the character length, number of stop bits, even/odd/no parity, baud rate etc. Once programmed, the PACI is ready to perform its communication functions.

The control registers can be written to in any order, however the MCR should be written to last because it controls the interrupt enables, modem control outputs and the receiver enable bit. Once the PACI is programmed and operational these registers can be updated any time that the PACI is not immediately transmitting or receiving data.

Table 1 shows the required control signals to access the PACI's internal registers.

ALE	$\overline{CS0}$	CS1	A1	A0	$\overline{WR}$	$\overline{RD}$	OPERATION
1 or ↓	0	1	0	0	↑	1	Data bus → TBR
1 or ↓	0	1	0	0	1	↓	RBR → Data bus
1 or ↓	0	1	0	1	↑	1	Data bus → UCR
1 or ↓	0	1	0	1	1	↓	USR → Data bus
1 or ↓	0	1	1	0	↑	1	Data bus → MCR
1 or ↓	0	1	1	0	1	↓	MCR → Data bus
1 or ↓	0	1	1	1	↑	1	Data bus → BRSR
1 or ↓	0	1	1	1	1	↓	MSR → Data bus

TABLE 1.

The Address Latch Enable (ALE) input acts as an address latch control signal during these operations. If ALE is left high, the address inputs A0, A1 must be held true during the entire bus operation (demultiplexed bus operation). For multiplexed bus applications the address inputs A0, A1 are latched when ALE goes low. In this case A0 and A1 are not required to be held true for the entire bus cycle.

DMA control of the PACI is discussed in a later section of this data sheet and involves reading and writing of the Receiver and Transmitter Buffer Registers (RBR and TBR).

The following descriptions discuss the control registers in detail.

UART CONTROL REGISTER (UCR)

The UCR is a write only register which configures the UART transmitter and receiver circuits. Data bits D7 and D6 are not used but should always be set to a zero in order to insure software compatibility with future product upgrades. During the Echo Mode, the transmitter always repeats the received word and parity, even when the UCR is programmed with different or no parity.

UCR

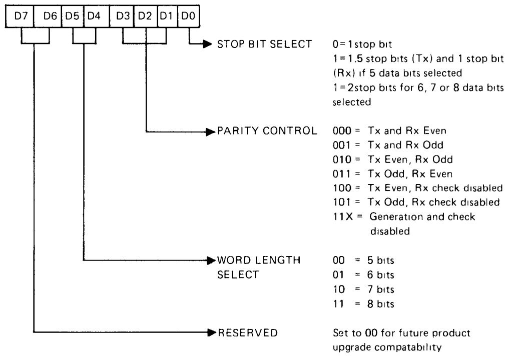


FIGURE 1.

BAUD RATE SELECT REGISTER (BRSR)

The PACI is designed to operate with a single crystal or external clock driving the IX input pin. The Baud Rate Select Register is used to select which divide ratio (one of 72) the internal Baud Rate Generator circuitry will use. The internal circuitry is seperated into two separate counters, a Prescaler and a Divisor Select. The Prescaler can be set to any one of four division rates, ÷1, ÷3, ÷4, or ÷5. This Prescaler design has been optimized to provide standard baud rates using any one of three popular crystal frequencies. By using one of these common system clock frequencies, 1.8432MHz, 2.4576MHz or 3.072MHz and a Prescaler of ÷3, ÷4 or ÷5 respectively, the Prescaler output will provide a constant 614,400Hz. When this frequency is further divided by the Divisor Select counter, any of the standard baud rates from 50 to 38.4Kbaud can be selected (see Table 2). Non-standard baud rates up to 1Mbaud can be selected by using different input frequencies (up to 16MHz) and/or different Prescaler and Divisor Select ratios. The baud rate generator provides a clock which is 16 times the desired baud rate. For example, in order to operate at a 1Mbaud data rate a 16MHz crystal, a Prescale rate of ÷1, and a Divisor Select rate of "external" would be used to provide a 16MHz clock as the output of the Baud Rate Generator to the Transmitter and Receiver Circuits.

The C0 select bit in the BRSR selects whether a buffered version of the external frequency input (IX input) or the Baud Rate Generator output (16X baud rate clock) will be output on the C0 output (pin 28). The Baud Rate Generator output will always be a 50% nominal duty cycle except when "external" is selected and the Prescaler is set to ÷3 or ÷5.

BRSR

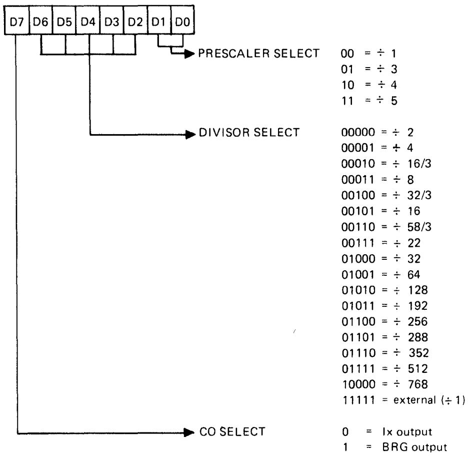


FIGURE 2.

BAUD RATE	DIVISOR
38.4K	External
19.2K	2
9600	4
7200	16/3
4800	8
3600	32/3
2400	16
2000*	58/3
1800*	21
1200	32
600	64
300	128
200	192
150	256
134.5*	288
110*	352
75	512
50	768

TABLE 2.

Note: These baud rates are based upon the following input frequency-/prescale divisor combinations.
1.8432MHz and Prescale = ÷3
2.4576MHz and Prescale = ÷4
3.072MHz and Prescale = ÷5
* All baud rates are exact except for:

BAUD RATE	ACTUAL	PERCENT ERROR
2000	1986.2	0.69%
134.5	133.33	0.87%
110	109.71	0.26%
1800	1828.57	1.56%

MODEM CONTROL REGISTER

The MCR is a general purpose control register which can be written to and read from. The $\overline{RTS}$ and $\overline{DTR}$ outputs are directly controlled by their associated bits in this register. Note that a logic one asserts a true logic level (low) at these output pins. The Interrupt Enable (INTEN) bit is the overall control for the INTR output pin. When INTEN is false, INTR is held false (low). The Operating Mode bits configure the PACI into one of four possible modes. "Normal" configures the PACI for normal full or half duplex communications. "Transmit Break" enables the transmitter to only transmit break characters (Start, Data and Stop bits all are logic zero). The Echo Mode causes any data that is received on the SDI input pin to be re-transmitted on the SDO output pin. Note that this output is a buffered version of the data seen on the SDI input and is not a re-synchronized output (see Figure 4). The Loop Test Mode internally routes transmitted data to the receiver circuitry for the purpose of self test. The transmit data is disabled from the SDO output pin. The Receiver Enable bit gates off the input to the receiver circuitry when in the false state. Modem Interrupt Enable will permit any change in modem status line inputs ($\overline{CTS}$, $\overline{RI}$, $\overline{RLSD}$, $\overline{DSR}$) to cause an interrupt when this bit is enabled. Bit D7 must always be written to with a logic zero to insure correct PACI operation.

MCR

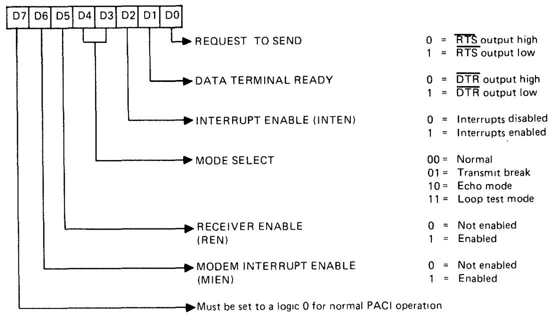


FIGURE 3.

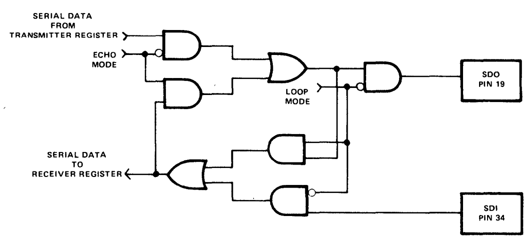


FIGURE 4. LOOP AND ECHO MODE FUNCTIONALITY

UART STATUS REGISTER (USR)

The USR provides a single register that the controlling system can examine to ascertain if errors have occurred or if other status changes in the PACI require the system's attention. For this reason, the USR is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of the PACI. **Reading the USR clears all of the status bits in the USR but does not affect associated output pins.** Three error flags OE, FE and PE report the status of any error conditions detected in the receiver circuitry. These error flags are updated with every character received during reception of the stop bits. The Overrun Error (OE) indicates that a character in the Receiver Register has been received and cannot be transferred to the Receiver Buffer Register (RBR) because the RBR was not read by the CPU. Framing Error (FE) indicates that last character received contained improper stop bits. This could be caused by the total absence of the required stop bit(s) or by a stop bit(s) that was too short to be properly detected. Parity Error (PE) indicates that the last character received contained a parity error based on the programmed parity of the receiver and the calculated parity of the received characters data and parity bits.

The Received Break (RBRK) status bit indicates that the last character received was a break character. A break character would be considered to be an invalid data character in that the entire character including parity and stop bits are a logic zero.

The Modem Status bit is set whenever a transition is detected on any of the Modem input lines ($\overline{RI}$, $\overline{RLSD}$, $\overline{CTS}$ or $\overline{DSR}$). A subsequent read of the Modem Status Register will show the state of these four signals. Assertion of this bit will cause an interrupt (INTR) to be generated if the MIEN and INTEN bits in the MCR register are enabled.

The Transmission Complete (TC) bit indicates that both the TBR and Transmitter Registers are empty and the PACI has completed transmission of the last character it was commanded to transmit. The assertion of this bit will cause an interrupt (INTR) if the SFD (pin 32) input is low and the INTEN bit in the MCR register is true.

USR

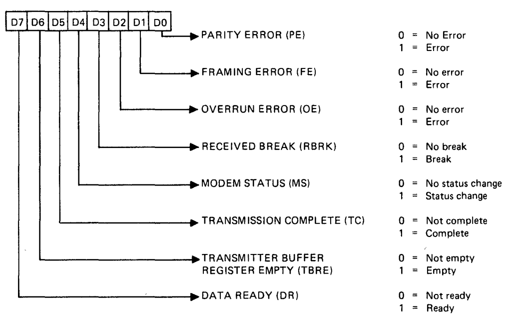


FIGURE 5

The Transmitter Buffer Register Empty (TBRE) bit indicates that the TBR register is empty and ready to receive another character. Assertion of this bit will cause an interrupt if the SIE (pin 31) input is high and the INTEN bit in the MCR is enabled.

The Data Ready (DR) bit indicates that the RBR has been loaded with a received character and that the CPU may access this data. An interrupt will be generated (INTR) if SIE input is high and the INTEN bit is enabled.

MODEM STATUS REGISTER (MSR)

The MSR provides a means whereby the CPU can read the modem signal inputs by accessing the data bus interface of the PACI. **Like all of the register images of external pins in the PACI, true logic levels are represented by a high (1) signal level.** By following this consistent definition the system software need not be concerned with whether external signals are high or low true. In particular the modem signal inputs are low true, thus a 0 (true assertion) at a modem input pin is represented by a 1 (true) in the MSR.

Any change of state of any of the modem input signals will set the Modem Status (MS) bit in the USR register. When this happens an interrupt (INTR) will be generated if the MIEN and INTEN bits of the MCR are enabled.

The Ring Indicator ($\overline{RI}$) input indicates to the PACI that the modem is receiving a ringing signal.

The Receive Line Signal Detect ($\overline{RLSD}$) input is used to notify the PACI that the signal quality received by the modem is within acceptable limits.

The Data Set Ready ($\overline{DSR}$) input is a status indicator from the modem to the PACI which indicates that the modem is ready to provide received data to the PACI receiver circuitry.

Clear to Send ($\overline{CTS}$) is both a status and control signal from the modem that tells the PACI that the modem is ready to receive transmit data from the PACI transmitter output (SDO). A high (false) level on this input will inhibit the PACI from beginning transmission and if asserted in the middle of a transmission will only permit the PACI to finish transmission of the current character.

MSR

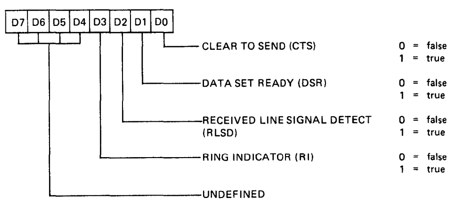
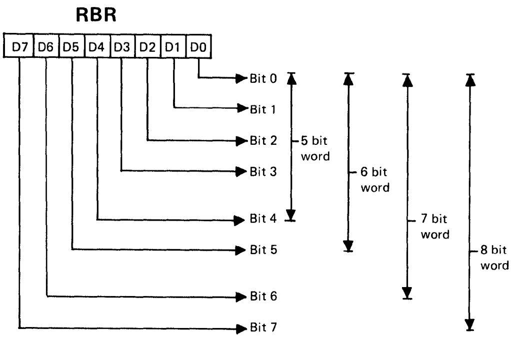


FIGURE 6

RECEIVER BUFFER REGISTER (RBR)

The receiver circuitry in the PACI is programmable for 5, 6, 7 or 8 data bits per character. For words of less than 8 bits, the data is right justified to the LSB (D0). Bit D0 of a data word is always the first data bit received. The unused bits in a less than 8 bit word, at the parallel interface, are set to 0 by the PACI. Received data at the SDI input pin is shifted into the Receiver Register by an internal 1X clock which has been synchronized to the incoming data based on the position of the start bit. When a complete character has been shifted into the Receiver Register, the assembled data bits are parallel loaded into the Receiver Buffer Register. Both the DR output pin and DR flag in the USR register are set. This double buffering of the received data permits continuous reception of data without losing any of the received data. While the Receiver Register is shifting a new character into the PACI, the Receiver Buffer Register is holding a previously received character for the system CPU to read. Failure to read the data in the RBR before complete reception of the next character can result in the loss of the data in the Receiver Register. The OE flag in the USR register indicates the overrun condition.

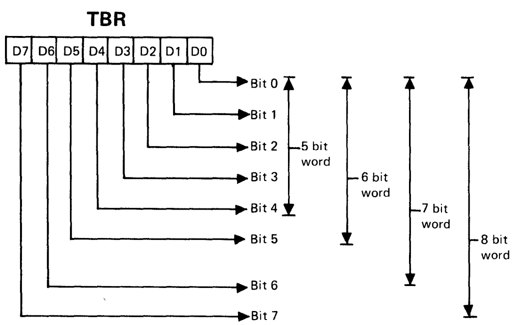


Note: The LSB, Bit 0 is the first serial data bit received.

FIGURE 7.

TRANSMITTER BUFFER REGISTER (TBR)

The Transmitter Buffer Register (TBR) accepts parallel data from the microprocessor data bus (D0-D7) and holds it until the Transmitter Register is empty and ready to accept a new character for transmission. The transmitter always has the same word length and number of stop bits as the receiver. For words of less than 8 bits the unused bits at the microprocessor data bus are ignored by the transmitter. Bit 0, which corresponds to D0 at the data bus, is always the first serial data bit transmitted. Provision is



Note: The LSB, Bit 0 is the first serial data bit transmitted.

FIGURE 8.

made for the transmitter parity to be the same or different from the receiver. The TBRE output pin and flag (USR register) reflect the status of the TBR. The TC output pin and flag (USR register) indicates when both the TBR and TR are empty.

PACI INTERRUPT STRUCTURE

The PACI has provision for both software and hardware masking of interrupts generated for the INTR output pin. The two input pins, SIE and SFD, provide the mask control for the receiver and transmitter status interrupts. Two control bits in the MCR register, MIEN and INTEN, control modem status interrupts and overall PACI interrupts respectively. Figure 9 illustrates the logical control function provided by these signals.

The modem status inputs ($\overline{RLSD}$, $\overline{RI}$, $\overline{DSR}$ and $\overline{CTS}$) will trigger the edge detection circuitry with any change of status. Reading the MSR register will clear the detect circuit but has no effect on the status bits themselves. These status bits always reflect the state of the input pins regardless of the mask control signals. Note that the state (high or low) of the status bits are inverted versions of the actual input pins.

The edge detection circuits for the USR register signals will trigger only for a positive edge (true assertion) of these status bits. **Reading the USR register not only clears the edge detect circuit but also clears (sets to 0) all of the status bits.** The output pins associated with these status bits are not affected by reading the USR register.

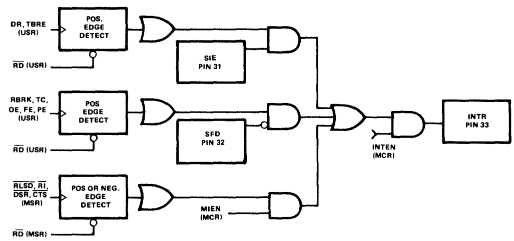


FIGURE 9.

DMA CONTROL OF THE PACI

Because of the high data rates possible with the PACI, provision for DMA control of the transmitter and receiver buffer registers has been included in the design. The $\overline{RXDACK}$ and $\overline{TXDACK}$ inputs in conjunction with the $\overline{RD}$ and $\overline{WR}$ inputs are driven by the system DMA controller to access the RBR and TBR registers respectively.

Reading of the RBR via the $\overline{RXDACK}$ control signal requires that the DR bit in the USR is set (high) and that the $\overline{RD}$ input be driven low. When these conditions are met the address logic overrides the address inputs (A0, A1) and forces a read of the RBR. Similarly, a DMA write to the TBR requires that the TBRE bit in the USR register is set (high) and that $\overline{\text{TXDACK}}$ and $\overline{\text{WR}}$ are asserted by the DMA controller. Once again the address logic overrides the address inputs and forces a write to the TBR register.

The $\overline{\text{CS0}}$ and CS1 inputs would normally be in their inactive state during DMA accesses. The A0, A1, and ALE inputs are overridden during DMA operations and as such their logical state is a don't care.

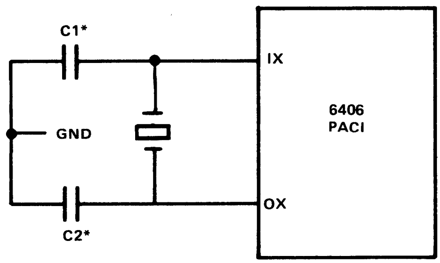
CRYSTAL OPERATIONS

The PACI crystal oscillator circuitry is designed to operate with a fundamental, parallel resonent crystal. This circuit is the same as used in the Harris 82C84A clock generator/driver and as such the general applications information contained in Tech Brief TB-47 that applies to the oscillator operation will be pertinent to the PACI. To summarize Table 3 and Figure 10 show the required crystal parameters and crystal circuit configuration respectively.

When using an external clock source the Ix input is driven and the Ox output is left open. Power consumption when using an external clock is typically 2 times lower than when using a crystal. This is due to the sinusoidal nature of the drive circuitry when using a crystal.

PARAMETER	TYPICAL CRYSTAL SPECIFICATION
Frequency	1.0 to 16MHz
Type of Operation	Parallel resonent, Fund. mode
Load Capacitance (CL)	20 or 32 pf. (typ.)
R_{series}(Max.)	100 ohms (f=16 MHz, CL = 32pf.) 200 ohms (f=16 MHz, CL = 20pf.)

TABLE 3.



* C1 = C2 ≈ 20pf for CL = 20pf.
C1 = C2 ≈ 47pf for CL = 32pf.

FIGURE 10.

REGISTER BIT ASSIGNMENT SUMMARY

REGISTER NAME	MNEMONIC	BIT ASSIGNMENT LSB 0	1	2	3	4	5	6	MSB 7
Receiver Buffer	RBR	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Transmitter Buffer	TBR	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
UART Status	USR	Parity Error (PE)	Framing Error (FE)	Overrun Error (OE)	Received Break (RBRK)	Modem Status (MS)	Transmission Complete (TC)	Transmitter Buffer Reg. empty (TBRE)	Data Ready (DR)
UART Control	UCR	Stop Bit Select	Parity Control 0	Parity Control 1	Parity Control 2	Word Length 0	Word Length 1	Reserved*	Reserved *
Modem Control	MCR	Request To Send (RTS)	Data Terminal Ready (DTR)	Interrupt Enable (INTEN)	Mode Select 0	Mode Select 1	Receiver Enable (REN)	Modem Interrupt enable (MIEN)	0
Modem Status	MSR	Clear to Send (CTS)	Data Set Ready (DSR)	Received Line Signal Detect (RLSD)	Ring Indicator (RI)	Not Used	Not Used	Not Used	Not Used
Bit Rate Select	BRSR	Prescaler Select 0	Prescaler Select 1	Divisor Select 0	Divisor Select 1	Divisor Select 2	Divisor Select 3	Divisor Select 4	Co Select

* Reserved for future use. Always set to zero (0) to maintain future software compatibility.

Absolute Maximum Ratings

Supply Voltage .... +8.0 Volts
Input, Output or I/O Voltage Applied .... GND -0.5V to VCC +0.5V
Storage Temperature Range .... -65°C to +150°C
Maximum Package Power Dissipation .... 1 Watt
θ_{jc} .... 16°C/W (CERDIP Package)
21°C/W (LCC Package)
θ_{ja} .... 43°C/W (CERDIP Package)
48°C/W (LCC Package)
Gate Count .... 1500 Gates
Junction Temperature .... +150°C
Lead Temperature (Soldering, Ten Seconds) ...... +260°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +4.5V to +5.5V
Operating Temperature Range
HD-6406-5 .... 0°C to +70°C
HD-6406-9 .... -40°C to +85°C
HD-6406-2/-8 .... -55°C to +125°C

D. C. Specifications

VCC = 5.0V ±10; T_A = 0°C to +70°C (6046-5);
T_A = -40°C to +85°C (6406-9);
T_A = -55°C to +125°C (6406-2/-8)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VIH	Logical One Input Voltage	2.0		V	
VIL	Logical Zero Input Voltage		0.8	V	
VTH	Schmidt Trigger Logical One Input Voltage	VCC -0.5		V	Reset Input
VTL	Schmidt Trigger Logical Zero Input Voltage		GND +0.5	V	Reset Input
VIH (CLK)	Logical One Clock Voltage	VCC -0.5		V	
VIL (CLK)	Logical Zero Clock Voltage		GND +0.5	V	External Clock
VOH	Output High Voltage	3.0 VCC -0.4		V	IOH = +2.5mA IOH = -400μA
VOL	Output Low Voltage		0.4	V	IOL = +2.5mA
II	Input Leakage Current	-1.0	+1.0	μA	VIN = GND or VCC, DIP Pins 1, 2, 3, 12-16, 22-25, 30, 31, 32, 34-39
IO	Input/Output Leakage Current	-10.0	+10.0	μA	VO = GND or VCC, DIP Pins 4-11
ICCOP*	Operating Power Supply Current		3	mA	External Clock F = 2.4576 MHz, VCC = 5.5V, VIN = VCC or GND, Outputs Open

*Guaranteed and sampled, but not 100% tested. ICCOP is typically ≤ 1mA/MHz.

Capacitance T_A = 25°C; VCC = GND = 0V; VIN = +5V or GND

SYMBOL	PARAMETER	TYP	UNITS	TEST CONDITIONS
CIN*	Input Capacitance	10	pF	FREQ = 1MHz Unmeasured pins returned to GND
COUT*	Output Capacitance	15	pF	
CI/O*	I/O Capacitance	20	pF	

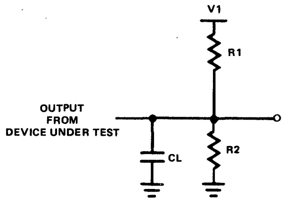
*Guaranteed and sampled, but not 100% tested.

A.C. Specifications VCC = +5V ±10%, GND = 0V: T_A = 0°C to +70°C (HD-6406-5)
T_A = -40°C to +85°C (HD-6406-9)
T_A = -55°C to +125°C (HD-6406-2/-8)

TIMING REQUIREMENTS & RESPONSES

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
TLHLL	ALE Pulse Width	50		ns	
TAVLL	Address Setup	20		ns	
TLLAX	Address Hold	20		ns	
TSVCTL	Select Setup to Control Leading Edge	30		ns	
TCTHSX	Select Hold from Control Trailing Edge	50		ns	
TCTLCTH	Control Pulse Width	150		ns	Control Consists of RD or WR
TCTHCTL	Control Disable to Control Enable	100		ns	
TRLDV	Read Low to Data Valid		120	ns	1
TRHDZ	Read Disable	0	60	ns	2
TCTHLH	Control Inactive to ALE High	20		ns	
TDVWH	Data Setup Time	50		ns	
TWHDX	Data Hold Time	20		ns	
FC	Clock Frequency	0	16	MHz	TCHCL + TCLCH Must Be ≥ 62.5ns
TCHCL	Clock High Time	25		ns	
TCLCH	Clock Low Time	25		ns	
TR/TF	IX Input Rise/Fall Time (10%-90%) (External Clock)		tx	ns	tx ≤ 1/(6FC) or 50ns Whichever is Smaller
TFCO	Clock Output Fall Time		15	ns	CL = 5pF
TRCO	Clock Output Rise Time		15	ns	CL =5pF

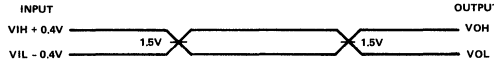
A.C. Test Circuit



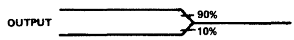
TEST CONDITION	V1	R1	R2	CL
1 Propagation Delay	1.7V	520	∞	100pF
2 Disable Delay	VCC	5K	5K	50pF

A.C. Testing Input, Output Waveform

PROPAGATION DELAY



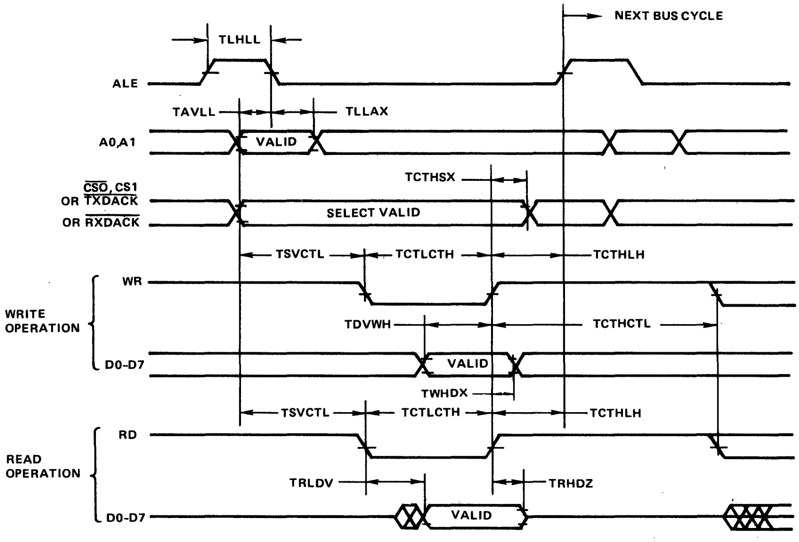
ENABLE/DISABLE DELAY



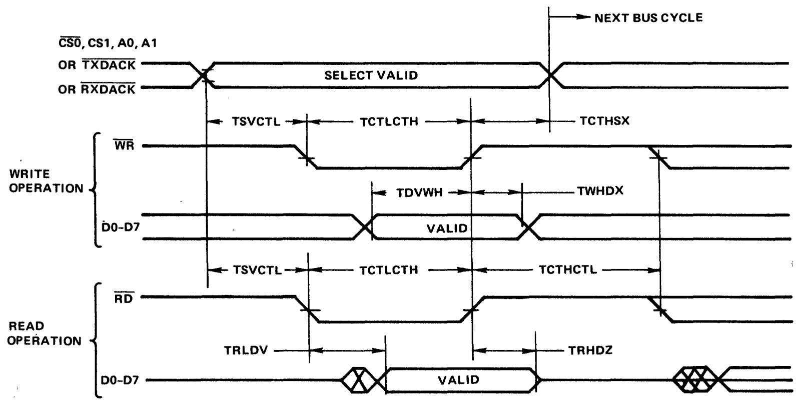
A.C. Testing: All inputs signals must switch between VIL -0.4V and VIH +0.4V. Input rise and fall times are driven at 1nsec per volt.

Timing Diagrams

MULTIPLEXED BUS OPERATION



DEMULTIPLEXED BUS OPERATION (ALE HIGH)



HARRIS

HD-6408

CMOS Asynchronous Serial Manchester Adapter (ASMA)

Features

- Low Bit Error Rate
- One Megabit/sec Data Rate
- Sync Identification and Lock-in
- Clock Recovery
- Manchester II Encoder, Decode
- Separate Encode and Decode
- Low Operating Power: 50mW at 5 Volts
- Single Power Supply
- 24 Pin Package

Pinout

TOP VIEW

VW	1	24	VCC
ESC	2	23	EC
TD	3	22	SCI
SDO	4	21	SD
DC	5	20	SS
BZI	6	19	EE
BOI	7	18	SDI
UDI	8	17	$\overline{BOO}$
DSC	9	16	$\overline{OI}$
CDS	10	15	$\overline{BZO}$
DR	11	14	DBS
GND	12	13	MR

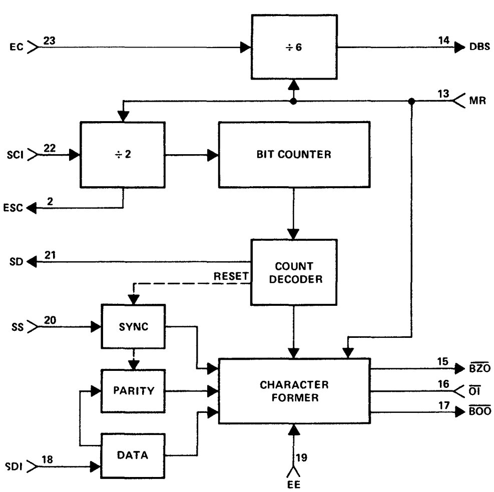
Description

The HD-6408 is a CMOS/LSI Manchester Encoder/Decoder for creating a very high speed asynchronous serial data bus. The Encoder converts serial NRZ data (typically from a shift register) to Manchester II encoded data adding a sync pulse and parity bit. The Decoder recognizes this sync pulse and identifies it as a Command Sync or a Data Sync. The data is then decoded and shifted out in NRZ code (typically into a shift register). Finally, the parity bit is checked. If there were no Manchester or parity errors the Decoder responds with a valid word signal. The Decoder puts the Manchester code to full use to provide clock recovery and excellent noise immunity at these very high speeds.

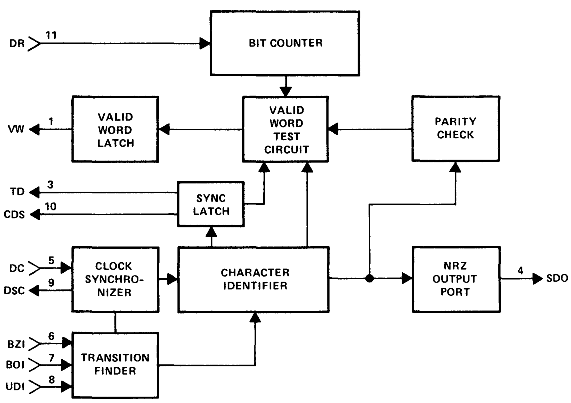
The HD-6408 can be used in many commercial applications such as, security systems, environmental control systems, serial data links and many others. It utilizes a single 12X clock and achieves data rates of up to one million bits per second with a very minimum overhead of only 4 bits out of 20, leaving 16 bits for data.

Block Diagrams

ENCODER



DECODER



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage .... +7.0 Volts
Input, Output or I/O Voltage Applied .... GND -0.5V to V_{CC} +0.3V
Storage Temperature Range .... -65°C to +150°C
Maximum Package Power Dissipation .... 1 Watt
θ_{jc} .... 17°C/W (CERDIP Package), 23°C/W (LCC Package)
θ_{ja} .... 55°C/W (CERDIP Package), 61°C/W (LCC Package)
Gate Count .... 225 Gates
Junction Temperature .... +150°C
Lead Temperature (Soldering, Ten Seconds) .... +260°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +4.5V to +5.5V
Operating Temperature Range
HD6408-9 .... -40°C to +85°C

Electrical Specifications

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
D.C.	V_{IH}	Logical "1" Input Voltage	70% VCC			V	
	V_{IL}	Logical "0" Input Voltage			20% VCC	V	
	V_{IHC}	Logical "1" Input Voltage (Clock)	VCC -0.5			V	
	V_{ILC}	Logical "0" Input Voltage (Clock)			GND +0.5	V	
	II	Input Leakage	-1.0		+1.0	μA	V_{IN} = VCC OR GND, DIP Pins 5-8, 11, 13, 16, 18, 19, 20, 22, 23
	V_{OH}	Logical "1" Output Voltage	2.4			V	I_{OH} = -3mA
	V_{OL}	Logical "0" Output Voltage			0.4	V	I_{OL} = 1.8mA
	I_{CCSB}	Supply Current Standby		0.5	2	mA	$V_{IN} = V_{CC}$ = 5.5V Outputs Open
	I_{CCOP}	Supply Current Operating*		8.0	10.0	mA	V_{CC} = 5.5V, f = 1MHz
		(* Guaranteed and sampled but not 100% tested).					
ENCODER TIMING V_{CC} = 5.0V ± 5% T_A = -40°C to +85°C							
A.C.	F_{EC}	Encoder Clock Frequency	0		12	MHz	CL = 50pF
	F_{ESC}	Send Clock Frequency	0		2.0	MHz	
	T_{ECR}	Encoder CLock Rise Time			8	ns	
	T_{ECF}	Encoder Clock Fall Time			8	ns	
	F_{ED}	Data Rate	0		1.0	MHZ	
	T_{MR}	Master Reset Pulse Width	150			ns	
	T_{E1}	Shift Clock Delay			125	ns	
	T_{E2}	Serial Data Setup	75			ns	
	T_{E3}	Serial Data Hold	75			ns	
	T_{E4}	Enable Setup	90			ns	
	T_{E5}	Enable Pulse Width	100			ns	
	T_{E6}	Sync Setup	55			ns	
	T_{E7}	Sync Pulse Width	150			ns	
	T_{E8}	Send Data Delay	0		50	ns	
	T_{E9}	Bipolar Output Delay			130	ns	
	T_{E10}	Enable Hold	10			ns	
	T_{E11}	Sync Hold	95			ns	
DECODER TIMING V_{CC} = 5.0V ±5% T_A = -40°C to +85°C							
A.C.	F_{DC}	Decoder Clock Frequency	0		15	MHz	CL = 50pF
	T_{DCR}	Decoder Clock Rise Time			8	ns	
	T_{DCF}	Decoder Clock Fall Time			8	ns	
	F_{DD}	Data Rate	0		1.0	MHz	
	T_{DR}	Decoder Reset Pulse Width	150			ns	
	T_{DRS}	Decoder Reset Setup Time	75			ns	
	T_{DRH}	Decoder Reset Hold Time	10			ns	
	T_{MR}	Master Reset Pulse Width	150			ns	
	T_{D1}	Bipolar Data Pulse Width	T_{DC} =10			ns	①
	T_{D2}	Sync Transition Span		$18T_{DC}$		ns	①
	T_{D3}	One Zero Overlap			T_{DC} -10	ns	①
	T_{D4}	Short Data Transition Span		$6T_{DC}$		ns	①
	T_{D5}	Long Data Transition Span		$12T_{DC}$		ns	①
	T_{D6}	Sync Delay (ON)	-20		110	ns	
	T_{D7}	Take Data Delay (ON)	0		110	ns	
	T_{D8}	Serial Data Out Delay			80	ns	
	T_{D9}	Sync Delay (OFF)	0		110	ns	
	T_{D10}	Take Data Delay (OFF)	0		110	ns	
	T_{D11}	Valid Word Delay	0		110	ns	

NOTE ①: T_{DC} = Decoder Clock Period = $\frac{1}{F_{DC}}$ (These parameters are guaranteed but not 100% tested).

Capacitance

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
CIN	Input Capacitance		5.0		pF	
CO	Output Capacitance		8.0		pF	

Pin Description

PIN	TYPE	SYMBOL	SECTION	DESCRIPTION
1	O	VW	Decoder	Output high indicates receipt of a VALID WORD.
2	O	ESC	Encoder	ENCODER SHIFT CLOCK is an output for shifting data into the Encoder. The Encoder samples SDI on the low-to-high transition of ESC.
3	O	TD	Decoder	TAKE DATA output is high during receipt of data after identification of a sync pulse and two valid manchester data bits
4	O	SDO	Decoder	SERIAL DATA OUT delivers received data in correct NRZ format.
5	I	DC	Decoder	DECODER CLOCK input drives the transition finder, and the synchronizer which in turn supplies the clock to the balance of the Decoder. Input a frequency equal to 12X the data rate.
6	I	BZI	Decoder	A high input should be applied to BIPOLAR ZERO IN when the bus is in its negative state. This pin must be held high when the Unipolar input is used.
7	I	BOI	Decoder	A high input should be applied to BIPOLAR ONE IN when the bus is in its positive state, this pin must be held low when the Unipolar input is used.
8	I	UDI	Decoder	With pin 6 high and pin 7 low, this pin enters UNIPOLAR DATA IN to the transition finder circuit. If not used this input must be held low.
9	O	DSC	Decoder	DECODER SHIFT CLOCK output delivers a frequency (DECODER CLOCK ÷ 12), synchronized by the recovered serial data stream.
10	O	CDS	Decoder	COMMAND/DATA SYNC output high occurs during output of decoded data which was preceded by a Command synchronizing character. A low output indicates a Data synchronizing character.
11	I	DR	Decoder	A high input to DECODER RESET during a rising edge of DECODER SHIFT CLOCK resets the decoder bit counting logic to a condition ready for a new word.
12	I	GND	Both	GROUND supply pin.
13	I	MR	Both	A high on MASTER RESET clears the 2:1 counters in both the encoder and decoder and the ÷ 6 counter.
14	O	DBS	Encoder	DIVIDE BY SIX is an output from 6:1 divider which is driven by the ENCODER CLOCK.
15	O	$\overline{\text{BZO}}$	Encoder	$\overline{\text{BIPOLAR ZERO OUT}}$ is a active low output designed to drive the zero or negative sense of a bipolar line driver.
16	I	$\overline{\text{OI}}$	Encoder	A low on $\overline{\text{OUTPUT INHIBIT}}$ forces pin 15 and 17 high, their inactive states.
17	O	$\overline{\text{BOO}}$	Encoder	$\overline{\text{BIPOLAR ONE OUT}}$ is an active low output designed to drive the one or positive sense of a bipolar line driver.
18	I	SDI	Encoder	SERIAL DATA IN accepts a serial data stream at a data rate equal to ENCODER SHIFT CLOCK.
19	I	EE	Encoder	A high on ENCODER ENABLE initiates the encode cycle. (Subject to the preceding cycle being complete.)
20	I	SS	Encoder	SYNC SELECT actuates a Command sync for an input high and Data sync for an input low.
21	O	SD	Encoder	SEND DATA is an active high output which enables the external source of serial data.
22	O	SCI	Encoder	SEND CLOCK IN is 2X the Encoder data rate.
23	I	EC	Encoder	ENCODER CLOCK is the input to the 6:1 divider.
24	I	VCC	Both	VCC is the +5V power supply pin. A 0.1μF decoupling capacitor from VCC (pin 24) to GND (pin 12) is recommended.

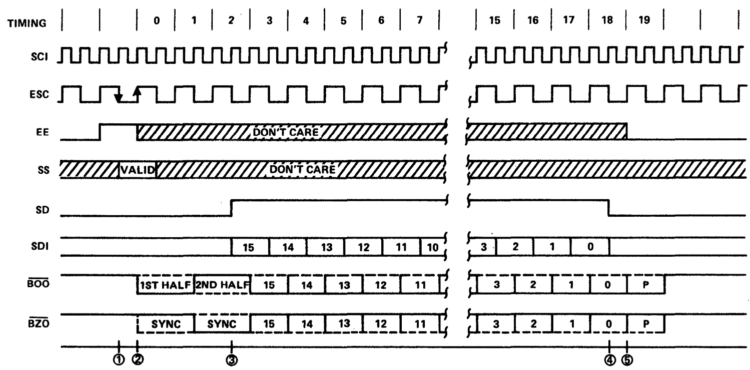
Encoder Operation

The Encoder requires a single clock with a frequency of twice the desired data rate applied at the SClock input. An auxilliary divide by six counter is provided on chip which can be utilized to produce the SClock by dividing the DClock.

The Encoder's cycle begins when EE is high during a falling edge of ESC ①. This cycle lasts for one word length or twenty ESC periods. At the next low-to-high transition of the ESC, a high at SS input actuates a Command sync or a low will produce a Data sync for that word ②. When the Encoder is ready to accept data, the SD output will go high and remain high for sixteen ESC periods ③ – ④.

During these sixteen periods the data should be clocked into the SDInput with every high-to-low transition of the ESC ③ – ④. After the sync and Manchester II encoded data are transmitted through the $\overline{BOO}$ and $\overline{BZO}$ outputs, the Encoder adds on an additional bit which is the (odd) parity for that word ⑤. If ENCODER ENABLE is held high continuously, consecutive words will be encoded without an interframe gap. ENCODER ENABLE must go low by time ⑤ as shown to prevent a consecutive word from being encoded. At any time a low on $\overline{OI}$ will force both bipolar outputs to a high state but will not affect the Encoder in any other way.

To Abort the Encoder transmission a positive pulse must be applied at MR. Any time after or during this pulse, a low-to-high transition on SCI clears the internal counters and initializes the Encoder for a new word.



Decoder Operation

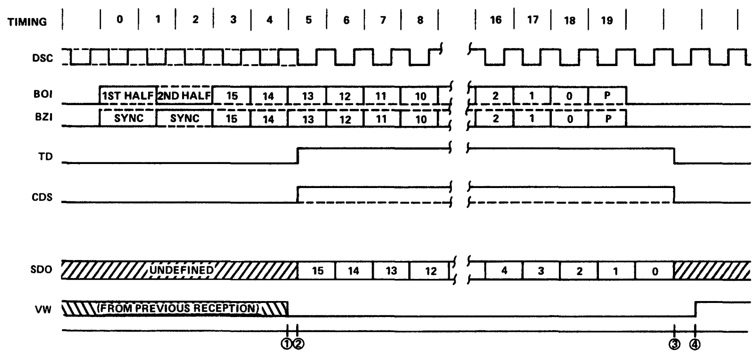
The Decoder requires a single clock with a frequency of 12 times the desired data rate applied at the DClock input. The Manchester II coded data can be presented to the Decoder in one of two ways. The BOI and BZI inputs will accept data from a differential output comparator. The UDI input can only accept noninverted Manchester II coded data (e.g. from $\overline{BOO}$ of an Encoder through an inverter to UDI).

The Decoder is free running and continuously monitors its data input lines for a valid sync character and two valid Manchester data bits to start an output cycle. When a valid sync is recognized ①, the type of sync is indicated by the CDS output. If the sync character was a command, this output will go high ② and remain high for sixteen DSC periods ③, otherwise it will remain low. The TD output will go high and remain high ② – ③ while the Decoder is transmitting the decoded data through SDO.

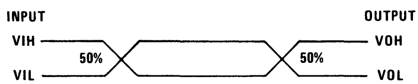
The decoded data available at SDO is in a NRZ format. The DSC is provided so that the decoded bits can be shifted into an external register on every low-to-high transition of this clock ② – ③. Note that DECODER SHIFT CLOCK may adjust its phase up until the time that TAKE DATA goes high.

After all sixteen decoded bits have been transmitted ③ the data is checked for odd parity. A high on VW output ④ indicates a successful reception of a word without any Manchester or parity errors. At this time the Decoder is looking for a new sync character to start another output sequence. VALID WORD will go low approximately 20 DECODER SHIFT CLOCK periods after it goes high if not reset low sooner by a valid sync and two valid Manchester bits as shown ①.

At any time in the above sequence a high input on DR during a low-to-high transition of DSC will abort transmission and initialize the Decoder to start looking for a new sync character.

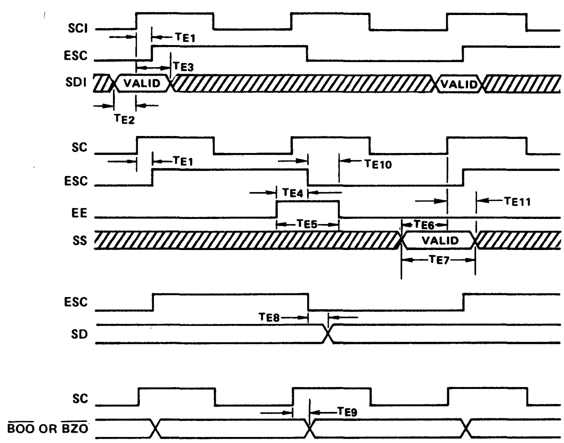


A. C. Testing Input, Output Waveform

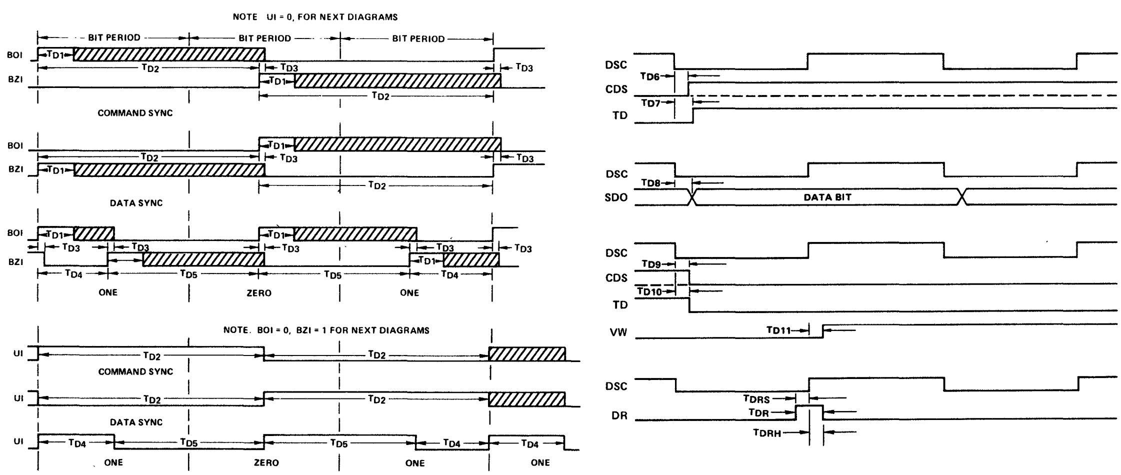


A.C. TESTING: All input signals must switch between VIL and VIH. Input rise and fall times are driven at 1nSec per volt.

Encoder Timing



Decoder Timing



HARRIS

HD-6409

CMOS Manchester Encoder-Decoder (MED)

Features

- Converter or Repeater Mode
- Independent Manchester Encoder and Decoder Operation
- Static to One Megabit/sec Data Rate Guaranteed
- Low Bit Error Rate
- Digital PLL Clock Recovery
- On Chip Oscillator
- Low Operating Power: 50mW at +5V Supply
- Two Temperature Ranges Available
  - ▸ HD-6409-9 .... -40°C to +85°C
  - ▸ HD-6409-2/-8 .... -55°C to +125°C

Description

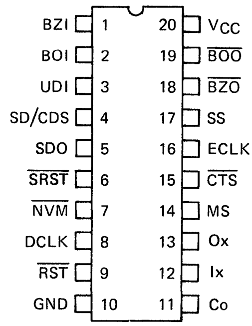
The HD-6409 Manchester Encoder-Decoder (MED) is a high speed, low power device manufactured using self-aligned silicon gate technology. The device is intended for use in serial data communication, and can be operated in either of two modes. In the converter mode, the MED converts Nonreturn-to-Zero code (NRZ) into Manchester code and decodes Manchester code into Nonreturn-to-Zero code. For serial data communication, Manchester code does not have some of the deficiencies inherent in Nonreturn-to-Zero code. For instance, use of the MED on a serial line eliminates DC components, provides clock recovery, and gives a relatively high degree of noise immunity. Because the MED converts the most commonly used code (NRZ) to Manchester code, the advantages of using Manchester code are easily realized in a serial data link.

In the Repeater mode, the MED accepts Manchester code input and reconstructs it with a recovered clock. This minimizes the effects of noise on a serial data link. A digital phase lock loop generates the recovered clock. A maximum data rate of 1MHz requires only 50mW of power.

Manchester code is used in magnetic tape recording and in fiber optic communication, and generally is used where data accuracy is imperative. Because it frames blocks of data, the HD-6409 easily interfaces to protocol controllers.

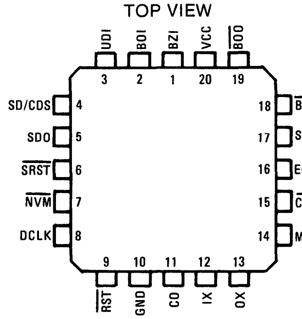
Pinout

TOP VIEW

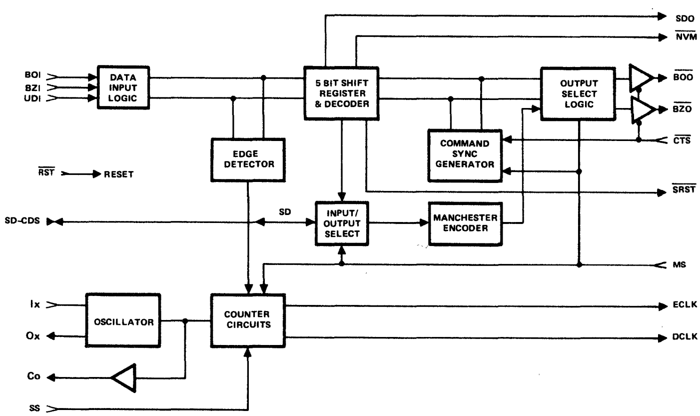


LCC

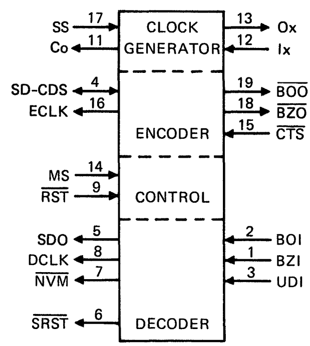
TOP VIEW



Functional Diagram



Logic Symbol



CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

Pin Description

PIN NUMBER	TYPE	SYMBOL	NAME	DESCRIPTION
1	I	BZI	Bipolar Zero Input	Used in conjunction with pin 2, Bipolar One Input (BOI), to input Manchester II encoded data to the decoder, BZI and BOI are logical complements. When using pin 3, Unipolar Data Input (UDI) for data input, BZI must be held high.
2	I	BOI	Bipolar One Input	Used in conjunction with pin 1, Bipolar Zero Input (BZI), to input Manchester II encoded data to the decoder, BOI and BZI are logical complements. When using pin 3, Unipolar Data Input (UDI) for data input, BOI must be held low.
3	I	UDI	Unipolar Data Input	An alternate to bipolar input (BZI, BOI), Unipolar Data Input (UDI) is used to input Manchester II encoded data to the decoder. When using pin 1 (BZI) and pin 2 (BOI) for data input, UDI must be held low.
4	I/O	SD/CDS	Serial Data/Command Data Sync	In the converter mode, SD/CDS is an input used to receive serial NRZ data. NRZ data is accepted synchronously on the falling edge of encoder clock output (ECLK). In the repeater mode, SD/CDS is an output indicating the status of last valid sync pattern received. A high indicates a command sync and a low indicates a data sync pattern.
5	O	SDO	Serial Data Out	The decoded serial NRZ data is transmitted out synchronously with the decoder clock (DCLK). SDO is forced low when RST is low.
6	O	SRST	Serial Reset	In the converter mode, SRST follows RST. In the repeater mode, when RST goes low, SRST goes low and remains low after RST goes high. SRST goes high only when RST is high, the reset bit is zero, and a valid synchronization sequence is received.
7	O	NVM	Nonvalid Manchester	A low on NVM indicates that the decoder has received invalid Manchester data and present data on Serial Data Out (SDO) is invalid. A high indicates that the sync pulse and data were valid and SDO is valid. NVM is set low by a low on RST, and remains low after RST goes high until valid sync pulse followed by two valid Manchester bits is received.
8	O	DCLK	Decoder Clock	The decoder clock is a 1X clock recovered from BZI and BOI to synchronously output received NRZ data (SDO).
9	I	RST	Reset	In the converter mode, a low on RST forces SDO, DCLK, NVM, and SRST low. A high on RST enables SDO and DCLK, and forces SRST high. NVM remains low after RST goes high until a valid sync pulse followed by two Manchester bits is received, after which it goes high. In the repeater mode, RST has the same effect on SDO, DCLK and NVM as in the converter mode. When RST goes low, SRST goes low and remains low after RST goes high. SRST goes high only when RST is high, the reset bit is zero and a valid synchronization sequence is received.

(I) — Input
(O) — Output

Pin Description

PIN NUMBER	TYPE	SYMBOL	NAME	DESCRIPTION
10	I	GND	Ground	Ground
11	O	Co	Clock Output	Buffered output of clock input Ix. May be used as clock signal for other peripherals.
12	I	Ix	Clock Input	Ix is the input for an external clock or, if the internal oscillator is used, Ix and Ox are used for the connection of the crystal.
13	O	Ox	Clock Drive	If the internal oscillator is used, Ox and Ix are used for the connection of the crystal.
14	I	MS	Mode Select	MS must be held low for operation in the converter mode, and high for operation in the repeater mode.
15	I	$\overline{CTS}$	Clear to Send	In the converter mode, a high disables the encoder, forcing outputs $\overline{BOO}$, $\overline{BZO}$ high and ECLK low. A high to low transition of $\overline{CTS}$ initiates transmission of a Command sync pulse. A low on $\overline{CTS}$ enables $\overline{BOO}$, $\overline{BZO}$, and ECLK. In the repeater mode, the function of $\overline{CTS}$ is identical to that of the converter mode with the exception that a transition of $\overline{CTS}$ does not initiate a synchronization sequence.
16	O	ECLK	Encoder Clock	In the converter mode, ECLK is a 1X clock output used to receive serial NRZ data to SD/CDS. In the repeater mode, ECLK is a 2X clock which is recovered from BZI and BOI data by the digital phase locked loop.
17	I	SS	Speed Select	A logic high on SS sets the data rate at 1/32 times the clock frequency while a low sets the data rate at 1/16 times the clock frequency.
18	O	$\overline{BZO}$	$\overline{\text{Bipolar Zero Output}}$	$\overline{BZO}$ and its logical complement $\overline{BOO}$ are the Manchester data outputs of the encoder. The inactive state for these outputs is in the high state.
19	O	$\overline{BOO}$	$\overline{\text{Bipolar One Out}}$	See pin 18.
20	I	VCC	VCC	VCC is the +5V power supply pin. A 1.0μF decompling capacitor from VCC (pin-20) to GND (pin-10) is recommended.

(I)—Input
(O)—Output

Absolute Maximum Ratings

Supply Voltage .... +7.0 Volts
Input, Output or I/O Voltage Applied .... GND -0.3V to VCC +0.3V
Maximum Package Power Dissipation .... 1 Watt
Storage Temperature Range .... -65°C to +150°C
θ_{jc} .... 32°C/W (CERDIP Package), 37°C/W (LCC Package)
θ_{ja} .... 91°C/W (CERDIP Package), 96°C/W (LCC Package)
Gate Count .... 250 Gates
Junction Temperature .... +150°C
Lead Temperature (Soldering, Ten Seconds) .... +260°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +4.5V to +5.5V
Operating Temperature Range
HD-6409C-9 .... -40°C to +85°C

Electrical Specifications

VCC = 5V ± 10%; GND = 0V; T_A = -40°C to +85°C

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
DC	V_{IH}	Logic-1 Input Voltage	70% VCC			V	
	V_{IL}	Logic-0 Input Voltage			20% VCC	V	
	V_{IHR}	Logic-1 Input Voltage (Reset)	VCC -0.5			V	
	V_{ILR}	Logic-0 Input Voltage (Reset)			GND +0.5	V	
	V_{IHC}	Logic-1 Input Voltage (Clock)	VCC -0.5			V	
	V_{ILC}	Logic-0 Input Voltage (Clock)			GND +0.5	V	$V_{IN} = V_{CC}$ or GND
	II	Input Leakage	-1.0		+1.0	µA	DIP Pins 1-4, 9, 12, 14, 15, 17
	V_{OH}	Logic-1 Output Voltage	VCC -0.4			V	I_{OH} = -2.0mA
	V_{OL}	Logic-0 Output Voltage			0.4	V	I_{OL} = 2.0mA
	I_{CCQ}	Supply Current Quiescent		1.0	100	µA	$V_{IN} = V_{CC}$ = 5.5V
	I_{CCOP}	Supply Current Operating*		4.0	10.0	mA	V_{CC} = 5.5V, f_{co} = 8MHz
AC	f_c	Clock Frequency			8	MHz	Ix or Xtal
	t_c	Clock Period			1/fc	s	
	t_1	Bipolar Pulse Width	t_c -10			ns	
	t_2	Sync Transition Span		1.5 x CR x t_c ① ②		ns	
	t_3	One-Zero Overlap			t_c -10	ns	
	t_4	Short Data Transition Span		0.5 x CR x t_c ① ②		ns	
	t_5	Long Data Transition Span		CR x t_c		ns	
	t6	Output Rise & Fall Time			50	ns	CL = 20pF for Co,
		Clock Out Co Rise & Fall Time			1/(5 x f_c)	s	50pF Otherwise
	t_7	Input Rise & Fall Time			1/(5 x f_c)	s	50ns Maximum
	t_8	Clock High Time	42			ns	T_{CYCLE} = 125ns, Fig. 6
	t_9	Clock Low Time	42			ns	T_{CYCLE} = 125ns, Fig. 6

CONVERTER MODE

	ENCODER SECTION						
AC	t_{CE1}	SD Setup Time	120			ns	
	t_{CE2}	SD Hold Time	0			ns	
	t_{CE3}	SD to BZO, BOO Prop Delay		1	1.5	DBP	
	t_{CE4}	CTS Low to BZO, BOO Enabled		1	1.5	DBP	
	t_{CE5}	CTS Low to ECLK Enabled		10.5		DBP	
	t_{CE6}	CTS High to ECLK Disabled		1.0	1.5	DBP	
	t_{CE7}	CTS High to BZO, BOO Disabled		2.0	2.5	DBP	

	DECODER SECTION						
AC	t_{CD1}	UDI to SDO, NVM	2.5		3	DBP ③	
	t_{CD2}	DCLK to SDO, NVM			40	ns	
	t_{CD3}	RST Low to DCLK, SDO, NVM Low		0.5	1.5	DBP ③	CL = 50pF
	t_{CD4}	RST High to DCLK Enabled		0.5	1.5	DBP ③	CL = 50pF

REPEATER MODE

AC	t_{R1}	UDI to BOO, BZO		1		DBP ③	
	t_{R2}	ECLK to BZO			40	ns	
	t_{R3}	UDI to SDO, NVM	2.5		3	DBP ③	

NOTES:
① CR — Clock Rate, either 16X or 32X.
② tc = 1/fc
③ DBP — Data Bit Period, CR = 16X, one DBP = 16 clock cycles; CR = 32X, one DBP = 32 clock cycles
* Guaranteed and sampled but not 100% tested.

Capacitance

SYMBOL	PARAMETER	TYPICAL	UNIT	TEST CONDITIONS
CIN	Input Capacitance	6.0	pF	
COUT	Output Capacitance	8.0	pF	

Absolute Maximum Ratings

Supply Voltage .... +7.0 Volts
Input, Output or I/O Voltage Applied .... GND -0.3V to VCC +0.3V
Maximum Package Power Dissipation .... 1 Watt
Storage Temperature Range .... -65°C to +150°C
θjc .... 32°C/W (CERDIP Package), 37°C/W (LCC Package)
θja .... 91°C/W (CERDIP Package), 96°C/W (LCC Package)
Gate Count .... 250 Gates
Junction Temperature .... +150°C
Lead Temperature (Soldering, Ten Seconds) .... +260°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +4.5V to +5.5V
Operating Temperature Range
HD-6409-9 .... -40°C to +85°C
HD-6409-2/-8 .... -55°C to +125°C

Electrical Specifications

VCC = 5V ± 10%; GND = 0V; T_A = -40°C to +85°C (HD-6409-9);
T_A = -55°C to +125°C (HD-6409-2)

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
DC	V_{IH}	Logic-1 Input Voltage	70% VCC			V	
	V_{IL}	Logic-0 Input Voltage			20% VCC	V	
	V_{IHR}	Logic-1 Input Voltage ($\overline{\text{Reset}}$)	VCC -0.5			V	
	V_{ILR}	Logic-0 Input Voltage ($\overline{\text{Reset}}$)			GND +0.5	V	
	V_{IHC}	Logic-1 Input Voltage (Clock)	VCC -0.5			V	
	V_{ILC}	Logic-0 Input Voltage (Clock)			GND +0.5	V	$V_{IN} = V_{CC}$ or GND
	II	Input Leakage	-1.0		+1.0	μA	DIP Pins 1-4, 9, 12, 14, 15, 17
	V_{OH}	Logic-1 Output Voltage	VCC -0.4			V	I_{OH} = -2.0mA
	V_{OL}	Logic-0 Output Voltage			0.4	V	I_{OL} = 2.0mA
	I_{CCQ}	Supply Current Quiescent		1.0	100	μA	$V_{IN} = V_{CC}$ = 5.5V
	I_{CCOP}	Supply Current Operating*		7.0	12.0	mA	V_{CC} = 5.5V, f_{co} = 16MHz
AC	f_c	Clock Frequency			16	MHz	Ix or Xtal
	t_c	Clock Period			1/fc	s	
	t_1	Bipolar Pulse Width	t_c -10			ns	
	t_2	Sync Transition Span		1.5 x CR x t_c (1) (2)		ns	
	t_3	One-Zero Overlap			t_c -10	ns	
	t_4	Short Data Transition Span		0.5 x CR x t_c (1) (2)		ns	
	t_5	Long Data Transition Span		CR x t_c		ns	
	t6	Output Rise & Fall Time			50	ns	CL = 20pF for Co,
		Clock Out Co Rise & Fall Time			1/(5 x f_c)	s	50pF Otherwise
	t_7	Input Rise & Fall Time			1/(5 x f_c)	s	50ns Maximum
	t_8	Clock High Time	20			ns	T_{CYCLE} = 62ns, Fig. 6
	t_9	Clock Low Time	20			ns	T_{CYCLE} = 62ns, Fig. 6

CONVERTER MODE

	ENCODER SECTION						
AC	t_{CE1}	SD Setup Time	70			ns	
	t_{CE2}	SD Hold Time	0			ns	
	t_{CE3}	SD to $\overline{\text{BZO}}$, $\overline{\text{BOO}}$ Prop Delay		1	1.5	DBP	
	t_{CE4}	$\overline{\text{CTS}}$ Low to $\overline{\text{BZO}}$, $\overline{\text{BOO}}$ Enabled		1	1.5	DBP	
	t_{CE5}	$\overline{\text{CTS}}$ Low to ECLK Enabled		10.5		DBP	
	t_{CE6}	$\overline{\text{CTS}}$ High to ECLK Disabled		1.0	1.5	DBP	
	t_{CE7}	CTS High to $\overline{\text{BZO}}$, BOO Disabled		2.0	2.5	DBP	

	DECODER SECTION						
AC	t_{CD1}	UDI to SDO, $\overline{\text{NVM}}$	2.5		3	DBP (3)	
	t_{CD2}	DCLK to SDO, NVM			40	ns	
	t_{CD3}	$\overline{\text{RST}}$ Low to DCLK, SDO, $\overline{\text{NVM}}$ Low		0.5	1.5	DBP (3)	CL = 50pF
	t_{CD4}	RST High to DCLK Enabled		0.5	1.5	DBP (3)	CL = 50pF

REPEATER MODE

AC	t_{R1}	UDI to $\overline{\text{BOO}}$, $\overline{\text{BZO}}$		1		DBP (3)	
	t_{R2}	ECLK to $\overline{\text{BZO}}$			40	ns	
	t_{R3}	UDI to SDO, NVM	2.5		3	DBP (3)	

NOTES:
(1) CR — Clock Rate, either 16X or 32X.
(2) tc = 1/fc
(3) DBP — Data Bit Period, CR = 16X, one DBP = 16 clock cycles; CR = 32X, one DBP = 32 clock cycles
* Guaranteed and sampled but not 100% tested.

Capacitance

SYMBOL	PARAMETER	TYPICAL	UNIT	TEST CONDITIONS
CIN	Input Capacitance	6.0	pF	
COUT	Output Capacitance	8.0	pF	

Converter Mode

ENCODER OPERATION

The encoder uses free running clocks at 1X and 2X the data rate derived from the system clock I_X for internal timing. $\overline{CTS}$ is used to control the encoder outputs, ECLK, $\overline{BOO}$ and $\overline{BZO}$. A free running 1X ECLK is transmitted out of the encoder to drive the external circuits which supply the NRZ data to the MED at pin SD/CDS.

A low on $\overline{CTS}$ enables encoder outputs ECLK, $\overline{BOO}$ and $\overline{BZO}$, while a high on $\overline{CTS}$ forces $\overline{BZO}$, $\overline{BOO}$ high and holds ECLK low. When $\overline{CTS}$ goes from high to low ①, a synchronization sequence is transmitted out on $\overline{BOO}$ and $\overline{BZO}$. A synchronization sequence consists of eight Manchester "0" bits followed by a command sync pulse. ② A command sync pulse is a three bit wide pulse with the first 1½ bits high followed by 1½ bits low. ③ Serial NRZ data is clocked into the encoder at SD/CDS on the high to low transition of ECLK during the command sync pulse. The NRZ data received is encoded into Manchester II data and transmitted out on $\overline{BOO}$ and $\overline{BZO}$ following the command sync pulse. ④ Following the synchronization sequence, input data is encoded and transmitted out continuously without parity check or word framing. The length of the data block encoded is defined by $\overline{CTS}$. Manchester data out is inverted.

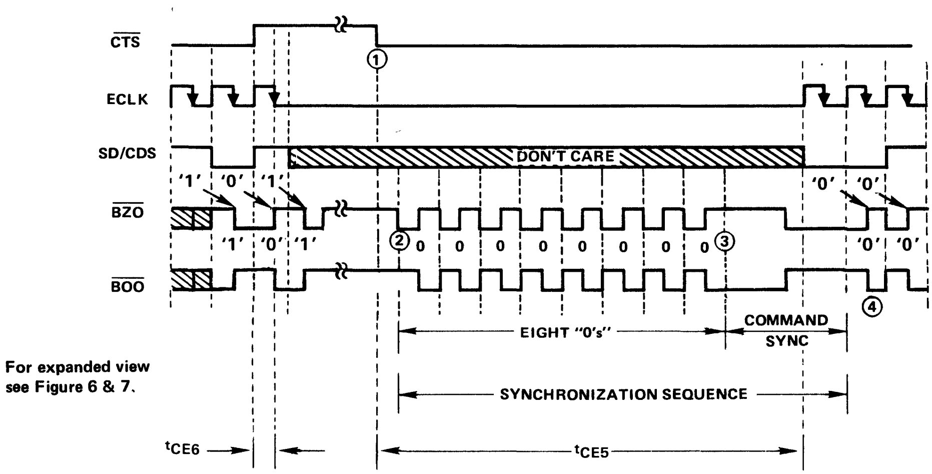


FIGURE 1.

DECODER OPERATION

The decoder requires a single clock with a frequency 16X or 32X the desired data rate. The rate is selected on the speed select with SS low producing a 16X clock and high a 32X clock. For long data links the 32X mode should be used as this permits a wider timing jitter margin. The internal operation of the decoder utilizes a free running clock synchronized with incoming data for its clocking.

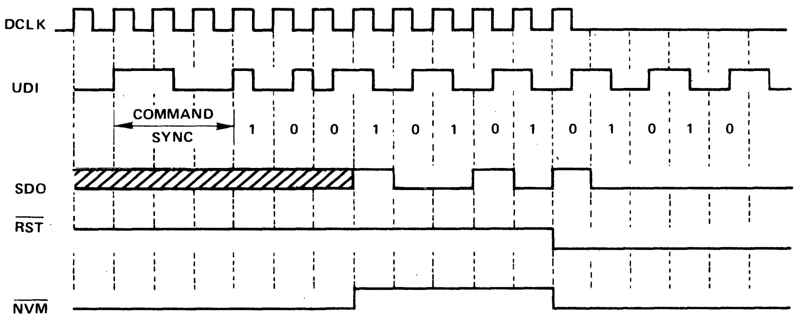
The Manchester II encoded data can be presented to the decoder in either of two ways. The Bipolar One and Bipolar Zero inputs will accept data from differential inputs such as a comparator sensed transformer coupled bus. The Unipolar Data input can only accept noninverted Manchester II encoded data i.e. $\overline{\text{Bipolar One Out}}$ through an inverter to Unipolar Data Input. The decoder continuously monitors this data input for a valid sync pattern. Note that while the MED encoder section can generate only a command sync pattern, the decoder can recognize either a command or data sync pattern. A data sync is a logically inverted command sync.

There is a three bit delay between UDI, BOI or BZI input and the decoded NRZ data transmitted out of SDO.

Control of the decoder outputs is provided by the $\overline{RST}$ pin. When $\overline{RST}$ is low, SDO, DCLK and $\overline{NVM}$ are forced low. When $\overline{RST}$ is high, SDO is transmitted out synchronously with the recovered clock DCLK. The $\overline{NVM}$ output remains low after a low to high transition on $\overline{RST}$ until a valid sync pattern is received.

The decoded data at SDO is in NRZ format. DCLK is provided so that the decoded bits can be shifted into an external register on every high to low transition of this clock.

Three bit periods after an invalid Manchester bit is received on UDI, or BOI, $\overline{NVM}$ goes low synchronously with the questionable data output on SDO. FURTHER, THE DECODER DOES NOT REESTABLISH PROPER DATA DECODING UNTIL ANOTHER SYNC PATTERN IS RECOGNIZED



For expanded view see Figure 9.

FIGURE 2.

Repeater Mode

Manchester II data can be presented to the repeater in either of two ways. The inputs Bipolar One In and Bipolar Zero In will accept data from differential inputs such as a comparator or sensed transformer coupled bus. The input Unipolar Data In accepts only non-inverted Manchester II coded data. The decoder requires a single clock with a frequency 16X or 32X the desired data rate. This clock is selected to 16X with Speed Select low and 32X with Speed Select high. For long data links the 32X mode should be used as this permits a wider timing jitter margin.

The inputs UDI, or BOI, BZI are delayed approximately 1/2 bit period and repeated as outputs $\overline{BOO}$ and $\overline{BZO}$. The 2X ECLK is transmitted out of the repeater synchronously with $\overline{BOO}$ and $\overline{BZO}$.

A low on $\overline{CTS}$ enables ECLK, $\overline{BOO}$, and $\overline{BZO}$. In contrast to the converter mode, a transition on $\overline{CTS}$ does not initiate a synchronization sequence of eight 0's and a command sync. The repeater mode does recognize a command or data sync pulse. SD/CDS is an output which reflects the state of the most recent sync pulse received, with high indicating a command sync and low indicating a data sync.

When $\overline{RST}$ is low, the outputs SDO, DCLK, and $\overline{NVM}$ are low, and $\overline{SRST}$ is set low. $\overline{SRST}$ remains low after $\overline{RST}$ goes high and is not reset until a sync pulse and two valid manchester bits are received with the reset bit low. The reset bit is the first data bit after the sync pulse. With RST high, NRZ Data is transmitted out of Serial Data Out synchronously with the 1X DCLK.

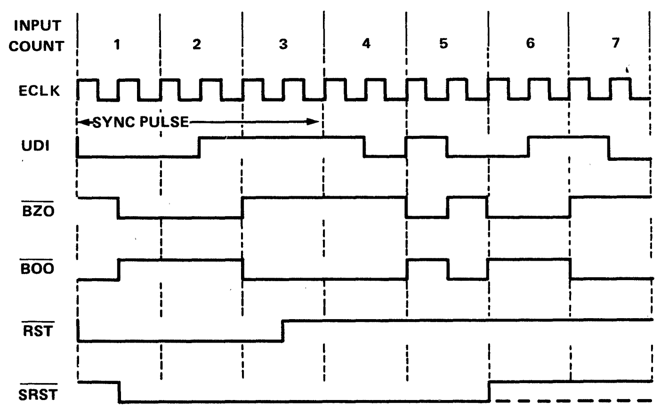


FIGURE 3.

Switching Waveforms

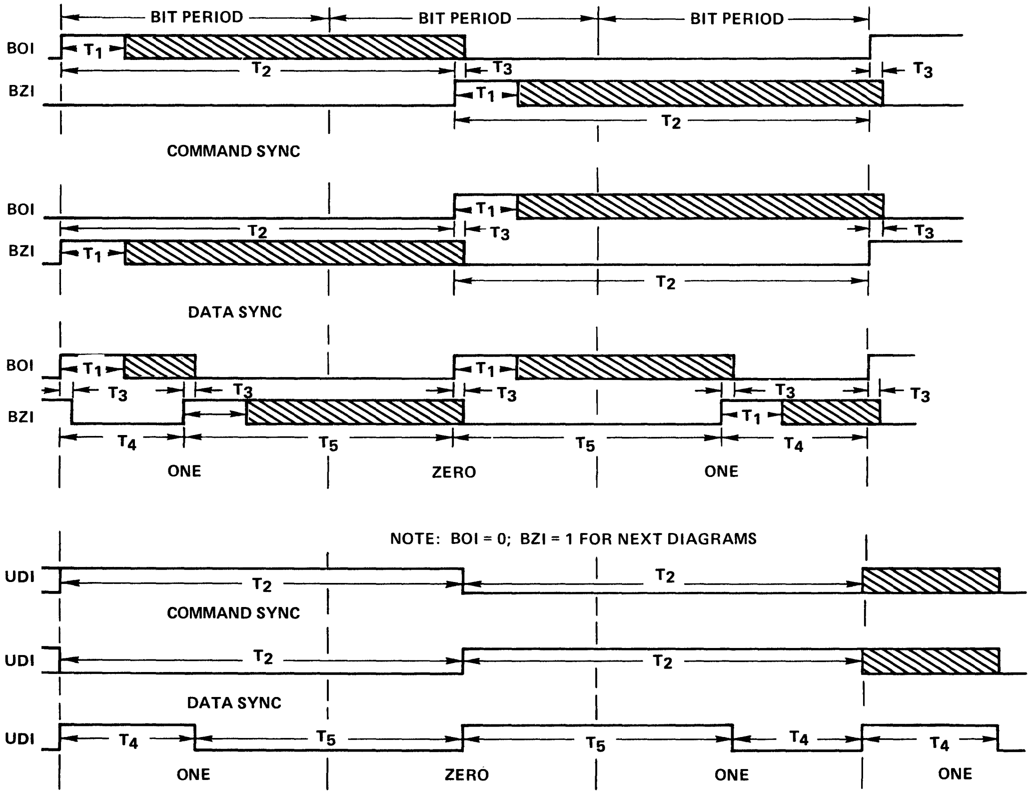


FIGURE 4.

A.C. Testing Input, Output Waveform

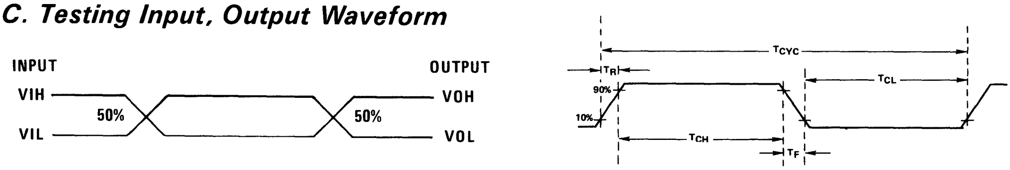


FIGURE 5.

A.C. Testing: All input signals must switch between VIL and VIH. Input rise and fall times are driven in 1nsec per volt.

FIGURE 6.

NOTE: Reference parameters t_6, t_7, t_8, t_9

Encoder Timing

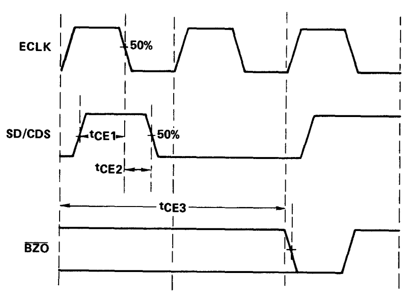
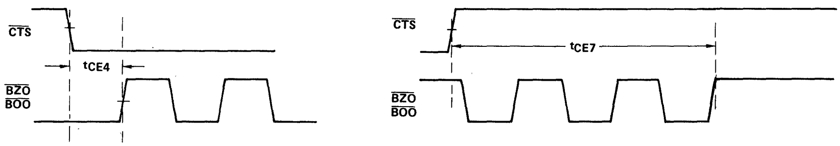


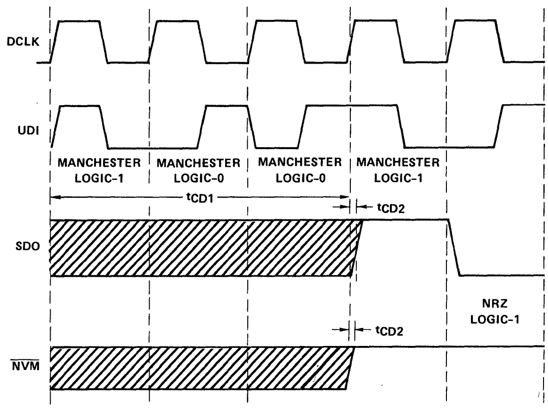
FIGURE 7.



NOTE: t_{CE5} – See Figure 1
t_{CE6} – See Figure 1

FIGURE 8.

Decoder Timing



NOTE: Manchester Data In is not synchronous with Decoder Clock.
Decoder Clock is synchronous with decoded NRZ out of SDO.

FIGURE 9.

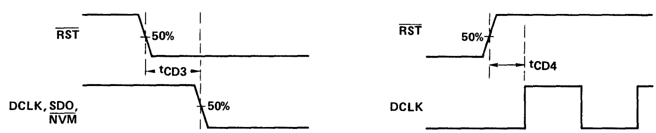


FIGURE 10.

Repeater Timing

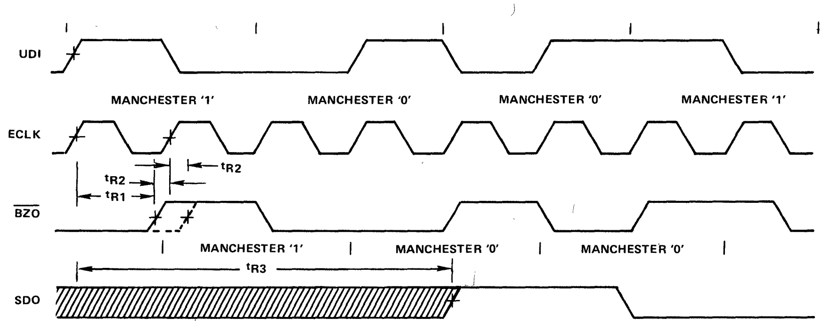


FIGURE 11.

MANCHESTER CODE

Nonreturn to Zero (NRZ) code represents the binary values logic-0 and logic-1 with a static level maintained throughout the data cell. In contrast, Manchester code represents data with a level transition in the middle of the data cell. Manchester has bandwidth, error detection, and synchronization advantages over NRZ code.

The Manchester II code Bipolar One and Bipolar Zero shown below are logical complements. The direction of the transition indicates the binary value of data. A logic-0 in Bipolar One is defined as a low to high transition in the middle of the data cell, and a logic-1 as a high to low mid bit transition. Manchester II is also known as Biphase-L code.

The bandwidth of NRZ is from DC to the clock frequency fc/2, while that of Manchester is from fc/2 to fc. Thus, Manchester can be AC or transformer coupled, which has considerable advantages over DC coupling. Also, the ratio of maximum to minimum frequency of Manchester extends one octave, while the ratio for NRZ is the range of 5-10 octaves. It is much easier to design a narrow band than a wideband amp.

Secondly, the mid bit transition in each data cell provides the code with an effective error detection scheme. If noise produces a logic inversion in the data cell such that there is no transition, an error indiction is given, and synchronization must be re-established. This places relatively stringent requirements on the incoming data.

The synchronization advantages of using the HD-6409 and Manchester code are several fold. One is that Manchester is a self clocking code. The clock in serial data communication defines the position of each data cell. Non self clocking codes, as NRZ, often require an extra clock wire or clock track (in magnetic recording). Further, there can be a phase variation between the clock and data track. Crosstalk between the two may be a problem. In Manchester, the serial data stream contains both the clock and the data, with the position of the mid bit transition representing the clock, and the direction of the transition representing data. There is no phase variation between the clock and the data.

A second synchronization advantage is a result of the number of transitions in the data. The decoder resynchronizes on each transition, or at least once every data cell. In contrast, receivers using NRZ, which does not necessarily have transitions, must resynchronize on frame bit transitions, which occur far less often, usually on a character basis. This more frequent resynchronization eliminates the cumulative effect of errors over sucessive data cells. A final synchronization advantage concerns the HD-6409's sync pulse used to initiate synchronization. This three bit wide pattern is sufficiently distinct from Manchester data that a false start by the receiver is unlikely.

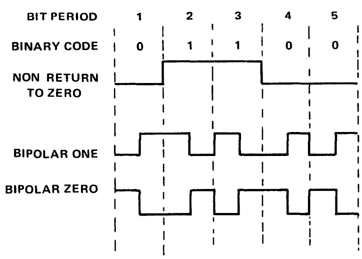
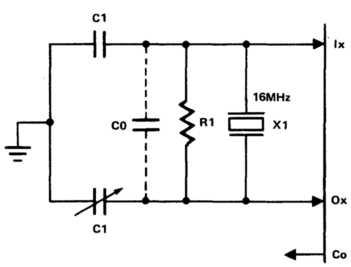


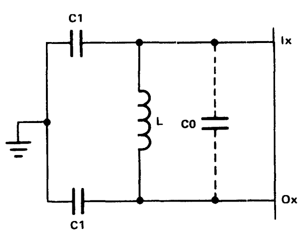
FIGURE 12.

Crystal Oscillator Mode



C1 = 32pF
C0 = Crystal + Stray
X1 = AT CUT PARALLEL RESONANCE FUNDAMENTAL MODE
Rs (TYP) = 30Ω
R1 = 15MΩ

LC Oscillator Mode



C1 = 20pF
C0 = 5pF

$$C_e \approx \frac{C1 - 2C0}{2}$$

$$f_o \approx \frac{1}{2\pi\sqrt{LC_e}}$$

HD-15530

CMOS Manchester Encoder-Decoder

Features

- Support of MIL-STD-1553
- 1.25 Megabit/Sec Data Rate
- Sync Identification and Lock-in
- Clock Recovery
- Manchester II Encode, Decode
- Separate Encode and Decode
- Low Operating Power .... 50mW @ 5 Volts
- Full -55°C to +125°C Temperature Range Operation

Description

The Harris HD-15530 is a high performance CMOS device intended to service the requirements of MIL-STD-1553 and similar Manchester II encoded, time division multiplexed serial data protocols. This LSI chip is divided into two sections, an Encoder and a Decoder. These sections operate completely independent of each other, except for the Master Reset functions.

This circuit meets many of the requirements of MIL-STD-1553. The Encoder produces the sync pulse and the parity bit as well as the encoding of the data bits.

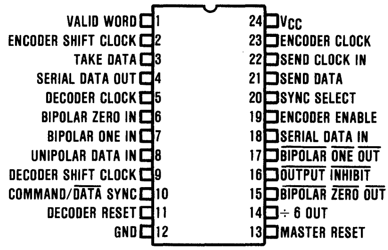
The Decoder recognizes the sync pulse and identifies it as well as decoding the data bits and checking parity.

This integrated circuit is fully guaranteed to support the 1MHz data rate of MIL-STD-1553 over both temperature and voltage. It interfaces with CMOS, TTL or N channel support circuitry, and uses a standard 5 volt supply.

The HD-15530 can also be used in many party line digital data communications applications, such as an environmental control system driven from a single twisted pair cable of fiber optic cable throughout the building.

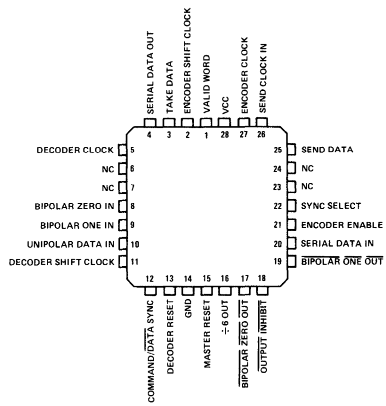
Pinouts

TOP VIEW



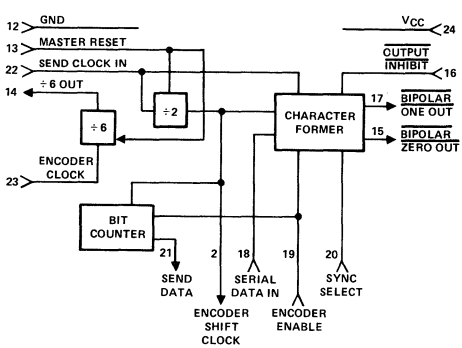
LCC

TOP VIEW

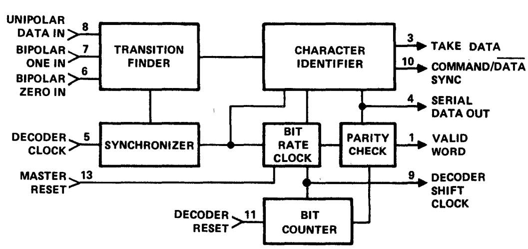


Block Diagrams

ENCODER



DECODER



Caution: These devices are sensitive to electronic discharge. Proger I.C. handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage .... +7.0 Volts
Input, Output or I/O Voltage Applied .... GND -0.3V to VCC +0.3V
Storage Temperature Range .... -65°C to +150°C
Maximum Package Power Dissipation .... 1 Watt
θ_{jc} .... 18°C/W (CERDIP package), 22°C/W (LCC package)
θ_{ja} .... 55°C/W (CERDIP package), 60°C/W (LCC package)
Gate Count .... 225 Gates
Junction Temperature .... +150°C
Lead Temperature (Soldering, Ten Seconds) .... +260°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +4.5V to +5.5V
Operating Temperature Range
HD-15530-9 .... -40°C to +85°C
HD-15530-2/-8 .... -55°C to +125°C

Electrical Specifications T_A = -40°C to +85°C (HD-15530-9), T_A = 55°C to +125°C (HD-15530-2/-8)

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
D.C.	V_{IH}	Logical "1" Input Voltage	70% V_{CC}			V	
	V_{IL}	Logical "0" Input Voltage			20% V_{CC}	V	
	V_{IHC}	Logical "1" Input Voltage (Clock)	V_{CC} -0.5			V	
	V_{ILC}	Logical "0" Input Voltage (Clock)			GND +0.5	V	
	II	Input Leakage	-1.0		+1.0	μA	V_{IN} = V_{CC} or GND, DIP Pins 5-8, 11, 13, 16, 18, 19, 20, 22, 23
	V_{OH}	Logical "1" Output Voltage	2.4			V	I_{OH} = -3mA
	V_{OL}	Logical "0" Output Voltage			0.4	V	I_{OL} = 1.8mA
	I_{CCSB}	Supply Current Standby		0.5	2.0	mA	V_{IN} = V_{CC} = 5.5V Outputs Open
	I_{CCOP}	Supply Current Operating *		8.0	10.0	mA	V_{CC} = 5.5V f = 15MHz
		*Guaranteed and sampled but not 100% tested					
ENCODER TIMING	V_{CC} = 5.0V ± 10%						
A.C.	F_{EC}	Encoder Clock Frequency	0		15	MHz	C_L = 50pF
	F_{ESC}	Send Clock Frequency	0		2.5	MHz	↓
	T_{ECR}	Encoder Clock Rise Time			8	ns	↓
	T_{ECF}	Encoder Clock Fall Time			8	ns	↓
	F_{ED}	Data Rate	0		1.25	MHz	↓
	T_{MR}	Master Reset Pulse Width	150			ns	↓
	T_{E1}	Shift Clock Delay			125	ns	↓
	T_{E2}	Serial Data Setup	75			ns	↓
	T_{E3}	Serial Data Hold	75			ns	↓
	T_{E4}	Enable Setup	90			ns	↓
	T_{E5}	Enable Pulse Width	100			ns	↓
	T_{E6}	Sync Setup	55			ns	↓
	T_{E7}	Sync Pulse Width	150			ns	↓
	T_{E8}	Send Data Delay	0		50	ns	↓
	T_{E9}	Bipolar Ouput Delay			130	ns	↓
	T_{E10}	Enable Hold	10			ns	↓
	T_{E11}	Sync Hold	95			ns	↓
DECODER TIMING	V_{CC} = 5.0V ± 10%						
A.C.	F_{DC}	Decoder Clock Frequency	0		15	MHz	C_L = 50pF
	T_{DCR}	Decoder Clock Rise Time			8	ns	↓
	T_{DCF}	Decoder Clock Fall Time			8	ns	↓
	F_{DD}	Data Rate	0		1.25	MHz	↓
	T_{DR}	Decoder Reset Pulse Width	150			ns	↓
	T_{DRS}	Decoder Reset Setup Time	75			ns	↓
	T_{DRH}	Decoder Reset Hold Time	10			ns	↓
	T_{MR}	Master Reset Pulse	150			ns	↓
	T_{D1}	Bipolar Data Pulse Width	T_{DC} +10			ns	(Note 1)
	T_{D2}	Sync Transition Span		$18T_{DC}$		ns	(Note 1)
	T_{D3}	One Zero Overlap			T_{DC} -10	ns	(Note 1)
	T_{D4}	Short Data Transition Span		$6T_{DC}$		ns	(Note 1)
	T_{D5}	Long Data Transition Span		$12T_{DC}$		ns	(Note 1)
	T_{D6}	Sync Delay (ON)	-20		110	ns	↓
	T_{D7}	Take Data Delay (ON)	0		110	ns	↓
	T_{D8}	Serial Data Out Delay			80	ns	↓
	T_{D9}	Sync Delay (OFF)	0		110	ns	↓
	T_{D10}	Take Data Delay (OFF)	0		110	ns	↓
	T_{D11}	Valid Word Delay	0		110	ns	↓

NOTE 1. TDC = Decoder Clock Period = $\frac{1}{FDC}$ (These parameters are guaranteed but not 100% tested)

Capacitance T_A = 25°C; V_{CC} = GND = 0V; V_{IN} = +5V or GND

SYMBOL	PARAMETER	TYPICAL	UNITS	CONDITIONS
C_{IN}	Input Capacitance	5.0	pF	
C_O	Output Capacitance	8.0	pF	

Pin Description

PIN NUMBER	TYPE	NAME	SECTION	DESCRIPTION
1	O	VALID WORD	Decoder	Output high indicates receipt of a valid word, (valid parity and no Manchester errors).
2	O	ENCODER SHIFT CLOCK	Encoder	Output for shifting data into the Encoder. The Encoder samples SDI on the low-to-high transition of Encoder Shift Clock.
3	O	TAKE DATA	Decoder	Output is high during receipt of data after identification of a sync pulse and two valid Manchester data bits.
4	O	SERIAL DATA OUT	Decoder	Delivers received data in correct NRZ format.
5	I	DECODER CLOCK	Decoder	Input drives the transition finder, and the synchronizer which in turn supplies the clock to the balance of the decoder, input a frequency equal to 12X the data rate.
6	I	BIPOLAR ZERO IN	Decoder	A high input should be applied when the bus is in its negative state. This pin must be held high when the Unipolar input is used.
7	I	BIPOLAR ONE IN	Decoder	A high input should be applied when the bus is in its positive state. This pin must be held low when the Unipolar input is used.
8	I	UNIPOLAR DATA IN	Decoder	With pin 6 high and pin 7 low, this pin enters unipolar data into the transition finder circuit. If not used this input must be held low.
9	O	DECODER SHIFT CLOCK	Decoder	Output which delivers a frequency (DECODER CLOCK ÷ 12), synchronized by the recovered serial data stream.
10	O	COMMAND SYNC	Decoder	Output of a high from this pin occurs during output of decoded data which was preceded by a Command (or Status) synchronizing character. A low output indicates a Data synchronizing character.
11	I	DECODER RESET	Decoder	A high input to this pin during a rising edge of DECODER SHIFT CLOCK resets the decoder bit counting logic to a condition ready for a new word.
12	I	GROUND	Both	Ground Supply pin.
13	I	MASTER RESET	Both	A high on this pin clears 2:1 counters in both Encoder and Decoder, and resets the ÷ 6 circuit.
14	O	÷ 6 OUT	Encoder	Output from 6:1 divider which is driven by the ENCODER CLOCK.
15	O	$\overline{\text{BIPOLAR}}$ $\overline{\text{ZERO}}$ $\overline{\text{OUT}}$	Encoder	An active low output designed to drive the zero or negative sense of a bipolar line driver.
16	I	$\overline{\text{OUTPUT}}$ $\overline{\text{INHIBIT}}$	Encoder	A low on this pin forces pin 15 and 17 high, the inactive states.
17	O	$\overline{\text{BIPOLAR}}$ $\overline{\text{ONE}}$ $\overline{\text{OUT}}$	Encoder	An active low output designed to drive the one or positive sense of a bipolar line driver.
18	I	SERIAL DATA IN	Encoder	Accepts a serial data stream at a data rate equal to ENCODER SHIFT CLOCK.
19	I	ENCODER ENABLE	Encoder	A high on this pin initiates the encode cycle. (Subject to the preceeding cycle being complete.)
20	I	SYNC SELECT	Encoder	Actuates a Command sync for an input high and Data sync for an input low.
21	O	SEND DATA	Encoder	An active high output which enables the external source of serial data.
22	I	SEND CLOCK IN	Encoder	Clock input at a frequency equal to the data rate X2, usually driven by ÷ 6 output.
23	I	ENCODER CLOCK	Encoder	Input to the 6:1 divider, a frequency equal to the data rate X12 is usually input here.
24	I	V_{CC}	Both	VCC is the +5V power supply pin. A $0.1\mu F$ decoupling capacitor from V_{CC} (pin 24) to GROUND (pin 12) is recommended.

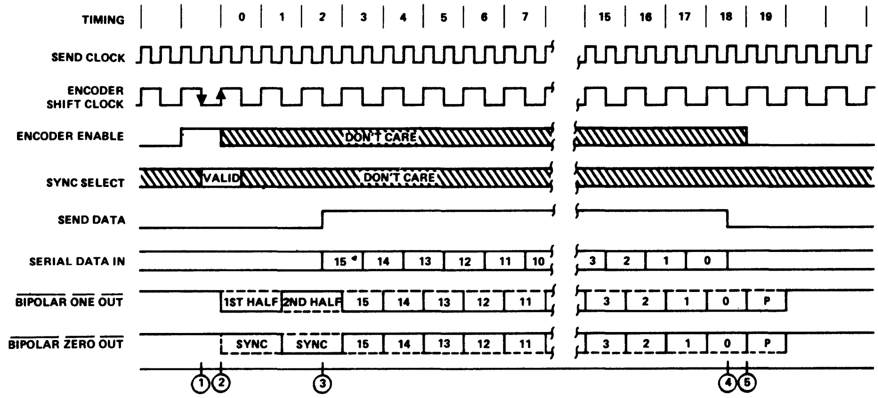
I = Input O = Output

Encoder Timing

The Encoder requires a single clock with a frequency of twice the desired data rate applied at the SEND CLOCK input. An auxiliary divide by six counter is provided on chip which can be utilized to produce the SEND CLOCK by dividing the DECODER CLOCK.

The Encoder's cycle begins when ENCODER ENABLE is high during a falling edge of ENCODER SHIFT CLOCK ①. This cycle lasts for one word length or twenty ENCODER SHIFT CLOCK periods. At the next low-to-high transition of the ENCODER SHIFT CLOCK, a high SYNC SELECT input actuates a command sync or a low will produce a data sync for the word ②. When the Encoder is ready to accept data, the SEND DATA output will go high and remain high for sixteen ENCODER SHIFT CLOCK periods ③. During these sixten periods the data should be clocked into the SERIAL DATA input with every high-to-low transition of the ENCODER SHIFT CLOCK so it can be sampled on the low-to-high transition ③ - ④. After the sync and Manchester II coded data are transmitted through the BIPOLAR ONE and BIPOLAR ZERO outputs, the Encoder adds on an additional bit which is the parity for that word ⑤. If ENCODER ENABLE is held high continuously, consecutive words will be encoded without an interframe gap. ENCODER ENABLE must go low by time ⑤ as shown to prevent a consecutive word from being encoded. At any time a low on OUTPUT INHIBIT input will force both bipolar outputs to a high state but will not affect the Encoder in any other way.

To abort the Encoder transmission a positive pulse must be applied at MASTER RESET. Anytime after or during this pulse, a low-to-high transition on SEND CLOCK clears the internal counters and initializes the Encoder for a new word.



Decoder Timing

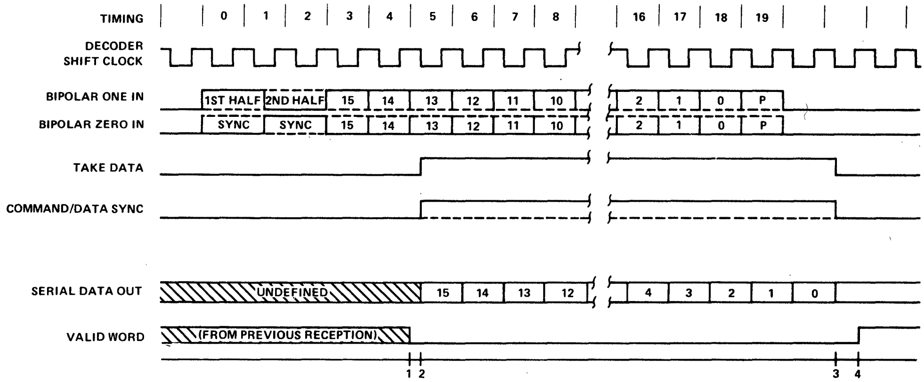
The Decoder requires a single clock with a frequency of 12 times the desired data rate applied at the DECODER CLOCK input. The Manchester II coded data can be presented to the Decoder in one of two ways. The BIPOLAR ONE and BIPOLAR ZERO inputs will accept data from a comparator sensed transformer coupled bus as specified in Military Spec 1553. The UNIPOLAR DATA input can only accept non-inverted Manchester II coded data. (e.g. from BIPOLAR ONE OUT of an Encoder through an inverter to Unipolar Data Input).

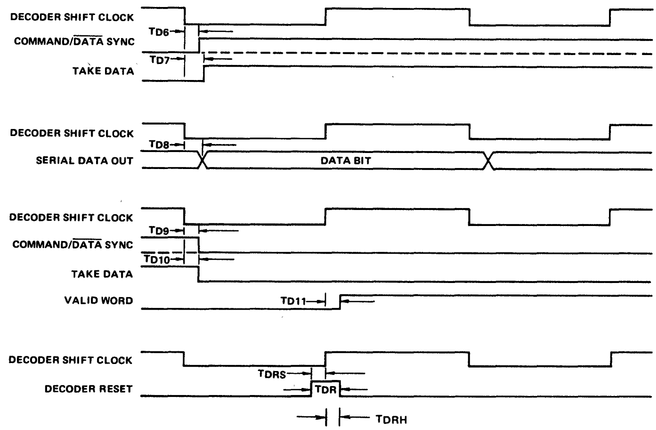
The Decoder is free running and continuously monitors its data input lines for a valid sync character and two valid Manchester data bits to start an output cycle. When a valid sync is recognized ①, the type of sync is indicated on COMMAND/DATA SYNC output. If the sync character was a command sync, this output will go high ② and remain high for sixten DECODER SHIFT CLOCK periods ③, otherwise it will remain low. The TAKE DATA output will go high and remain high ② - ③ while the Decoder is transmitting the decoded data through SERIAL DATA OUT. The decoded data available at SERIAL DATA OUT is in NRZ format. The DECODER SHIFT CLOCK is provided so that the decoded bits can be shifted into an external register on every low-to-high transition of this clock ② - ③. Note that DECODER SHIFT CLOCK may adjust its phase up until the time that TAKE DATA goes high.

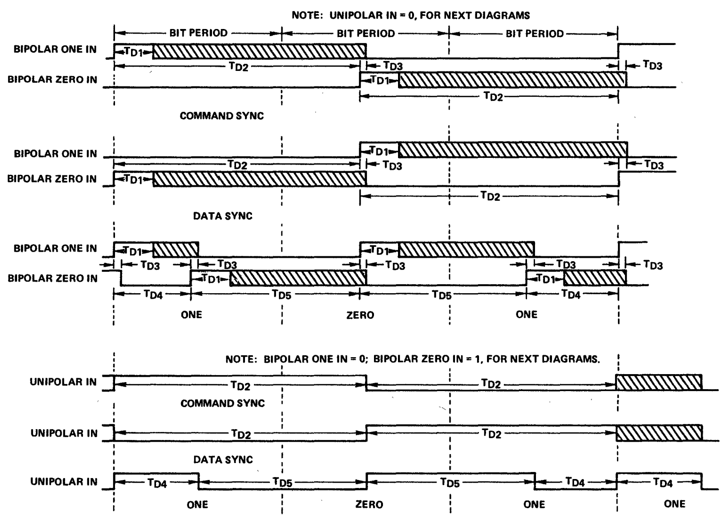
After all sixteen decoded bits have been transmitted ③ the data is checked for odd parity. A high on VALID WORD output ④ indicates a successful reception of a word without any Manchester or parity errors. At this time the Decoder is looking for a new sync character to start another output sequence. VALID WORD will go low approximately 20 DECODER SHIFT CLOCK periods after it goes high if not reset low sooner by a valid sync and two valid Manchester bits as shown ①.

At any time in the above sequence a high input on DECODER RESET during a low-to-high transition of DECODER SHIFT CLOCK will abort transmission and initialize the Decoder to start looking for a new sync character.

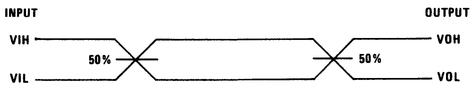
Decoder Timing





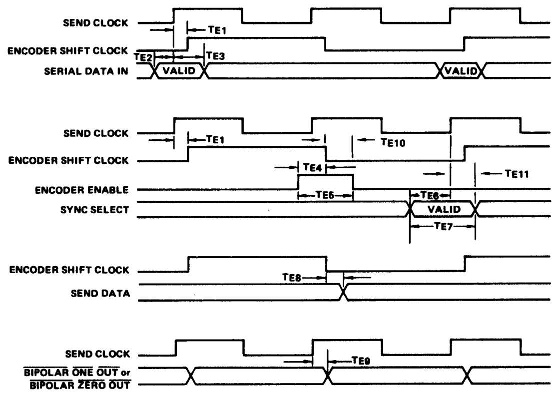


A. C. Testing Input, Output Waveform



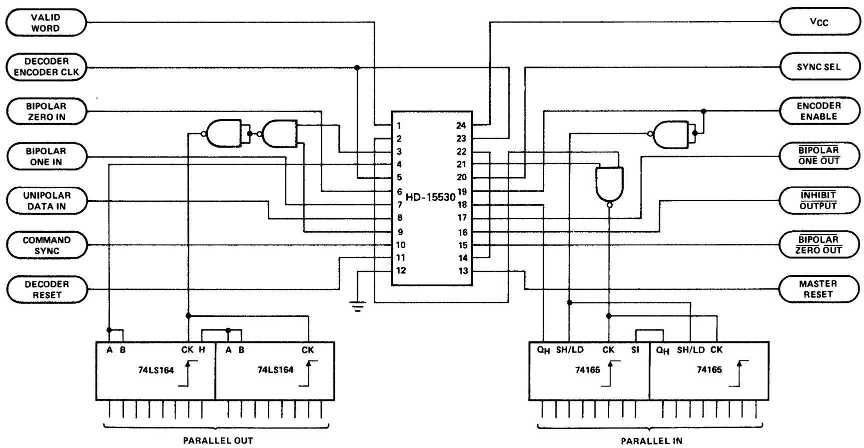
A.C. Testing: All input signals must switch between VIL and VIH. Input rise and fall times are driven at 1 nsec per volt.

Encoder Timing

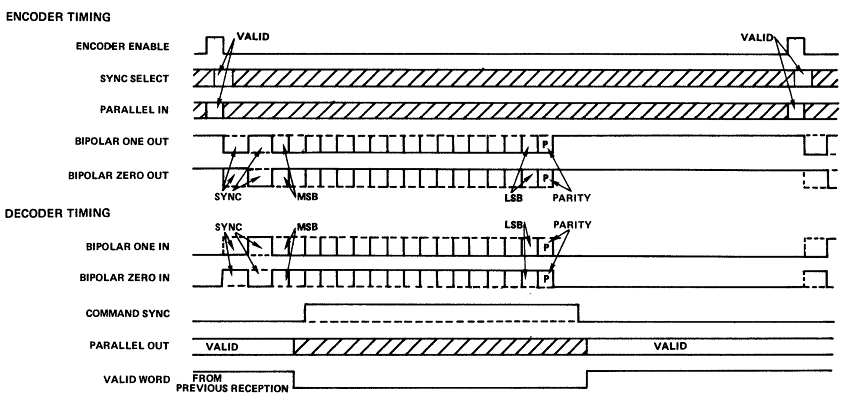


Applications

How to Make Our MTU Look Like a Manchester Encoded UART



Typical Timing Diagram for a Manchester Encoded UART



HOW TO MAKE OUR MTU LOOK LIKE A MANCHESTER ENCODED UART

HD-15530

4
DATA COMMUNICATIONS

MIL-STD-1553

The 1553 standard defines a time division multiplexed data bus for application within aircraft. The bus is defined to be bipolar, and encoded in a Manchester II format, so no DC component appears on the bus. This allows transformer coupling and excellent isolation among systems and their environment.

The HD-15530 supports the full bipolar configuration, assuming a bus driver configuration similar to that in Figure 1. Bipolar inputs from the bus, like Figure 2, are also accommodated.

The signaling format in MIL-STD-1553 is specified on the assumption that the network of 32 or fewer terminals are controlled by a central control unit by means of Command Words. Terminals respond with Status Words. Each word is preceded by a synchronizing pulse, and followed by parity bit, occupying a total of 20μsec. The word formats are shown in Figure 4. The special abbreviations are as follows:

P Parity, which is defined to be odd, taken across all 17 bits.

R/T Receive on logical zero, transmit on ONE.

ME Message Error if logical 1.

TF Terminal Flag, if set, calls for controller to request self-test data.

The paragraphs above are intended only to suggest the content of MIL-STD-1553, and do not completely describe its bus requirements, timing or protocols.

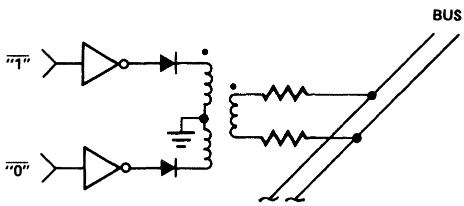


FIGURE 1. SIMPLIFIED MIL-STD-1553 DRIVER

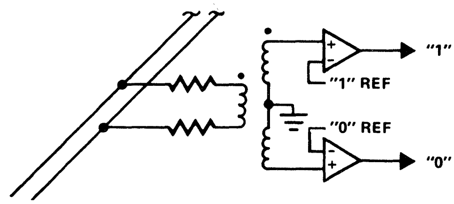


FIGURE 2. SIMPLIFIED MIL-STD-1553 RECEIVER

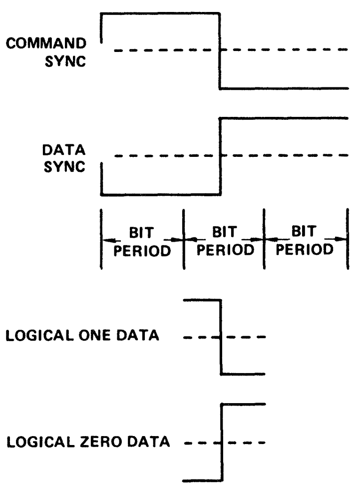


FIGURE 3. MIL-STD-1553 CHARACTER FORMATS

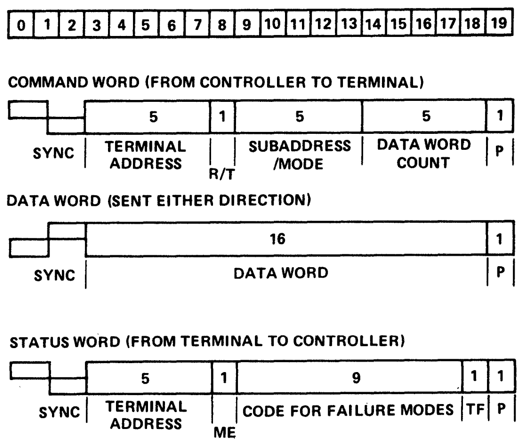


FIGURE 4. MIL-STD-1553 WORD FORMATS

NOTE: This page is a summary of MIL-STD-1553 and is not intended to describe the operation of the HD-15530.

HARRIS

HD-15531

CMOS Manchester Encoder-Decoder

Features

- Support of MIL-STD-1553
- 2.5 Megabit/Sec Data Rate (15531B)
- 1.25 Megabit/Sec Data Rate (15531)
- Sync Identification and Lock-in
- Clock Recovery
- Variable Frame Length to 32-Bits
- Manchester II Encode, Decode
- Separate Encode and Decode
- Low Operating Power .... 50mW @ 5 Volts
- Full -55°C to +125°C Temperature Range Operation

Description

The Harris HD-15531 is a high performance CMOS device intended to service the requirements of MIL-STD-1553 and similar Manchester II encoded, time division multiplexed serial data protocols. This LSI chip is divided into two sections, an Encoder and a Decoder. These sections operate independently of each other, except for the master reset and word length functions.

This circuit provides many of the requirements of MIL-STD-1553. The Encoder produces the sync pulse and the parity bit as well as the encoding of the data bits. The Decoder recognizes the sync pulse and identifies it as well as decoding the data bits and checking parity.

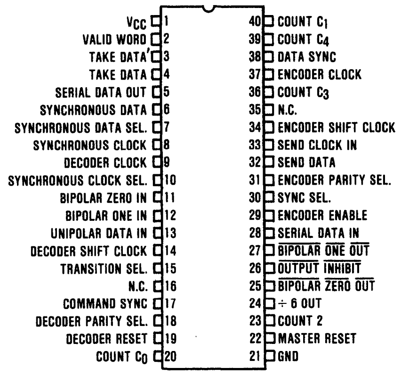
The HD-15531 also surpasses the requirements of MIL-STD-1553 by allowing the word length to be programmable (from 2 to 28 data bits). A frame consists of three bits for sync followed by the data word (2 to 28 data bits) followed by one bit of parity, thus the frame length will vary from 6 to 32 bit periods. This chip also allows selection of either even of odd parity for the Encoder and Decoder separately.

This integrated circuit is fully guaranteed to support the 1MHz data rate of MIL-STD-1553 over both temperature and voltage. For high speed applications the 15531B will support a 2.5 Megabit/sec data rate.

The HD-15531 can also be used in many party line digital data communications applications, such as a local area network or an environmental control system driven from a single twisted pair of fiber optic cable throughout a building.

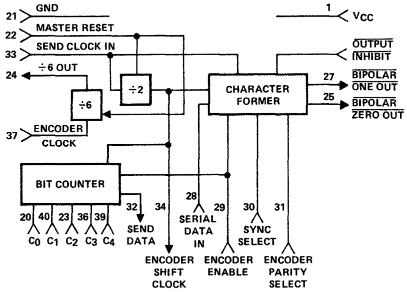
Pinout

TOP VIEW

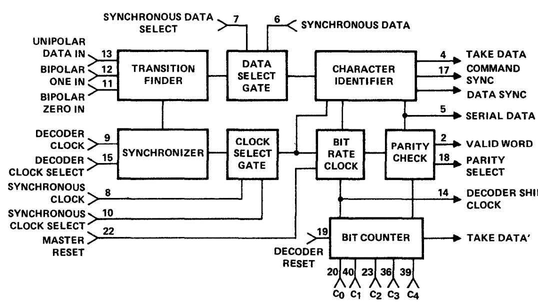


Block Diagrams

ENCODER



DECODER



Absolute Maximum Ratings

Supply Voltage .... +7.0 Volts
Input, Output or I/O Voltage Applied .... GND -0.3V to VCC +0.3V
Storage Temperature Range .... -65°C to +150°C
Maximum Package Power Dissipation .... 1 Watt
θ_{jc} .... 17°C/W (CERDIP package), 23°C/W (LCC package)
θ_{ja} .... 45°C/W (CERDIP package), 50°C/W (LCC package)
Gate Count .... 225 Gates
Junction Temperature .... +150°C
Lead Temperature (Soldering, Ten Seconds) .... +260°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +4.5V to +5.5V
Operating Temperature Range
HD-15531-9 .... -40°C to +85°C
HD-15531-2/-8 .... -55°C to +125°C

Electrical Specifciations T_A = -40°C to +85°C (HD-15531-9), T_A = -55°C to +125°C (HD-15531-2/-8)

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
D.C.	V_{IH}	Logical "1" Input Voltage	70% V_{CC}			V	
	V_{IL}	Logical "0" Input Voltage			20% V_{CC}	V	
	V_{IHC}	Logical "1" Input Voltage (Clock)	V_{CC} -0.5			V	
	V_{ILC}	Logical "0" Input Voltage (Clock)			GND +0.5	V	
	II	Input Leakage	-1.0		+1.0	μA	V_{IN} = V_{CC} or GND, DIP Pins 6-13, 15, 18, 19, 20, 22, 23, 26, 28-31, 33, 36 37, 39, 40
	V_{OH}	Logical "1" Output Voltage	2.4			V	I_{OH} = -3mA
	V_{OL}	Logical "0" Output Voltage			0.4	V	I_{OL} = 1.8mA
	I_{CCSB}	Supply Current Standby		0.5	2.0	mA	V_{IN} = V_{CC} = 5.5V Outputs Open
	I_{CCOP}	Supply Current Operating*		8.0	10.0	mA	V_{CC} = 5.5V f = 15MHz
	C_{IN}	Input Capacitance		5.0		pF	
	C_O	Output Capacitance		8.0		pF	
		*Guaranteed and sampled but not 100% tested					
ENCODER TIMING VCC = 5.0V ± 10%							
A.C.	F_{EC}	Encoder Clock Frequency	0		15	MHz	C_L = 50pF
	F_{ESC}	Send Clock Frequency	0		2.5	MHz	
	T_{ECR}	Encoder Clock Rise Time			8	ns	
	T_{ECF}	Encoder Clock Fall Time			8	ns	
	F_{ED}	Data Rate	0		1.25	MHz	
	T_{MR}	Master Reset Pulse Width	150			ns	
	T_{E1}	Shift Clock Delay			125	ns	
	T_{E2}	Serial Data Setup	75			ns	
	T_{E3}	Serial Data Hold	75			ns	
	T_{E4}	Enable Setup	90			ns	
	T_{E5}	Enable Pulse Width	100			ns	
	T_{E6}	Sync Setup	55			ns	
	T_{E7}	Sync Pulse Width	150			ns	
	T_{E8}	Send Data Delay	0		50	ns	
	T_{E9}	Bipolar Ouput Delay			130	ns	
	T_{E10}	Enable Hold	10			ns	
	T_{E11}	Sync Hold	95			ns	
DECODER TIMING VCC = 5.0V ± 10%							
A.C.	F_{DC}	Decoder Clock Frequency	0		15	MHz	C_L = 50pF
	F_{DS}	Decoder Sync Clock	0		2.5	MHz	
	T_{DCR}	Decoder Clock Rise Time			8	ns	
	T_{DCF}	Decoder Clock Fall Time			8	ns	
	F_{DD}	Data Rate	0		1.25	MHz	
	T_{DR}	Decoder Reset Pulse Width	150			ns	
	T_{DRS}	Decoder Reset Setup Time	75			ns	
	T_{DRH}	Decoder Reset Hold Time	10			ns	
	T_{MR}	Master Reset Pulse	150			ns	
	T_{D1}	Bipolar Data Pulse Width	T_{DC} +10			ns	(Note 1)
	T_{D2}	Sync Transition Span		$18T_{DC}$		ns	(Note 1)
	T_{D3}	One Zero Overlap			TDC -10	ns	(Note 1)
	T_{D4}	Short Data Transition Span		$6T_{DC}$		ns	(Note 1)
	T_{D5}	Long Data Transition Span		$12T_{DC}$		ns	(Note 1)
	T_{D6}	Sync Delay (ON)	-20		110	ns	
	T_{D7}	Take Data Delay (ON)	0		110	ns	
	T_{D8}	Serial Data Out Delay			80	ns	
	T_{D9}	Sync Delay (OFF)	0		110	ns	
	T_{D10}	Take Data Delay (OFF)	0		110	ns	
	T_{D11}	Valid Word Delay	0		110	ns	
	T_{D12}	Sync Clock to Shift Clock Delay			75	ns	
	T_{D13}	Sync Data Setup	75			ns	

NOTE 1. TDC = Decoder Clock Period = $\frac{1}{FDC}$ (These parameters are guaranteed but not 100% tested)

Absolute Maximum Ratings

Supply Voltage .... +7.0 Volts
Input, Output or I/O Voltage Applied .... GND -0.3V to VCC +0.3V
Storage Temperature Range .... -65°C to +150°C
Maximum Package Power Dissipation .... 1 Watt
θ_{jc} .... 17°C/W (CERDIP package), 23°C/W (LCC package)
θ_{ja} .... 45°C/W (CERDIP package), 50°C/W (LCC package)
Gate Count .... 225 Gates
Junction Temperature .... +150°C
Lead Temperature (Soldering, Ten Seconds) .... +260°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +4.5V to +5.5V
Operating Temperature Range
HD-15531B-9 .... -40°C to +85°C
HD-15531B-2/-8 .... -55°C to +125°C

Electrical Specifications T_A = -40°C to +85°C (HD-15531B-9), T_A = -55°C to +125°C (HD-15531B-2/-8)

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
D.C.	V_{IH}	Logical "1" Input Voltage	70% V_{CC}			V	
	V_{IL}	Logical "0" Input Voltage			20% V_{CC}	V	
	V_{IHC}	Logical "1" Input Voltage (Clock)	V_{CC} -0.5			V	
	V_{ILC}	Logical "0" Input Voltage (Clock)			GND +0.5	V	
	II	Input Leakage	-1.0		+1.0	μA	V_{IN} = V_{CC} or GND, DIP Pins 6-13, 15, 18, 19, 20, 22, 23, 26, 28-31, 33, 36, 37, 39, 40
	V_{OH}	Logical "1" Output Voltage	2.4			V	I_{OH} = -3mA
	V_{OL}	Logical "0" Output Voltage			0.4	V	I_{OL} = 1.8mA
	I_{CCSB}	Supply Current Standby		0.5	2.0	mA	V_{IN} = V_{CC} = 5.5V Outputs Open
	I_{CCOP}	Supply Current Operating*		8.0	10.0	mA	V_{CC} = 5.5V f = 15MHz
	C_{IN}	Input Capacitance		5.0		pF	
	C_O	Output Capacitance		8.0		pF	
		*Guaranteed and sampled but not 100% tested					
	ENCODER TIMING VCC = 5.0V ± 10%						
A.C.	F_{EC}	Encoder Clock Frequency	0		30	MHz	C_L = 50pF (applies to all encoder timing)
	F_{ESC}	Send Clock Frequency	0		5.0	MHz	
	T_{ECR}	Encoder Clock Rise Time			8	ns	
	T_{ECF}	Encoder Clock Fall Time			8	ns	
	F_{ED}	Data Rate	0		2.5	MHz	
	T_{MR}	Master Reset Pulse Width	150			ns	
	T_{E1}	Shift Clock Delay			80	ns	
	T_{E2}	Serial Data Setup	50			ns	
	T_{E3}	Serial Data Hold	50			ns	
	T_{E4}	Enable Setup	90			ns	
	T_{E5}	Enable Pulse Width	100			ns	
	T_{E6}	Sync Setup	55			ns	
	T_{E7}	Sync Pulse Width	150			ns	
	T_{E8}	Send Data Delay	0		50	ns	
	T_{E9}	Bipolar Ouput Delay			130	ns	
	T_{E10}	Enable Hold	10			ns	
	T_{E11}	Sync Hold	95			ns	
	DECODER TIMING VCC = 5.0V ± 10%						
A.C.	F_{DC}	Decoder Clock Frequency	0		30	MHz	C_L = 50pF (applies to all decoder timing)
	F_{DS}	Decoder Sync Clock	0		5.0	MHz	
	T_{DCR}	Decoder Clock Rise Time			8	ns	
	T_{DCF}	Decoder Clock Fall Time			8	ns	
	F_{DD}	Data Rate	0		2.50	MHz	
	T_{DR}	Decoder Reset Pulse Width	150			ns	
	T_{DRS}	Decoder Reset Setup Time	75			ns	
	T_{DRH}	Decoder Reset Hold Time	10			ns	
	T_{MR}	Master Reset Pulse	150			ns	
	T_{D1}	Bipolar Data Pulse Width	T_{DC} +10			ns	(Note 1)
	T_{D2}	Sync Transition Span		$18T_{DC}$		ns	(Note 1)
	T_{D3}	One Zero Overlap			TDC -10	ns	(Note 1)
	T_{D4}	Short Data Transition Span		$6T_{DC}$		ns	(Note 1)
	T_{D5}	Long Data Transition Span		$12T_{DC}$		ns	(Note 1)
	T_{D6}	Sync Delay (ON)	-20		110	ns	
	T_{D7}	Take Data Delay (ON)	0		110	ns	
	T_{D8}	Serial Data Out Delay			80	ns	
	T_{D9}	Sync Delay (OFF)	0		110	ns	
	T_{D10}	Take Data Delay (OFF)	0		110	ns	
	T_{D11}	Valid Word Delay	0		110	ns	
	T_{D12}	Sync Clock to Shift Clock Delay			75	ns	
	T_{D13}	Sync Data Setup	75			ns	

NOTE 1. TDC = Decoder Clock Period = $\frac{1}{FDC}$ (These parameters are guaranteed but not 100% tested)

Pin Description

PIN NUMBER	TYPE	NAME	SECTION	DESCRIPTION
1		V_{CC}	Both	Positive supply pin. A 0.1μF decoupling capacitor from V_{CC} (pin 1) to GROUND (pin 21) is recommended.
2	O	VALID WORD	Decoder	Output high indicateds receipt of a valid word, (valid parity and no Manchester errors).
3	O	TAKE DATA'	Decoder	A continuous, free running signal provided for host timing or data handling. When data is present on the bus, this signal will be synchronized to the incoming data and will be identical to take data.
4	O	TAKE DATA	Decoder	Output is high during receipt of data after identification of a valid sync pulse and two valid Manchester bits.
5	O	SERIAL DATA OUT	Decoder	Delivers received data in correct NRZ format.
6	I	SYNCHRONOUS DATA	Decoder	Input presents Manchester data directly to character identification logic. SYNCHRONOUS DATA SELECT must be held high to use this input. If not used this pin must be held high.
7	I	SYNCHRONOUS DATA SELECT	Decoder	In high state allows the synchronous data to enter the character identification logic. Tie this input low for asynchronous data.
8	I	SYNCHRONOUS CLOCK	Decoder	Input provides externally synchronized clock to the decoder, for use when receiving synchronous data. This input must be tied high when not in use.
9	I	DECODER CLOCK	Decoder	Input drives the transition finder, and the synchronizer which in turn supplies the clock to the balance of the decoder. Input a frequency equal to 12X the data rate.
10	I	SYNCHRONOUS CLOCK SELECT	Decoder	In high state directs the SYNCHRONOUS CLOCK to control the decoder character identification logic. A low state selects the DECODER CLOCK.
11	I	BIPOLAR ZERO IN	Decoder	A high input should be applied when the bus is in its negative state. This pin must be held high when the unipolar input is used.
12	I	BIPOLAR ONE IN	Decoder	A high input should be applied when the bus is in its positive state. This pin must be held low when the unipolar input is used.
13	I	UNIPOLAR DATA IN	Decoder	With pin 11 high and pin 12 low, this pin enters unipolar data into the transition finder circuit. If not used this input must be held low.
14	O	DECODER SHIFT CLOCK	Decoder	Output which delivers a frequency (DECODER CLOCK ÷ 12), synchronous by the recovered serial data stream.
15	I	TRANSITION SELECT	Decoder	A high input to this pin causes the transition finder to synchronize on every transition of input data. A low input causes the transition finder to synchronize only on mid-bit transitions.
16		N.C.	Blank	Not connected.
17	O	COMMAND SYNC	Decoder	Output of a high from this pin occurs during output of decoded data which was preceded by a Command (or Status) synchronizing character.
18	I	DECODER PARITY SELECT	Decoder	An input for parity sense, calling for even parity with input high and odd parity with input low.
19	I	DECODER RESET	Decoder	A high input to this pin during a rising edge of DECODER SHIFT CLOCK resets the decoder bit counting logic to a condition ready for a new word.
20	I	COUNT C_0	Both	One of five binary inputs which establish the total bit count to be encoded or decoded.
21		GROUND	Both	Supply pin.
22	I	MASTER RESET	Both	A high on this pin clears 2:1 counters in both encoder and decoder, and resets the ÷ 6 circuit.
23	I	COUNT C_2	Both	See pin 20.
24	O	÷ 6 OUT	Encoder	Output from 6:1 divider which is driven by the ENCODER CLOCK.
25	O	$\overline{\text{BIPOLAR ZERO OUT}}$	Encoder	An active low output designed to drive the zero or negative sense of a bipolar line driver.
26	I	$\overline{\text{OUTPUT INHIBIT}}$	Encoder	A low on this pin forces pin 25 and 27 high, the inactive states.
27	O	$\overline{\text{BIPOLAR ONE OUT}}$	Encoder	An active low output designed to drive the one or positive sense of a bipolar line driver.
28	I	SERIAL DATA IN	Encoder	Accepts a serial data stream at a data rate equal to ENCODER SHIFT CLOCK.
29	I	ENCODER ENABLE	Encoder	A high on this pin initiates the encode cycle. (Subject to the preceeding cycle being complete.)
30	I	SYNC SELECT	Encoder	Actuates a Command sync for an input high and Data sync for an input low.
31	I	ENCODER PARITY SELECT	Encoder	Sets transmit parity odd for a high input, even for a low input.
32	O	SEND DATA	Encoder	Is an active high output which enables the external source of serial data.
33	I	SEND CLOCK IN	Encoder	Clock input at a frequency equal to the data rate X2, usually driven by ÷ 6 output.
34	O	ENCODER SHIFT CLOCK	Encoder	Output for shifting data into the Encoder. The Encoder samples SDI pin-28 on the low-to-high transition of ESC.
35		N.C.	Blank	Not connected.
36	I	COUNT C3	Both	See pin 20.
37	I	ENCODER CLOCK	Encoder	Input to the 6:1 divider, a frequency equal to 12 times the data rate is usually input here.
38	O	DATA SYNC	Decoder	Output of a high from this pin occurs during output of decoded data which was preceded by a data synchronizing character.
39	I	COUNT C4	Both	See pin 20.
40	I	COUNT C1	Both	See pin 20.

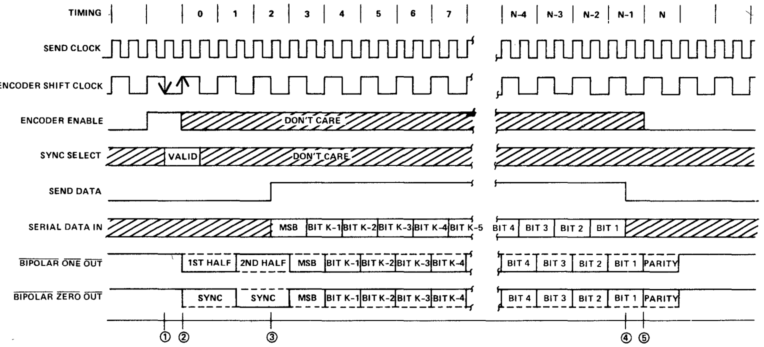
I = Input O = Output

Encoder Operation

The Encoder requires a single clock with a frequency of twice the desired data rate applied at the SEND CLOCK input. An auxiliary divide by six counter is provided on chip which can be utilized to product the SEND CLOCK by dividing the DECODER CLOCK. The frame length is set by programming the COUNT inputs. Parity is selected by programming ENCODER PARITY SELECT high for odd parity or low for even parity.

The Encoder's cycle begins when ENCODER ENABLE is high during a falling edge of ENCODER SHIFT CLOCK ①. This cycle lasts for one word length or K + 4 ENCODER SHIFT CLOCK periods, where K is the number of bits to be sent. At the next low-to-high transition of the ENCODER SHIFT CLOCK, a high SYNC SELECT input actuates a Command sync or a low will produce a Data sync for the word ②. When the Encoder is ready to accept data, the SEND DATA output will go high for K ENCODER SHIFT CLOCK periods ④. During these K periods the data should be clocked into the SERIAL DATA input with every high-to-low transition of the ENCODER SHIFT CLOCK ③ - ④ so it can be sampled on the low-to-high transition. After the sync and Manchester II encoded data are transmitted through the BIPOLAR ONE and BIPOLAR ZERO outputs, the Encoder adds on an additional bit with the parity for that word ⑤. If ENCODER ENABLE is held high continuously, consecutive words will be encoded without an interframe gap. ENCODER ENABLE must go low by time ⑤ (as shown) to prevent a consecutive word from being encoded. At any time a low on OUTPUT INHIBIT input will force both bipolar outputs to a high state but will not affect the Encoder in any other way.

To abort the Encoder transmission a positive pulse must be applied at MASTER RESET. Any time after or during this pulse, a low-to-high transition on SEND CLOCK clears the internal counters and initializes the Encoder for a new word.



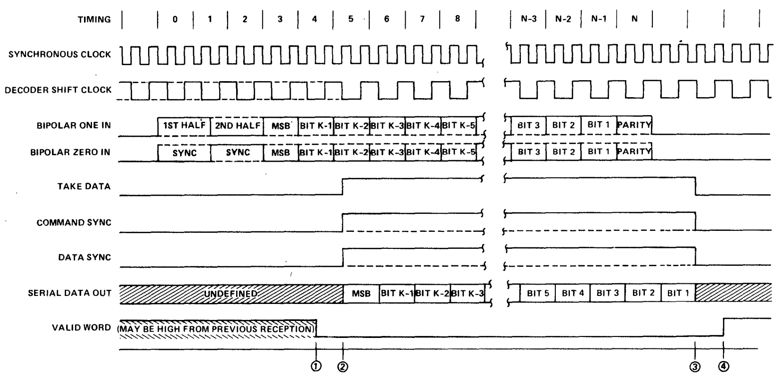
Decoder Operation

To operate the Decoder asynchronously requires a single clock with a frequency of 12 times the desired data rate applied at the DECODER CLOCK input. To operate the Decoder synchronously requires a SYNCHRONOUS CLOCK at a frequency 2 times the data rate which is synchronized with the data at every high-to-low transition applied to the SYNCHRONOUS DATA input. The Manchester II coded data can be presented to the Decoder asynchronously in one of two ways. The BIPOLAR ONE and BIPOLAR ZERO inputs will accept data from a comparator sensed transformer coupled bus as specified in Military Spec 1553. The UNIPOLAR DATA input can only accept noninverted Manchester II coded data. (e.g. from BIPOLAR ONE OUT on an Encoder through an inverter to Unipolar Data Input).

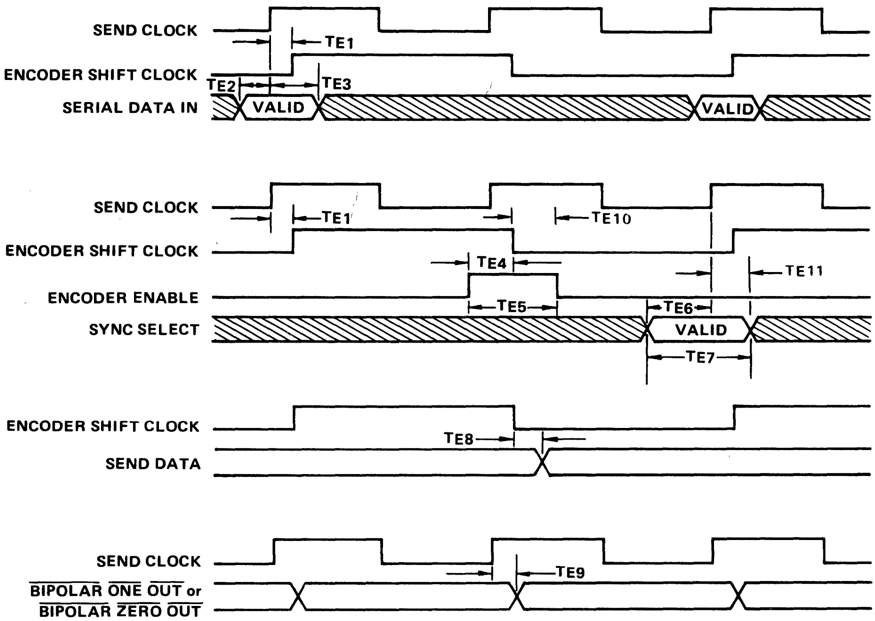
The Decoder is free running and continuously monitors its data input lines for a valid sync character and two valid Manchester data bits to start an output cycle. When a valid sync is recognized ①, the type of sync is indicated by a high level at either COMMAND SYNC or DATA SYNC output. If the sync character was a command sync the COMMAND SYNC output will go high ② and remain high for K SHIFT CLOCK periods ③, where K is the number of bits to be received. If the sync character was a data sync the DATA SYNC output will go high. The TAKE DATA output will go high and remain high ② - ③ while the Decoder is transmitting the decoded data through SERIAL DATA OUT. The decoded data available at SERIAL DATA OUT is in NRZ format. The DECODER SHIFT CLOCK is provided so that the decoded bits can get shifted into an external register on every low-to-high transition of this clock ② - ③. Note that DECODER SHIFT CLOCK may adjust its phase up until the time that TAKE DATA goes high.

After all K decoded bits have been transmitted ③ the data is checked for parity. A high input on DECODER PARITY SELECT will set the Decoder to check for even parity or a low input will set the Decoder to check for odd parity. A high on VALID WORD output ④ indicates a successful reception of a word without any Manchester or parity errors. At this time the Decoder is looking for a new sync character to start another output sequence. VALID WORD will go low approximately K + 4 DECODER SHIFT CLOCK periods after it goes high if not reset low sooner by a valid sync and two valid Manchester bits as shown ①.

At any time in the above sequence a high input on DECODER RESET during a low-to-high transition of DECODER SHIFT CLOCK will abort transmission and initialize the Decoder to start looking for a new sync character.



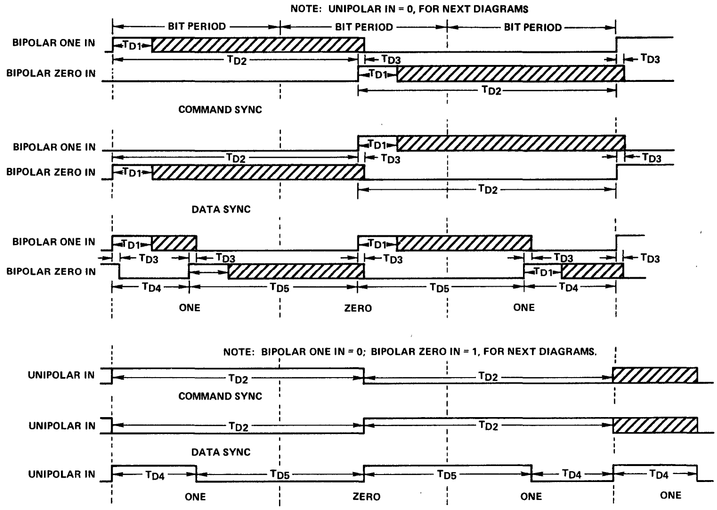
Encoder Timing

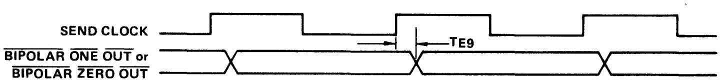


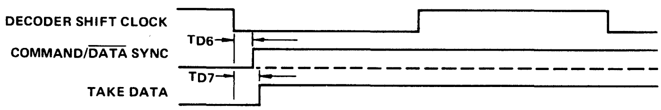
A.C. Testing Input, Output Waveform

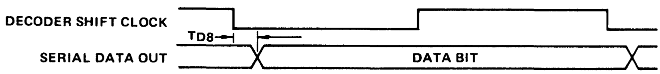
A.C. Testing: All inputs signals must switch between VIL and VIH. Input rise and fall times are driven at 1nsec per volt.

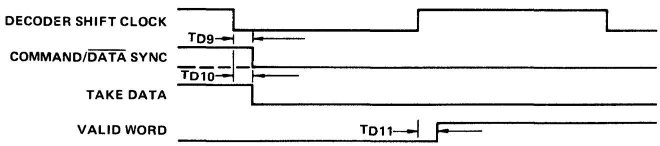
Decoder Timing

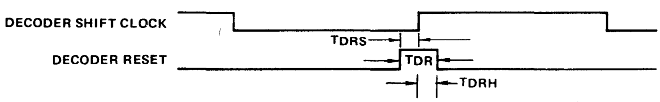


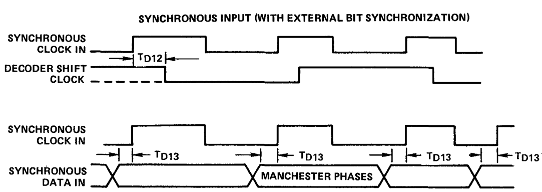












HD-15531

4 DATA COMMUNICATIONS

Frame Counter

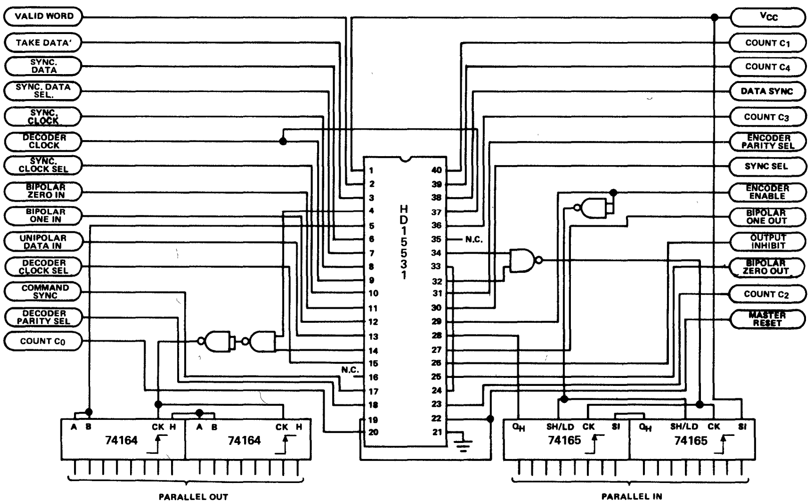
DATA BITS	FRAME LENGTH (BIT PERIODS)	PIN WORD C_4	C_3	C_2	C_1	C_0
2	6	L	L	H	L	H
3	7	L	L	H	H	H
4	8	L	L	H	H	H
5	9	L	H	L	L	L
6	10	L	H	L	L	H
7	11	L	H	L	H	L
8	12	L	H	L	H	H
9	13	L	H	H	L	L
10	14	L	H	H	L	H
11	15	L	H	H	H	L
12	16	L	H	H	H	H
13	17	H	L	L	L	L
14	18	H	L	L	L	H
15	19	H	L	L	H	L

DATA BITS	FRAME LENGTH (BIT PERIODS)	PIN WORD C_4	C_3	C_2	C_1	C_0
16	20	H	L	L	H	H
17	21	H	L	H	L	H
18	22	H	L	H	L	H
19	23	H	L	H	H	L
20	24	H	L	H	H	H
21	25	H	H	L	L	L
22	26	H	H	L	L	H
23	27	H	H	L	H	L
24	28	H	H	L	H	H
25	29	H	H	H	L	L
26	30	H	H	H	L	H
27	31	H	H	H	H	L
28	32	H	H	H	H	H

The above Table demonstrates all possible combinations of frame lengths ranging from 6 to 32 bits. The pin word described here is common to both the Encoder and Decoder.

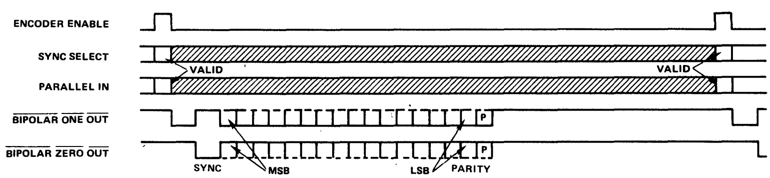
Applications

How to Make Our MTU Look Like a Manchester Encoded UART

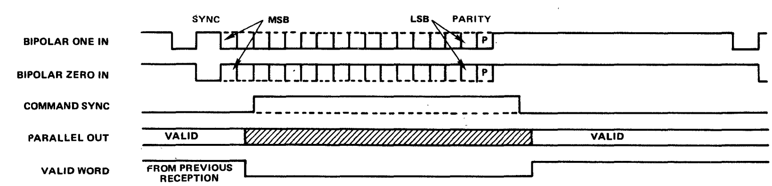


Typical Timing Diagram for a Manchester Encoded UART

ENCODER TIMING



DECODER TIMING



MIL-STD-1553

The 1553 standard defines a time division multiplexed data bus for application within aircraft. The bus is defined to be bipolar, and encoded in a Manchester II format, so no DC component appears on the bus. This allows transformer coupling and excellent isolation among systems and their environment.

The HD-15531 supports the full bipolar configuration, assuming a bus driver configuration similar to that in Figure 1. Bipolar inputs from the bus, like Figure 2, are also accommodated.

The signaling format in MIL-STD-1553 is specified on the assumption that the network of 32 or fewer terminals are controlled by a central control unit by means of Command Words, and Data. Terminals respond with Status Words, and Data. Each word is preceded by a synchronizing pulse, and followed by parity bit, occupying a total of 20μ sec. The word formats are shown in Figure 4. The special abbreviations are as follows:

P — Parity, which is defined to be odd, taken across all 17 bits.

R/T — Receive on logical zero, transmit on ONE.

ME — Message Error if logical 1.

TF — Terminal Flag, if set, calls for controller to request self-test data.

The paragraphs above are intended only to suggest the content of MIL-STD-1553, and do not completely describe its bus requirements, timing or protocols.

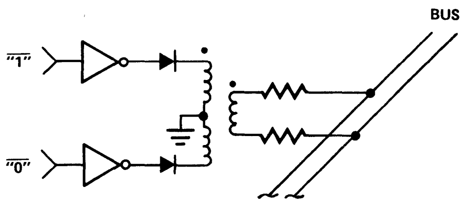


FIGURE 1. SIMPLIFIED MIL-STD-1553 DRIVER

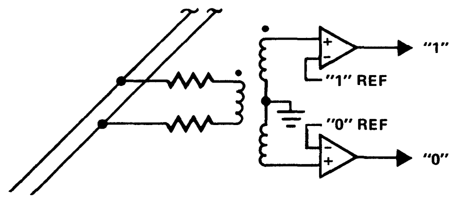


FIGURE 2. SIMPLIFIED MIL-STD-1553 RECEIVER

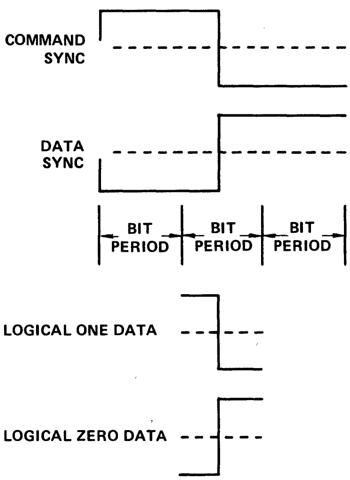


FIGURE 3. MIL-STD-1553 CHARACTER FORMATS

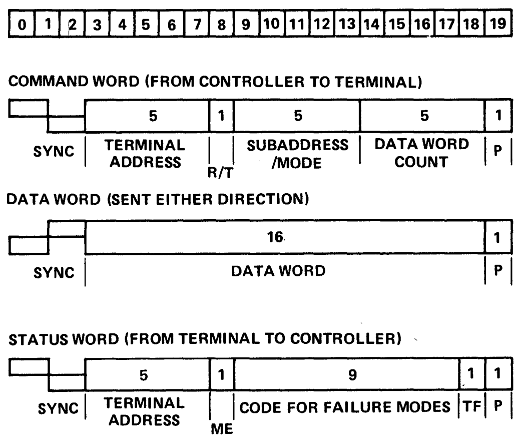


FIGURE 4. MIL-STD-1553 WORD FORMATS

NOTE: This page is a summary of MIL-STD-1553 and is not intended to describe the operation of the HD-15531.

APP NOTE

FOR YOUR INFORMATION

No. 108

Harris Microprocessor

HD-6406 SOFTWARE APPLICATIONS

By J. A. Goss

PAGE

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

HD-6406 CMOS PROGRAMMABLE ASYNCHRONOUS COMMUNICATION INTERFACE

Introduction

The HD-6406 CMOS Programmable Asynchronous Communication Interface (PACI) can be utilized for serial communications at data rates from DC to 1M baud using clock speeds in the range of 0-16MHz. In addition, the device provides an internal baud rate generator, and a complete set of handshaking signals to provide a Data Communications Equipment (DCE) interface.

In the following discussion, we will look at the functional capabilities of the HD-6406 PACI, and give information and examples on how the device can be programmed. The following topics will be discussed:

(1) Glossary of Communications Terms
(2) Control Registers
(3) Status Registers
(4) Transmit/Receive Buffer Registers
(5) I/O Addressing Methods
(6) Reset of the HD-6406 PACI
(7) Programming the HD-6406 PACI

1.0 Glossary of Data Communication Terms

1.1 Clear to Send ($\overline{CTS}$):

Clear-to-send in an input signal to the HD-6406 PACI. It is provided by the device with which the HD-6406 is communicating, such as a modem. When this signal is in its active state (active low), the HD-6406 is being told that the modem will accept data sent to it from its Serial Data Out (SDO) pin.

The $\overline{CTS}$ signal is specified in the RS-232C protocol and is used in conjunction with the Request to Send ($\overline{RTS}$) signal. This signal is used mainly in half-duplex systems. In a half-duplex system communications can be performed in both directions, but in only one direction at a time.

To illustrate this: Suppose we are using the HD-6406 to communicate over an RS-232C link to a modem. In half-duplex operation the UART tells the modem that it wishes to transmit a character by putting $\overline{RTS}$ into its active state (active low for the HD-6406). The modem, if ready for the data, will respond by driving the HD-6406's $\overline{CTS}$ line to its active state (low). When the HD-6406 recognizes this, it will then begin data transmission.

1.2 Data Set Ready ($\overline{DSR}$):

This is also an input signal to the HD-6406 PACI. When in its active state, it signifies that the device with which it is to communicate is powered on and ready for communications. When using a modem, an active state for this signal indicates that the modem is also connected to a communications line (is on line).

1.3 Data Terminal Ready (DTR):

This is an output signal generated by the HD-6406 PACI. its purpose is to inform the target (i.e. modem) that it is ready for communications.

1.4 Framing Error:

Each time the HD-6406 receives a character of data, it will check for 3 types of errors: (1) Parity error, (2) Framing error, and (3) Overrun error.

When reading characters through the Serial Data In (SDI) pin, the HD-6406 will first encounter a start bit. This start bit is a logical zero, and is detected by the first falling edge of the signal on SDI. Next, the HD-6406 will see a specified number of data bits followed by the parity bit. The parity bit is checked for a parity error (see 1.8 and 1.9). The stop bits are then checked for a framing error.

A framing error occurs when an incorrect stop bit is found, or if there are too few stop bits. This happens most often when the baud rates between the communicating devices differ. The data will have a tendency to become skewed. For information on this skewing problem, see 1.10.

1.5 Interrupt Driven I/O:

This is a method of handling interaction between a CPU and an I/O device. In this scheme, the I/O device will issue an interrupt to the CPU when it requires attention.

With the HD-6406, an interrupt might occur when (1) the device receives a character on its SDI pin, (2) the device completes transmission of a character, (3) an error is found in a received character, or (4) a change was detected in one of the modem control lines.

After the interrupt is recognized by the CPU, it (the CPU) will go to the corresponding Interrupt Service Routine (ISR). This routine decides how the interrupt should be serviced, and then services it. Upon completion of the ISR, execution of the user's software will resume at the point where the interrupt occured.

1.6 I/O Polling:

A second method for handling interaction between a CPU and an I/O device. Rather than waiting for an I/O device to interrupt the CPU, the software assumes the responsibility of checking to see if an I/O device needs servicing.

When the system software needs to output to the HD-6406, it will poll (look at) the device to see if it is ready to accept data. Similarly, in order to receive data from the HD-6406, the software will poll to see if there is any data waiting to be read in. Once read, the software must test the status of the HD-6406 to see if any errors were detected in the data received. The software must also look for status changes in the modem control lines.

1.7 Overrun Error:

With the HD-6406, data is received on the SDI pin. From there it is shifted serially into the Receiver Register. Once in this register, it will be shifted (in parallel) into the Receive Buffer Register (RBR) should this register be empty. Should it not be empty, the data cannot be shifted into the RBR. However, subsequent data coming in on the SDI pin will be shifted into the Receiver Register, overwriting the data already there. This causes the HD-6406 to flag an overrun error.

To clear the RBR, data must be read from it by the CPU. This data must be read faster than the data is being received on SDI and written to the Receiver Register. In most cases, this problem must be dealt with in software: (1) Either the receive data routine must be optimized for better performance, or (2) The baud rate must be lowered to compensate for the data loss.

1.8 Parity:

Parity is a form of error detection commonly used in serial communications. In parity checking, the sending device generates and sends an extra bit with each character transmitted. The state of this bit (0 or 1) is determined by (1) the number of 1 bits in the character transmitted, and (2) by whether parity was defined to be even or odd.

With even parity, the parity bit is generated such that the number of 'one' bits in the character (including the parity bit) is an even number. For example, if a word has 5 bits that are ones, the parity bit must be set to a one so that the total number of 'one' bits is an even number. If a character being sent has 6 bits set to a one, the parity bit will be zero. This still gives an even number of one bits in the character:

Conversely, in odd parity, the parity bit is generated such that the total number of 1 bits (including the parity bit) is an odd number. For a character having 5 one bits, the parity bit generated is a zero. For a character having 6 one bits, the parity bit is set to one.

Character Sent	(EVEN) Parity bit	(ODD) Parity bit
01101110	1	0
11111010	0	1

FIGURE 1. PARITY

1.9 Parity Error:

This is caused by an invalid parity bit being detected in a character received. The condition occurs when (A) even parity is specified and an odd number of 'one' bits are detected in the character, or (B) odd parity is specified and an even number of 'one' bits are detected.

For example, if the character 6EH (01101110 b) is received by the device, and the parity bit read in is a 1, a parity error would be flagged if parity was defined to be ODD. Should parity be set to EVEN and the parity bit is a 1 for this same character, a parity error will not be flagged.

1.10 Percentage Error in Baud Rate Generation:

When exchanging data between two systems through serial links (i.e. RS-232C) it is important that the baud rates of the two systems be as equal as possible. Roughly speaking, these baud rates should not differ by more than 2%. For example, if system X is using an HD-6406 to generate 1200 bits per second (bps), and system Y with which it is communicating is generating 1244 bps, there is a 3.67% difference in the baud rates. Errors may occur when data is received by system X.

The HD-6406 samples the data being received on the SDI pin beginning from when the receiver detects a start bit. This is denoted by a high-to-low transition on the SDI pin. Based on the specified baud rate, the HD-6406 will count and sample such that each bit is read at the center of a bit period. Figure 2B shows a character generated at 1200 bps, and sampled for 10 bit periods (S0 - S10). The character is 1B Hex with even parity.

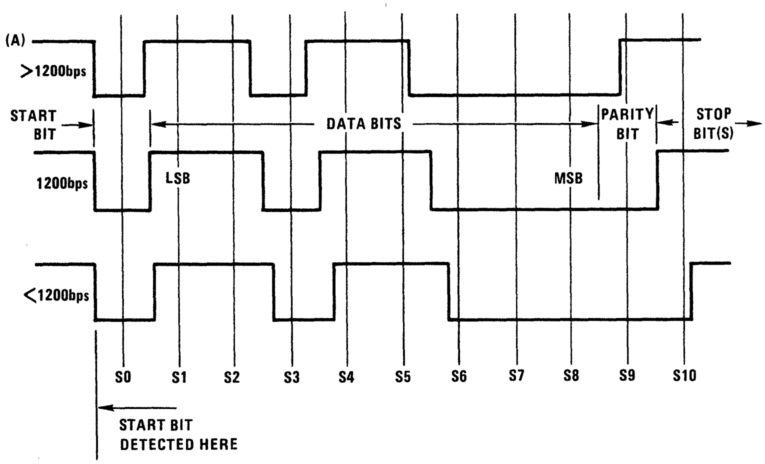


FIGURE 2. PERCENTAGE ERROR

Assume that system X is configured to transmit and receive at 1200 bps. The system we are communicating with is running slightly faster as stated above (1244 bps). Our sampling rate will still be based upon 1200 bps, but the sampling of the incoming signal will be off by a short time period. With each sample this error accumulates. Thus, the skewing to the right becomes greater over time. By the time we normally would be sampling the parity bit (S9), the stop bit(s) would be coming in over the SDI pin (see Figure 2A). In this case, the HD-6406 thinks it is sampling the parity bit when in fact, what it is seeing is really the stop bit. This could cause a parity error to be flagged.

Conversely, if data is being received at a baud rate slightly less than our specified baud rate, we would get a skewing of the received data in the opposite direction. From Figure 2C, we see that at S10 we are checking the stop bit, but system Y is still transmitting the parity bit. Therefore, the Framing error will be flagged.

1.11 Receive Line Signal Detect ($\overline{\text{RLSD}}$):

Also known as CARRIER DETECT, this signal would be sent from a modem. It indicates that the modem has an established communications link with a remote system (i.e. via telephone). Any data transmitted from the modem to the HD-6406 is valid only if the the $\overline{\text{RLSD}}$ line is in its active state (active low). Otherwise, the data from the modem should be ignored.

1.12 Request To Send ($\overline{\text{RTS}}$):

This signal is an output of the HD-6406. It is used to inform a modem or remote system that it wishes to transmit data. The modem (remote system) would then respond by activating the $\overline{\text{CTS}}$ signal. As with the $\overline{\text{CTS}}$, this signal is of most value in half-duplex communications.

1.13 Ring Indicator ($\overline{\text{RI}}$):

This signal is an input to the HD-6406. It is generated by a modem and is used to inform the HD-6406 that the modem is receiving a ringing signal. In response, an interrupt could be generated by the HD-6406 to the CPU. This would force the CPU to initiate a connection to the caller. When this connection is made, the $\overline{\text{RLSD}}$ line should become active (low).

2.0 Control Registers

In order for the HD-6406 to properly operate in a system, it must be configured for the desired form of operation. The user must decide how the device will be used in the system, and know the communications protocol of the device it will be communicating with. For example, in a system communicating with a modem we would need to utilize the modem control lines. When using the HD-6406 in a local area network these modem control lines may be of no use to us.

The HD-6406 is initialized and configured by writing a series of control words from the CPU to various control registers in the device. These registers include the UART Control Register (UCR), the Baud Rate Selector Register (BRSR), and the Modem Control Register (MCR).

UCR: Defines the format of characters being transmitted. The format of the characters includes the number of data bits, parity control, and the number of stop bits.

BRSR: Used in setting up the internal baud rate generator in the HD-6406 for a specific baud rate. It will also be used to specify what the CO output is to be.

MCR: Defines which interrupts will be enabled, and will also set the modem control output lines ($\overline{\text{RTS}}$ and $\overline{\text{DTR}}$). In addition, the MCR allows the user to select one of four modes of communications (normal mode, echo mode, transmit break, and loop test mode).

2.1 UART Control Register

The UART Control Register (UCR) is a write-only register. Writing a command word to the UCR configures the transmission and reception circuitry of the HD-6406. The command word essentially describes the format of characters that are to be transmitted or received. The format of these characters are made up of (1) a specific word length, (2) parity information, and (3) a selected number of stop bits, used to indicate transmission of that character is completed.

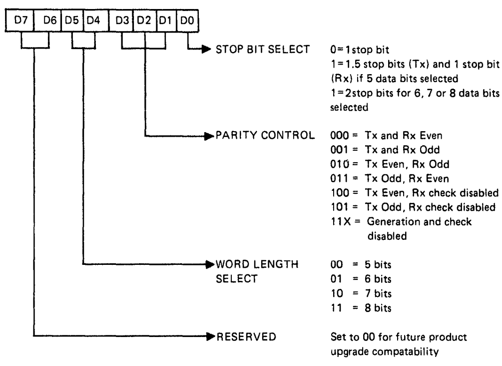


FIGURE 3. UCR FORMAT

UCR

D7 | D6 D5 | D4 D3 | D2 D1 | D0

D0	STOP BIT SELECT	0=1stop bit 1=1.5 stop bits (Tx) and 1 stop bit (Rx) if 5 data bits selected 1=2stop bits for 6, 7 or 8 data bits selected
D3 D2 D1	PARITY CONTROL	000 = Tx and Rx Even 001 = Tx and Rx Odd 010 = Tx Even, Rx Odd 011 = Tx Odd, Rx Even 100 = Tx Even, Rx check disabled 101 = Tx Odd, Rx check disabled 11X = Generation and check disabled
D5 D4	WORD LENGTH SELECT	00 = 5 bits 01 = 6 bits 10 = 7 bits 11 = 8 bits
D7 D6	RESERVED	Set to 00 for future product upgrade compatability

USR

D7 D6 D5 D4 D3 D2 D1 D0

D0	PARITY ERROR (PE)	0 = No Error 1 = Error
D1	FRAMING ERROR (FE)	0 = No error 1 = Error
D2	OVERRUN ERROR (OE)	0 = No error 1 = Error
D3	RECEIVED BREAK (RBRK)	0 = No break 1 = Break
D4	MODEM STATUS (MS)	0 = No status change 1 = Status change
D5	TRANSMISSION COMPLETE (TC)	0 = Not complete 1 = Complete
D6	TRANSMITTER BUFFER REGISTER EMPTY (TBRE)	0 = Not empty 1 = Empty
D7	DATA READY (DR)	0 = Not ready 1 = Ready

MSR

D7 D6 D5 D4 D3 D2 D1 D0

D0	CLEAR TO SEND (CTS)	0 = false 1 = true
D1	DATA SET READY (DSR)	0 = false 1 = true
D2	RECEIVED LINE SIGNAL DETECT (RLSD)	0 = false 1 = true
D3	RING INDICATOR (RI)	0 = false 1 = true
D7 D6 D5 D4	UNDEFINED	

BRSR

D7 D6 D5 D4 D3 D2 D1 D0

D1 D0	PRESCALER SELECT	00 = ÷ 1 01 = ÷ 3 10 = ÷ 4 11 = ÷ 5
D6 D5 D4 D3 D2	DIVISOR SELECT	00000 = ÷ 2 00001 = ÷ 4 00010 = ÷ 16/3 00011 = ÷ 8 00100 = ÷ 32/3 00101 = ÷ 16 00110 = ÷ 58/3 00111 = ÷ 22 01000 = ÷ 32 01001 = ÷ 64 01010 = ÷ 128 01011 = ÷ 192 01100 = ÷ 256 01101 = ÷ 288 01110 = ÷ 352 01111 = ÷ 512 10000 = ÷ 768 11111 = ÷ external (÷ 1)
D7	CO SELECT	0 = Ix output 1 = BRG output

RBR

D7 D6 D5 D4 D3 D2 D1 D0

D0	Bit 0
D1	Bit 1
D2	Bit 2
D3	Bit 3
D4	Bit 4
D5	Bit 5
D6	Bit 6
D7	Bit 7

5 bit word: Bit 0 – Bit 4; 6 bit word: Bit 0 – Bit 5; 7 bit word: Bit 0 – Bit 6; 8 bit word: Bit 0 – Bit 7

Note: The LSB, Bit 0 is the first serial data bit received.

MCR

D7 D6 D5 D4 D3 D2 D1 D0

D0	REQUEST TO SEND ($\overline{RTS}$)	0 = $\overline{RTS}$ output high 1 = $\overline{RTS}$ output low
D1	DATA TERMINAL READY ($\overline{DTR}$)	0 = $\overline{DTR}$ output high 1 = $\overline{DTR}$ output low
D2	INTERRUPT ENABLE (INTEN)	0 = Interrupts enabled 1 = Interrupts disabled
D4 D3	MODE SELECT	00 = Normal 01 = Transmit break 10 = Echo mode 11 = Loop test mode
D5	RECEIVER ENABLE (REN)	0 = Not enabled 1 = Enabled
D6	MODEM INTERRUPT ENABLE (MIEN)	0 = Not enabled 1 = Enabled
D7	Must be set to a logic 0 for normal PACI operation	

TBR

D7 D6 D5 D4 D3 D2 D1 D0

D0	Bit 0
D1	Bit 1
D2	Bit 2
D3	Bit 3
D4	Bit 4
D5	Bit 5
D6	Bit 6
D7	Bit 7

5 bit word: Bit 0 – Bit 4; 6 bit word: Bit 0 – Bit 5; 7 bit word: Bit 0 – Bit 6; 8 bit word: Bit 0 – Bit 7

Note: The LSB, Bit 0 is the first serial data bit transmitted.

D0 — Stop Bit Select: This bit is used to select the number of stop bits that the HD-6406 will insert into a character to be transmitted, and the number to look for in received characters. The stop bit(s) denote where the end of a character occurs. The external device must be configured with the same number of stop bits as the HD-6406. The setting(s) for this bit are as follows:

0 — If this bit is set to zero, then a single stop bit will be generated and checked for.

1 — Setting this bit to a one will cause either of two configurations. If we select a character length of 5 data bits, the HD-6406 will generate 1.5 stop bits during transmission, and will look for a single stop bit when receiving data. If a character length of 6, 7, or 8 data bits is selected, then two (2) stop bits will be generated and checked for.

D3, D2 and D1 — Parity Control: These three bits are used to control the generation and checking of the parity bit. The HD-6406 can be configured to perform this function one of seven ways. These are:

000 - Even parity is generated for transmitting data, and will be checked for when receiving data.

001 - Odd parity is generated for transmitting data, and checked for during data reception.

010 - Even parity is generated for data transmission, and odd parity will be checked for during data reception.

011 - Odd parity is generated for data transmission, and even parity will be checked for during data reception.

100 - Even parity is generated for data transmission, however, the HD-6406 will do no parity checking on data that has been received.

101 - Odd parity is generated for data transmission. The HD-6406 will not check parity on data received.

11X - The generation of a parity bit is disabled. Also, the HD-6406 will not check for parity on incoming data. D1 is not used therefore, it can be either a 0 or a 1.

TABLE 1. PARITY SELECTION

	Transmitter	Receiver
000	Even	Even
001	Odd	Odd
010	Even	Odd
011	Odd	Even
100	Even	Disabled
101	Odd	Disabled
11X	Disabled	Disabled

D5, D4 — Word Length Select: The state of these bits determines the number of bits that are transmitted as a data word. The word length can be 5, 6, 7, or 8 bits long.

TABLE 2. WORD LENGTH SELECTION

D5	D4	Word Length
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

D7, D6 — Reserved: These bits have been reserved for future product upgrade compatibility. To insure that the future upgrades of the HD-6406 will operate with existing software, these bits must both be set to zero (00).

2.2 Baud Rate Select Register

The Baud Rate Select Register (BRSR) is a write-only register used to set the internal HD-6406 baud rate generator to the desired data transfer rate. Essentially, this baud rate will depend upon the clock speed of the crystal being used with the device. However, to provide more flexibility, the HD-6406 provides two seperate counters for selecting a divide ratio to fit the user's needs.

These two counters are the Prescaler, and the Divisor select. The Prescaler allows the input clock rate to be divided by one of four values; 1, 3, 4, and 5. This new data rate can then be further divided by using the values available with the Divisor select. This final clock speed will be 16 times the actual baud rate used by the HD-6406.

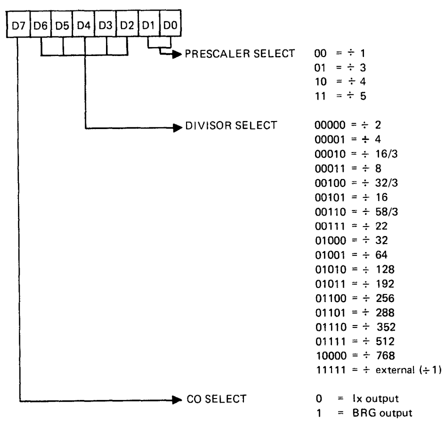


FIGURE 4. BRSR FORMAT

The 16X clock speed can be output to the CO pin of the device through the CO Select function of the BRSR. If CO select is not selected, the output of the CO pin will reflect the crystal frequency input by the part on the IX pin. Note, this output (CO) is a buffered version of the IX input or 16X baud rate.

D1 and D0 — Prescaler Select: This allows the user to choose one of four values that the input clock frequency (IX) will be divided by.

TABLE 3. PRESCALER SELECTION

D1	D0	PRESCALER DIVISOR
0	0	÷1
0	1	÷3
1	0	÷4
1	1	÷5

D6, D5, D4, D3, and D2 — Divisor Select: The state of these bits determines the value of the Divisor select. The possible values are as follows:

TABLE 4. DIVISOR SELECTION

D6-D2	DIVISOR
00000	÷2
00001	÷4
00010	÷16/3
00011	÷8
00100	÷32/3
00101	÷16
00110	÷58/3
00111	÷22
01000	÷32
01001	÷64
01010	÷128
01011	÷192
01100	÷256
01101	÷288
01110	÷352
01111	÷512
10000	÷768
11111	÷1

By using a crystal or external frequency with one of the common crystal frequencies (1.8432 MHz, 2.4576 MHz, or 3.072MHz) and a prescaler of divide by 3, 4, or 5 respectively, standard baud rates can easily be generated by selecting the Divisor as shown in Table 5 below:

TABLE 5. STANDARD DIVISORS

BAUD RATE	DIVISOR
38.4K	External
19.2K	2
9600	4
7200	16/3
4800	8
3600	32/3
2400	16
2000*	58/3
1800*	21
1200	32
600	64
300	128
200	192
150	256
134.5*	288
110*	352
75	512
50	768

NOTE: All baud rates are exact except for:

TABLE 6. PERCENT DIFFERENTIAL

BAUD RATE	ACTUAL	% DIFFERENCE
2000	1968.2	0.69%
1800	1828.6	1.56%
134.5	133.33	0.87%
110	109.71	0.26%

To illustrate how a baud rate can be determined, let us look at the following example:

EXAMPLE 2.1:

Assume that we are using a clock frequency of 2.4576 MHz with the HD-6406, and we wish to configure the device to run at a baud rate of 9600 bits per second (bps).

First, select a prescaler of divide-by-four. Therefore, bits D1 and D0 will be set to 1 and 0. This will give an effective clock frequency of 614,400 Hz.

Next, look at Table 5 to determine which divisor is needed to generate 9600 bps. The divisor is four (4). Bits 6 through 2 will be set to 0 0 0 0 and 1. The 614,400 Hz clock has then been divided by 4 to give the appropriate 16X clock, which is 153,600 HZ (16 x 9600).

To determine what the actual baud rate is, take 153,600 Hz and divide it by 16. This will give us our 9600 bits per second (bps). A 16X clock rate is required by the internal circuitry of the HD-6406. That is why the prescalar and divisor are selected to yield a clock rate that is 16 times the desired baud rate.

Finally, set the CO Select bit to 1 so that the CO output will be the same as the BRG output. This is the 16X frequency calculated above (153,600 Hz).

The command word written to the BRSR will be:

10000110 or 86 Hex

D7 — CO Select: This tells the HD-6406 what the source will be for the output pin CO.

0 - The output on CO will be a buffered version of the clock input (IX) to the device. The frequency of this signal will be the actual crystal frequency (or external frequency) used to run the HD-6406.

1 - The output of CO will be a buffered version of a clock rate that is 16 times the actual baud rate generated by the HD-6406. This signal is suitable for driving a second HD-6406 or UART in a system.

2.3 Modem Control Register

The Modem Control Register (MCR) is a general purpose register controlling various operation parameters within the device. These parameters include: (1) setting modem control lines $\overline{RTS}$ and $\overline{CTS}$, (2) Enabling the interrupt structure of the device, (3) enabling the receiver on the device, and (4) selecting one of four operating modes in the device.

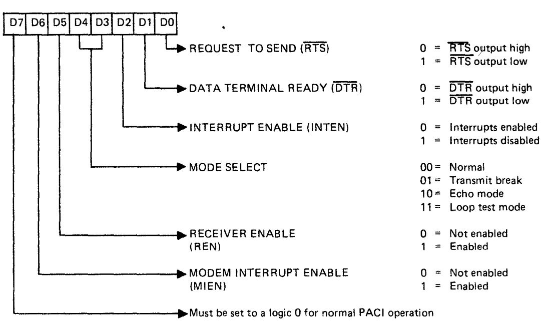


FIGURE 5. MCR FORMAT

D0 — Request to Send: This bit allows the user to set the state of the $\overline{RTS}$ output pin. This pin is used as a modem control line in the RS-232C interface protocol. It is important to remember that the $\overline{RTS}$ output pin is active low.

0 - Setting this bit to a zero causes a one (1) to be output on the $\overline{RTS}$ pin. In effect, this is setting the pin to its logical false state.

1 - If this bit is set to a one, the $\overline{RTS}$ pin will be forced to a zero (0). This puts the $\overline{RTS}$ signal in its logical true state.

D1 — Data Terminal Ready: This is a modem control line for an RS-232C-like interface. It is an output pin and is also active low.

0 - A zero in bit D1 causes $\overline{DTR}$ pin to be put in a logical false state. The $\overline{DTR}$ pin outputs a one (1).

1 - By writing a one to this bit, the HD-6406 $\overline{DTR}$ output pin is set to its logical true state (zero).

D2 — Interrupt Enable (INTEN): This bit is an overall control for the INTR pin on the HD-6406. With it, all HD-6406 interrupts to the processor can either be enabled or disabled. When D2 is reset to disable interrupts, no status changes including modem status changes can cause an interrupt to the processor.

0 - Interrupts are disabled. The INTR pin will be held in a false state (low) so that no interrupt requests to the processor are generated.

1 - Interrupts are enabled. Interrupts will be discussed in more detail later.

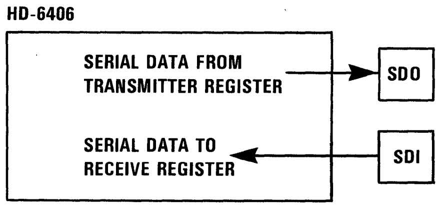
D4 and D3 — Mode Select: These two bits allow the user to select one of the four possible operating modes for the HD-6406. These are:

00 - Normal mode - The HD-6406 is configured for normal full or half duplex communications. Data will not be looped back in any form or fashion between the serial data input pin and the serial data output pin (see Figure 6a).

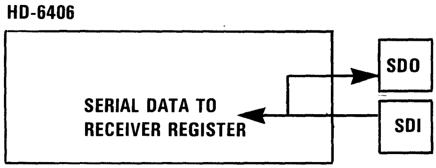
01 - Transmit break - Selecting this mode of operation will cause the transmitter to transmit break characters only. A break character is composed of all logical zeros for the start, data, parity, and stop bits.

10 - Echo mode - When this is selected, the HD-6406 will re-transmit data received on the SDI pin out to the SDO pin. In this mode of operation, any data written to the Transmitter Buffer Register will not be sent out on the SDO pin (see Figure 6b).

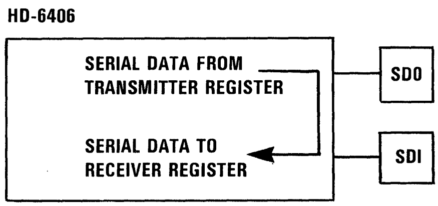
11 - Loop Test mode - If this mode is selected, the data that normally would be transmitted is internally routed back to the receiver circuitry. The transmitted data will not appear at the SDO pin. Also, data that is received on the SDI pin will be ignored by the device. This mode of operation is useful for performing self test(s) on the device (see Figure 6c).



6a. NORMAL MODE



6b. ECHO MODE



6c. LOOP TEST MODE

FIGURE 6. OPERATING MODES

D5 — Receiver Enable (REN): Controls the reception of data through the SDI pin into the Receiver Register. Disabling the receiver is useful when performing a software reset on the device. This locks out any errant data from being received. This would also prevent interrupts from occuring due to data reception. Other possible reasons for disabling the receiver might be so that sections of software can execute without interruption, so that software only accepts data when ready for it, or so that a software reset/reconfiguration can be performed.

0 - A zero for this bit prevents the device from recognizing data sent to the SDI pin. The receive circuitry will remain in an idle state.

1 - Writing a one to this bit enables the receiver. Data will then be recognized at the SDI pin.

D6 — Modem Interrupt Enable: Enabling this bit will allow any change in the modem status line inputs ($\overline{\text{CTS}}$, $\overline{\text{RI}}$, $\overline{\text{RLSD}}$, $\overline{\text{DSR}}$) to cause an interrupt. The Modem Status register (MSR) will contain information pertaining to which condition(s) caused the interrupt.

0 - Modem interrupts not enabled.

1 - Modem interrupts enabled.

D7 — This bit must always be set to a logic zero to insure device compatibility for future product upgrades. Should this bit be set to a one (1) during initialization, the device will not respond to any data at the SDI pin, and no data will be transmitted from the Transmitter Register to the SDO pin.

3.0 Status Registers

In addition to the various Control registers, the HD-6406 has two read only status registers that can be accessed by the CPU to determine the status of the device at any given time. These are the UART Status Register (USR), and the Modem Status Register (MSR). The registers are used for keeping track of any changes in (1) the modem lines on the device (2) the status of data transmission or reception, and (3) whether any error(s) were detected in received data.

The USR deals with the different types of data errors, the status of data transmission, as well as data waiting to be read. The MSR, on the otherhand, reflects the status of the various modem control lines in the device (i.e. $\overline{\text{CTS}}$, $\overline{\text{DSR}}$, $\overline{\text{RLSD}}$ and $\overline{\text{RI}}$).

Normally, in an interrupt-driven system, after an interrupt occurs, the user's software would check the status register(s) to determine what caused the interrupt. The software then should deal with the various types of interrupts in an appropriate manner.

3.1 UART Status Register

The UART Status Register (USR) contains information pertaining to the status of the HD-6406 operation. The information that is kept in the USR includes: data reception error information, modem status, and the status of data transmission. This register will normally be the first HD-6406 register read when servicing an HD-6406 interrupt, or when polling the device.

NOTE: the USR will be cleared upon reading its contents. We will later deal with this situation from a software standpoint.

After reading and clearing the status register, the bits will remain as zeros until a status change occurs to set the proper bit(s).

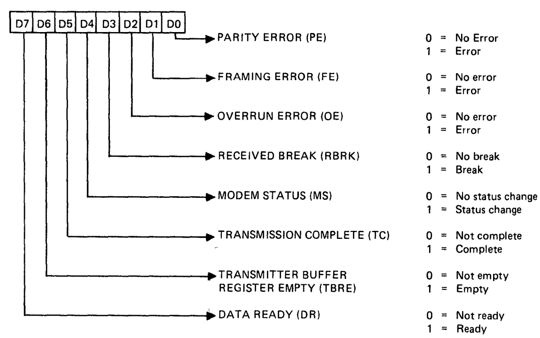


FIGURE 7. USR FORMAT

D0 — Parity error (PE): This bit indicates whether a parity error was detected in the last character read into the Receive Buffer Register. If parity is disabled, this bit will always be a zero.

0 - No error detected.

1 - Parity error detected.

D1 — Framing error (FE): A one in this bit indicates that the last character received contained an improper number of stop bits. This might be caused by no stop bits being sent, or by the length of the stop bits being too short.

0 - No framing error.

1 - Framing error detected.

D2 — Overrun error (OE): When this status bit is set to a one, it indicates that data in the RBR is not being read by the CPU fast enough to permit data in the Receiver Buffer to be shifted to the RBR before the next character comes in on the SDI pin. Data is then lost because it is overwritten by incoming characters.

0 - No overrun error detected.

1 - Overrun error detected.

D3 — Received Break (RBRK): This status bit indicates that the last character received was a break character. A break character consists of all logic zeros including the parity and stop bits. The most common usage of this character is to indicate a special condition in the communications taking place. For example, the device sending information to the HD-6406 might send a break character to it to indicate that it has completed transmitting its stream of data.

0 - No break.

1 - Break detected.

D4 — Modem Status (MS): This bit indicates whether or not there has been a change in the states of any of the modem control lines on the device. These lines include: $\overline{RI}$, $\overline{RLSD}$, $\overline{CTS}$ and $\overline{DSR}$. To determine which of these lines has changed, the user can read the Modem Status Register (MSR).

Also, should both the MIEN and INTEN bits be set in the MCR register, an interrupt will be generated when the MS bit gets set.

0 - No status change.

1 - Status change detected.

D5 — Transmission Complete (TC): When a character is written to the HD-6406 Transmitter Buffer Register (TBR), it will be transferred to the Transmitter Register before actually being shifted out serially through the SDO pin. When the character has finally been transmitted on SDO, and both the TBR and Transmitter Registers are empty, the TC bit will be set.

NOTE: The TC bit getting set does not always mean that an end of transmission has occured. It indicates that both the TBR and the Transmitter Register are empty. For instance, if we are running the HD-6406 at a high baud rate, it could transmit data faster than the user's software can write characters to the device. In this case, the TC bit could get set between each character being transmitted.

Assertion of this bit will cause an interrupt when the INTEN bit of the MCR has been set, and when the Status Flags Disable (SFD) pin (32) is held low.

0 - Not complete.

1 - Transmission complete.

D6 — Transmitter Buffer Register Empty (TBRE): When a character written to the TBR has been transferred to the Transmitter Register and the TBR is ready for another character, this bit will get set.

The user should check the TBRE bit before writing another character to the Transmitter Buffer Register. This insures that the previous character written to the TBR no longer resides there, but is being shifted out on the SDO pin.

An interrupt is generated by a change in this status, should the INTEN bit of the MCR be set, and should the SIE (pin 31) input to the device be high.

0 - Not empty.

1 - Empty.

D7 — Data Ready (DR): Is set when the Receive Buffer Register (RBR) has been loaded with a received character through the SDI pin. The CPU can access this data by reading the RBR. For example, if the user wishes to see if there is any data waiting to be read from the Receiver Register, this bit can be checked.

An interrupt signaling this condition is caused if the INTEN bit of the MCR is enabled, and if the SIE input (pin 31) is high.

0 - No data ready.

1 - Data ready in RBR.

NOTE: In an interrupt driven system, interrupts caused by the DR signal should have a higher priority than those caused by the TBRE signal. This will guard the software against Overrun errors. You have no control over the information being sent to you, but you can control how and when you are transmitting data.

3.2 Modem Status Register

The Modem Status Register (MSR), a read-only register, allows the user to determine the status of the Modem Status pins. The status of these pins is reflected by the corresponding bit(s) being set to a one if the state of the pin is in its true state (low), and by being set to a zero if the pin is in its false state (high). This will apply regardless of whether the pin is set up to be active high or active low.

A change in any of the status bits will cause an interrupt if the INTEN and MIEN bits of the MCR are enabled.

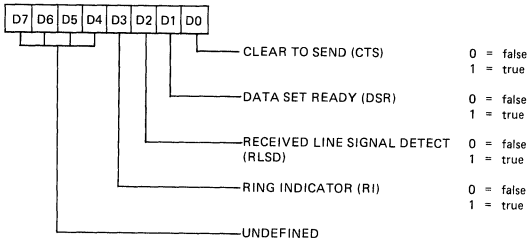


FIGURE 8. MSR FORMAT

D0 — Clear to Send (CTS): This is both a status and control signal from the modem. It tells the HD-6406 that the modem is ready to receive data from the HD-6406 transmitter output (SDO). If this line is inhibited (false), then the HD-6406 will not be able to begin transmission of data. Should this line go false in the middle of a transmission, the UART will only be able to finish transmission of the current character.

0 - CTS in false state.

1 - CTS is true.

D1 — Data Set Ready (DSR): This is a status indicator from the modem to the HD-6406 indicating that the modem is ready to provide data to the HD-6406.

0 - DSR in false state.

1 - DSR is true.

D2 — Received Line Signal Detect (RLSD): This input is provided from the modem, and indicates that the signal quality received from the HD-6406 is within acceptable limits.

0 - Unacceptable signal quality.

1 - Signal quality acceptable.

D3 — Ring Indicator (RI): The RI input informs the HD-6406 that the modem is receiving a ringing signal. This is useful for implementing automatic answering in communications systems.

0 - No ringing detected.

1 - Ringing detected.

4.0 Transmit/Receive Buffer Registers

In addition to the control and status registers, the HD-6406 PACI has two buffer registers that allow for the actual serial communications to be performed. These registers are used for sending characters out to the SDO pin, and for reading data from the SDI pin.

4.1 Receiver Buffer Register

The Receiver Buffer Register (RBR) is a read-only register which contains the character received via the SDI pin. When data is received by the HD-6406, it is read serially into the Receiver Register from the SDI pin, and then transferred to the RBR for the CPU's access. This double buffering allows for higher transmission rates without loss of data. However, should additional characters be received by the HD-6406 before this register is read, then the Receiver Register will be overwritten with the subsequent characters. This will cause the Overrun Error (OE) flag to be asserted.

The RBR is 8 bits long and can accept data lengths of 5 to 8 bits. The data will be right justified in the register. When selecting data lengths of less than 8 bits, the HD-6406 will insert zeros (0) into the RBR for the unused (most significant) bits. For example, if the HD-6406 is configured for 6 data bits, and the character 31H is received, the RBR will look as follows when read:

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	0	0	0	1

FIGURE 9. RECEIVED DATA

Bits D7 and D6 are automatically zeroed out by the HD-6406.

4.2 Transmitter Buffer Register

The Transmitter Buffer Register (TBR) is a write only register used for sending characters out through the SDO pin. Characters to be transmitted should only be written to this register when it is empty. This condition can be checked for by reading the UART Status Register (USR) TBRE bit, or waiting for an interrupt to signal this condition.

Like the Receiver circuitry, the Transmitter also uses double buffering. Here, we are taking advantadge of the double buffering to increase throughput with the HD-6406. The user would first write a character to the TBR. From here it is shifted (in parallel) into a second register known as the Transmit Buffer. After this transfer has been completed, the TBRE bit is set, and an interrupt generated if they have been enabled.

The character shifted into the Transmit Buffer is then shifted serially out onto the SDO pin. Meanwhile, because the TBR is empty, another character can be written by the CPU to the TBR. In effect, the transmitter circuitry is then performing two operations simultaneously. This double buffering technique allows continuous data flow transmission.

The Transmit Buffer Register is also 8 bits wide. Because we can specify data lengths as being from 5 to 8 bits wide, the HD-6406 right justifies the data when it is written to the TBR, and fills the unused bits with zero's. In other words, unused (most significant) bits are truncated. For example, if we set up the device so that 6 data bits are specified and we write the character 71H (01110001 b) to the TBR, we will effectively be transmitting the character:

D7	D6	D5	D4	D3	D2	D1	D0	
0	0	1	1	0	0	0	1	= 31H

FIGURE 10. TRANSMITTED DATA

The two most significant bits are zeroed out automatically by the HD-6406.

5.0 I/O Addressing Methods

To utilize the HD-6406 in a microprocessor based system, it is necessary for the system to be designed such that we can easily access (address) the device. In the following discussion, we will look at two I/O device addressing schemes that can be applied to the HD-6406:

- I/O Mapped Addressing, and

- Memory Mapped I/O Addressing

We will look at these two modes as they apply to an 80C86/80C88-based system.

5.1 I/O Mapped Addressing:

In this scheme of I/O addressing, the microprocessor uses one set of instructions for accessing memory, and a different set for accessing I/O devices. The CPU will generate different control signals ($\overline{IO}$/M) to select either memory or I/O based upon the type of instruction it is executing. Because of this, the system needs two sets of control logic for accessing memory and I/O. As we can see in Figure 11, the control logic for each is essentially the same.

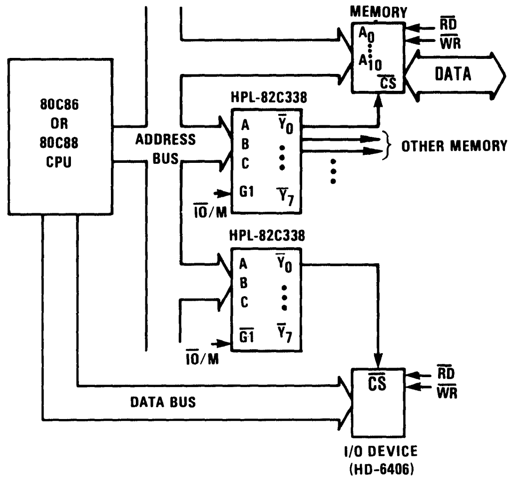


FIGURE 11. I/O MAPPED ADDRESSING

When addressing I/O, we would use either the IN instruction or the OUT instruction. The port address specified in the instruction is placed on the address bus, and the $\overline{IO}$/M signal selects and activates the control logic for I/O. If we used one of the memory commands (MOV, CMP, TEST, etc.), the $\overline{IO}$/M signal would activate the control logic for the system memory.

5.2 Memory Mapped I/O:

Memory Mapped I/O uses the same control logic for accessing both memory and I/O devices within a system. This is illustrated in Figure 12. Because we are using one set of control logic, we reduce the number of devices in the system, and save board space.

When I/O devices are placed within the Memory Space of a system, it is possible to take advantage of the memory instruction set. This would now allow us to utilize the full register set in I/O operations, as opposed to only being able to use the accumulator (AX/AL) for the I/O instructions. Also, conditional testing can be applied to the I/O devices (i.e. TEST, CMP). When using memory mapped I/O, it should be noted that the I/O devices can no longer be accessed through the I/O instructions (IN and OUT).

There are disadvantages to using memory mapped I/O as well:

- The I/O devices are treated as memory, therefore the amount of available memory in the system is reduced.

- Memory instructions will execute slower than the I/O commands (IN and OUT). In certain situations (i.e. I/O polling), this could lead to loss of data during communications (overrun errors).

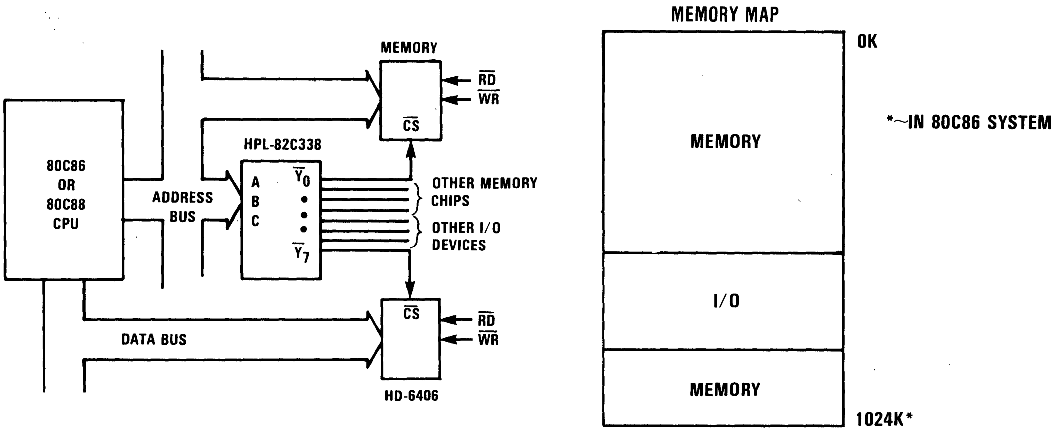


FIGURE 12. MEMORY MAPPED I/O ADDRESSING

5.3 I/O Addressing For The HD-6406:

The actual addressing of the HD-6406 internal registers takes place through the address pins A0 and A1. These two signals are taken from the address bus. In the following example(s), address lines AD0 and AD1 from the 80C86/88 drive A0 and A1, respectively, on the HD-6406. Control logic will decode the remaining address lines from the CPU to generate a 'chip select' for enabling the HD-6406. The control logic consists of an HPL-82C338 Programmable Chip Select Decoder (PCSD). The Gx lines of the PCSD are fuse programmable, and have been programmed to be active low for this particular application. A diagram of this logic is shown in Figure 13.

The addresses for the HD-6406 set up as described above are shown in Table 7.

TABLE 7. EXAMPLE ADDRESSES

REGISTER	ADDRESS	REGISTER TYPE
Transmit Buffer Register	10H	Write only register
Receiver Buffer Register	10H	Read only register
UART Control Register	11H	Write only register
UART Status Register	11H	Read only register
Modem Control Register	12H	Write/Read register
Baud Rate Selector Register	13H	Write only register
Modem Status Register	13H	Read only register

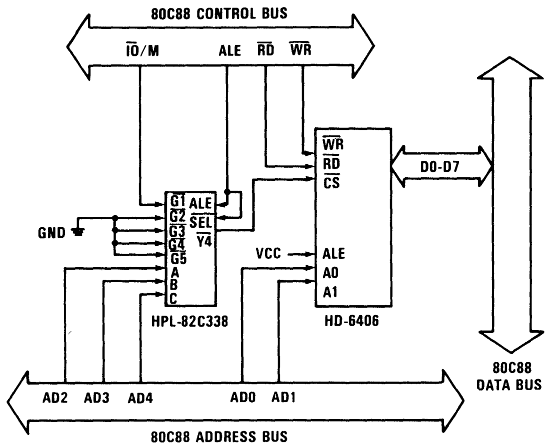


FIGURE 13. EXAMPLE SYSTEM

6.0 Reset Of The HD-6406 PACI

There are two distinct ways in which the HD-6406 can be reset to a known initial state: (1) By applying a reset pulse for at least two clock cycles on the RST pin, or (2) through software.

A hardware reset is accomplished by forcing the RST pin to a high state for a minimum of two clock cycles. This should be for two cycles of the HD-6406's IX clock input as opposed to the system clock. This reset will cause the UART Status Register (USR) to be set to 60H (TC and TBRE bits will be set), and the Modem Control Register (MCR) will be cleared. Any lines associated with the bits in the USR and MCR will be cleared or disabled.

During the reset of the device, the Baud Rate Select Register (BRSR) and the UART Control Register (UCR) will not be affected. However, if the reset comes due to power on, these registers will have an indeterminate value associated with them. After this reset, the HD-6406 will remain in an idle state until programmed to its desired configuration.

A second method of resetting the HD-6406 is through a software reset. This will allow the device to be set to a known state. The procedure for performing a software reset is outlined below:

(1) MCR = 00H. Write a zero to the MCR. This will disable the receiver as well as the modem control lines, and interrupts.

(2) Read the RBR to clear out any residual data.

(3) Read the USR to reset status, thus keeping status lines from causing possible interrupts to the CPU.

(4) Reconfigure the device for the desired mode of operation.

7.0 Programming The HD-6406 PACI

In order to configure the HD-6406 for proper operation, three separate command words need to be written to the command (control) registers that were specified earlier.

These registers include (1) the UART Control Register, (2) the Baud Rate Select Register, and (3) the Modem Control Register. When programming the device, these registers can be written to in any order. It is advisable to initialize the Modem Control Register last because it controls the enabling of interrupts, and the receiver circuitry.

Once initialized, the HD-6406 can be reconfigured at any time by writing new command word(s) to the control registers. However, the device should not be actively transmitting or receiving data when reconfiguring the control registers.

Addressing of the internal registers on the HD-6406 occurs by using the address lines A1 and A0, as well as the $\overline{WR}$ and $\overline{RD}$ lines. A more complete description of this is shown in Table 8.

TABLE 8. ADDRESSING THE HD-6406

ALE	$\overline{CS0}$	CS1	A1	A0	$\overline{WR}$	$\overline{RD}$	OPERATION
1 or ↓	0	1	0	0	↑	1	Data bus → TBR
1 or ↓	0	1	0	0	1	↓	RBR → Data bus
1 or ↓	0	1	0	1	↑	1	Data bus → UCR
1 or ↓	0	1	0	1	1	↓	USR → Data bus
1 or ↓	0	1	1	0	↑	1	Data bus → MCR
1 or ↓	0	1	1	0	1	↓	MCR → Data bus
1 or ↓	0	1	1	1	↑	1	Data bus → BRSR
1 or ↓	0	1	1	1	1	↓	MSR → Data bus

7.1 Device Driver Examples:

The following examples are provided to illustrate how we can program the HD-6406 as described above. The first example shows a system set up for I/O polling of the device. In the second example, we will take advantage of interrupt driven I/O.

It is important to note the following assumptions for these examples:

(1) The HD-6406 is being used as an RS-232C interface in an 80C86 or 80C88 based system.

(2) A 2.4576 MHz clock is being supplied to the HD-6406 PACI.

(3) For the interrupt driven example (example 2), we are utilizing an 82C59A Interrupt Controller to interface with the CPU when an interrupt occurs (see Figure 15).

HD-6406 Polling Operation

When utilizing a polling scheme for communications with the HD-6406, it is important to note that the UART status register will be cleared of its contents when it is read by the processor. Therefore, subsequent reads of this register will show the contents to be 00H unless the status of the device has changed between reads. Because of this, it would be necessary for a copy of the status to be saved so that the proper status can be seen.

A listing of the assembly language program for HD-6406 Polling operation is given in the Program Listing, Example 1, Page 15.

HD-6406 Interrupt Driven Operation

In this example, the 82C59A Interrupt Controller is being used to handle interrupts generated by the HD-6406. The 82C59A then communicates this interrupt information to the CPU so that it may be properly serviced. An example of how the 82C59A and HD-6406 are interfaced to the CPU is shown in Figure 14. The listing of the assembly language program for Interrupt Driven Operation is given in the Program Listing, Example 2, page 19.

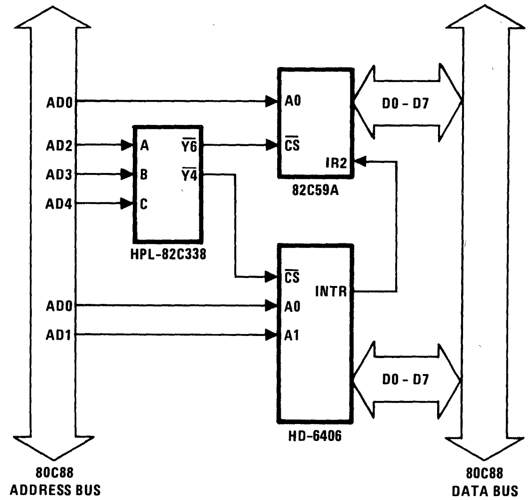


FIGURE 14. INTERRUPT DRIVEN SYSTEM

PROGRAM LISTING, EXAMPLE 1

```
NAME            EXAMPLE_1
; ****************************************************************************
;  HARRIS SEMICONDUCTOR                                           AUG 14, 1985
;  P.O. Box 883
;  Melbourne, FL  32901
;
;  Microprocessor Applications
;  JAGoss
;
;  EXAMPLE #1:      I/O Polling operation of the HD-6406 PACI.
;
;  This program sets up and runs the HD-6406 for polling operation.
;  It will input characters sent to it and place them into a data buffer.
;  When a carriage return is detected, no more data will be accepted.
;  The data will then be transmitted back to the sender.
; ****************************************************************************

;  The following are port addresses for accessing the HD-6406
;  in a demonstration system.

;  ------ 6406 Register Addresses ------

UCR             EQU     11H             ;UART control register
BRSR            EQU     13H             ;Baud Rate Select Register
MCR             EQU     12H             ;Modem Control Register
USR             EQU     11H             ;UART Status Register
MSR             EQU     13H             ;Modem Status Register
TBR             EQU     10H             ;Transmit Buffer Register
RBR             EQU     10H             ;Receive Buffer Register
```

PROGRAM LISTING, EXAMPLE 1

```
CARRIAGE RETURN EQU     0DH
LINE FEED       EQU     0AH
DR              EQU     80H                 ;Mask for checking DATA READY
TBRE            EQU     40H                 ;Mask for checking TRANSMIT BUFFER
                                            ;  REGISTER EMPTY


ASSUME          CS:DRIVER_6406,
&               DS:BUFFER_AREA,
&               SS:STACK_AREA

DRIVER_6406     SEGMENT         PUBLIC
; ***********************************************************
; *                           MAIN                           *
; ***********************************************************

MAIN            PROC    NEAR

SET UP:         MOV     AX,BUFFER_AREA  ;Set up the data segment
                MOV     DS,AX
                MOV     AX,STACK_AREA   ;Set up the stack segment
                MOV     SS,AX
                                        ;Set up the stack pointer
                MOV     SP,OFFSET STACK_AREA:TOP_OF_STACK

;  Initialize the HD-6406 PACI

                CALL    INIT_6406

;  Initialize the pointer into the data buffer.

BEGIN:          MOV     BX,OFFSET BUFFER
                XOR     DI,DI           ;Clear the index register

;  Read data from the HD-6406 and place it in the data buffer until
;  the CPU detects a carriage return.

READ:           CALL    CHAR_INPUT      ;Get a character from the keyboard
                MOV     [BX][DI],AL     ;Store the char. in the buffer
                INC     DI              ;Point to the next location in the
                                        ;  buffer.

;  Check to see if the character read was a carriage return.  If
;  it wasn't, then go read another character, otherwise we will
;  echo the data read-in back out of the HD-6406.

                CMP     AL,CARRIAGE_RETURN
                JNE     READ
```

PROGRAM LISTING, EXAMPLE 1

```
;  Print a line feed, then echo back the character string from the
;  input buffer...

                MOV     AL,LINE_FEED        ;Load the accumulator
                MOV     [BX][DI],AL         ;Put a line-feed at end of buffer

                INC     DI                  ;Point to next buffer location.
                CALL    CHAR_OUTPUT         ;Print the line-feed.
                MOV     CX,DI               ;Load the string length into counter
                XOR     DI,DI               ;Set DI to zero.

;  Print loop...

WRITE:          MOV     AL,[BX][DI]         ;Load char. from the buffer.
                CALL    CHAR_OUTPUT         ;Print the character
                LOOP    WRITE
                JMP     BEGIN               ;Start all over again...
MAIN            ENDP


INIT_6406       PROC    NEAR
; ****************************************************************
; *                         INIT_6406                            *
; ****************************************************************

;  This routine sets up the HD-6406 to communicate with a dumb
;  terminal.

;  Set up for 8 data bits, 1 stop bit, and no parity.

BEGIN_6406:     MOV     AL,00111111B
                OUT     UCR,AL

;  Set up BRSR for 9600 bps, assuming that the target system uses
;  a 2.4576 MHz clock crystal.

                MOV     AL,00000110B
                OUT     BRSR,AL

;  Disable interrupts on the 6406, enable the receiver, and
;  select normal mode.

                MOV     AL,00100000B
                OUT     MCR,AL

                RET                         ;Return to the MAIN
INIT_6406       ENDP
```

PROGRAM LISTING, EXAMPLE 1

```
CHAR_INPUT      PROC    NEAR
; ***********************************************************
; *                      CHAR_INPUT                         *
; ***********************************************************

POLL_IN:        NOP
                IN      AL,USR          ;Read the status register
                TEST    AL,DR           ;See if the data ready bit is set
                JZ      POLL_IN         ;If not, wait for data ready
                OR      STATUS_06,AL    ;Save the current state of status reg.
                IN      AL,RBR          ;Read the data from the Receiver reg.
                RET
CHAR_INPUT      ENDP

CHAR_OUTPUT     PROC    NEAR
; ***********************************************************
; *                      CHAR_OUTPUT                        *
; ***********************************************************

                PUSH    AX              ;Save the character to print
POLL_OUT:       NOP
                IN      AL,USR          ;Test to see if the transmit buffer
                CMP     AL,0            ;  has been cleared.  If so, then look
                JNE     CONTIN          ;  at the stored value of the USR.  If
                MOV     AL,STATUS_06    ;  either shows the transmit buffer to
CONTIN:         TEST    AL,TBRE         ;  be empty, send the char. to the RBR.
                JZ      POLL_OUT
                MOV     STATUS_06,0     ;Clear out the UART status word.
                POP     AX              ;Load the character to print.
                OUT     TBR,AL          ;Output the character...
                RET
CHAR_OUTPUT     ENDP
DRIVER_6406     ENDS

BUFFER_AREA     SEGMENT         PUBLIC
; ***********************************************************
; *                      BUFFER_AREA                        *
; ***********************************************************
BUFFER          DB      80 DUP(?)
STATUS_06       DB      ?
BUFFER_AREA     ENDS

STACK_AREA      SEGMENT         PUBLIC
; ***********************************************************
; *                      STACK_AREA                         *
; ***********************************************************
STACK           DW      80H DUP(?)
TOP_OF_STACK    LABEL   WORD
STACK_AREA      ENDS
                END
```

PROGRAM LISTING, EXAMPLE 2

```
NAME            EXAMPLE_2
;  *****************************************************************************
;  HARRIS SEMICONDUCTOR                                          AUG 14, 1985
;  P.O. Box 883
;  Melbourne, FL  32901
;
;  Microprocessor Applications
;  JAGoss
;
;  EXAMPLE #2:     Interrupt driven HD-6406.  We are also using an 92C59A
;                  Interrupt Controller in this system.
;
;  *****************************************************************************


;  The following are port addresses for the devices used in our example
;  system.  The devices that we will look at are the HD-6406 PACI, and the
;  two 82C59A Interrupt Controller.

;  ----- HD-6406 Register Addresses -----

UCR             EQU     11H             ;UART control register
BRSR            EQU     13H             ;Baud Rate Select Register
MCR             EQU     12H             ;Modem Control Register
USR             EQU     11H             ;UART Status Register
MSR             EQU     13H             ;Modem Status Register
TBR             EQU     10H             ;Transmit Buffer Register
RBR             EQU     10H             ;Receive Buffer Register

;  ---------- 82C59A Addresses ----------

ICW1            EQU     18H
ICW2            EQU     19H
ICW4            EQU     19H
OCW1            EQU     19H
OCW2            EQU     18H

CARRIAGE_RETURN EQU     0DH
LINE_FEED       EQU     0AH
DR              EQU     80H             ;Mask for checking DATA READY
TBRE            EQU     40H             ;Mask for checking TRANSMIT BUFFER
                                        ;  REGISTER EMPTY


ASSUME          CS:DRIVER_59A,
&               DS:BUFFER_AREA,
&               SS:STACK_AREA
```

PROGRAM LISTING, EXAMPLE 2

```
DRIVER_6406     SEGMENT         PUBLIC
; ***************************************************************
; *                          MAIN                               *
; ***************************************************************

MAIN            PROC     NEAR

SET_UP:         MOV      AX,BUFFER_AREA  ;Set up the data segment
                MOV      DS,AX
                MOV      AX,STACK_AREA   ;Set up the stack segment
                MOV      SS,AX
                                         ;Set up the stack pointer
                MOV      SP,OFFSET STACK_AREA:TOP_OF_STACK

;  Set up the interrupt vector table

                MOV      AX,OFFSET INT_SERVICE_ROUTINE
                MOV      ISR_34,AX
                MOV      ISR_34[2],CS

;  Initialize the pointer into the data buffer.

                MOV      BX,OFFSET BUFFER
                XOR      DI,DI           ;Clear the index register

;  Initialize the 82C59A

                CALL     INIT_82C59A

;  Initialize the HD-6406 PACI

                CALL     INIT_6406

;  Wait for interrupts from the '59A...

                STI                      ;Set the interrupt enable flag.
WAIT_LOOP:      NOP
                JMP      WAIT_LOOP

                HLT
MAIN            ENDP
```

PROGRAM LISTING, EXAMPLE 2

```
;  Set up for 8 data bits, 1 stop bit, and no parity.

BEGIN_6406:      MOV     AL,00111110B
                 OUT     UCR,AL

;  Set up BRSR for 9600 bps, assuming that the target system uses
;  a 2.4576 MHz clock crystal.

                 MOV     AL,00000110B
                 OUT     BRSR,AL

;  Enable interrupts on the 6406, enable the receiver, and
;  select normal mode.

                 MOV     AL,00100100B
                 OUT     MCR,AL

                 RET                      ;Return to the MAIN
INIT_6406        ENDP



INT_SERVICE_ROUTINE      PROC    NEAR
; *************************************************************
; *                      INT_SERVICE_ROUTINE                  *
; *************************************************************

ISR_START:       IN      AL,USR           ;Find out what caused the interrupt.
                 TEST    AL,DR            ;Was it DATA READY ?
                 JNZ     READ_DATA
                 TEST    AL,TBRE          ;Was it TRANSMIT BUFFER REG. EMPTY ?
                 JNZ     PRINT_BUFFER     ;If so, then print next character

;  If this condition was not detected, then we have an erroneous
;  interrupt from the HD-6406.  Rather than servicing this, we will
;  simply return from the service routine to the MAIN.

ERROR:           JMP     ISR_EXIT

;  Read the data that is present in the Receive Buffer Register.

READ_DATA:       IN      AL,RBR
                 MOV     [BX][DI],AL      ;Save the data in our buffer area.
                 INC     DI               ;Increment the index into the buffer.
                 CMP     AL,CARRIAGE_RETURN
                 JE      PRINT_LF

                 JMP     ISR_EXIT         ;Exit the service routine.

;  Set up for writing the data out to the Transmit Buffer...

PRINT_LF:        MOV     AL,LINE_FEED
                 MOV     [BX][DI],AL      ;Add a line feed to the buffer.
```

PROGRAM LISTING, EXAMPLE 2

```
; Set up for 8 data bits, 1 stop bit, and no parity.

BEGIN_6406:     MOV     AL,00111110B
                OUT     UCR,AL

; Set up BRSR for 9600 bps, assuming that the target system uses
; a 2.4576 MHz clock crystal.

                MOV     AL,00000110B
                OUT     BRSR,AL

; Enable interrupts on the 6406, enable the receiver, and
; select normal mode.

                MOV     AL,00100100B
                OUT     MCR,AL

                RET                     ;Return to the MAIN
INIT_6406       ENDP



INT_SERVICE_ROUTINE     PROC    NEAR
; ***************************************************************
; *                     INT_SERVICE_ROUTINE                      *
; ***************************************************************

ISR_START:      IN      AL,USR          ;Find out what caused the interrupt.
                TEST    AL,DR           ;Was it DATA READY ?
                JNZ     READ_DATA
                TEST    AL,TBRE         ;Was it TRANSMIT BUFFER REG. EMPTY ?
                JNZ     PRINT_BUFFER    ;If so, then print next character

; If this condition was not detected, then we have an erroneous
; interrupt from the HD-6406.  Rather than servicing this, we will
; simply return from the service routine to the MAIN.

ERROR:          JMP     ISR_EXIT

; Read the data that is present in the Receive Buffer Register.

READ_DATA:      IN      AL,RBR
                MOV     [BX][DI],AL     ;Save the data in our buffer area.
                INC     DI              ;Increment the index into the buffer.
                CMP     AL,CARRIAGE_RETURN
                JE      PRINT_LF

                JMP     ISR_EXIT        ;Exit the service routine.

; Set up for writing the data out to the Transmit Buffer...

PRINT_LF:       MOV     AL,LINE_FEED
                MOV     [BX][DI],AL     ;Add a line feed to the buffer.
```

PROGRAM LISTING, EXAMPLE 2

```
                INC     DI
                OUT     TBR,AL
                MOV     CX,DI           ;Load the buffer size into CX
                XOR     DI,DI           ;Set the index back to beginning
                                        ;  of the buffer.
                JMP     ISR_EXIT

;  Print out the contents of the buffer...

PRINT_BUFFER:   CMP     CX,0            ;Anything to print ?
                JNE     PRINT_CHAR      ;If so, then print it...
                JMP     ISR_EXIT        ;Else, ignore this interrupt...
PRINT_CHAR:     MOV     AL,[BX][DI]     ;Print the byte pointed to in buffer.
                OUT     TBR,AL
                INC     DI              ;Point to next character.
                LOOP    PRINT_CHAR      ;Print til end-of-buffer.

DONE_PRINTING:  XOR     DI,DI           ;Re-initialize pointer into buffer.

;  Exit from the service routine, sending out a non-specific EOI first.

ISR_EXIT:       MOV     AL,00100000B    ;Send out an End-of-Interrupt
                OUT     OCW2_S,AL       ;  to both master and slave.
                OUT     OCW2_M,AL
                IRET

INT_SERVICE_ROUTINE     ENDP
DRIVER_59A              ENDS


BUFFER_AREA     SEGMENT         PUBLIC
; *************************************************************
; *                        BUFFER_AREA                        *
; *************************************************************

                ORG     88H
ISR_34          DW      4 DUP(?)
                ORG     100H
BUFFER          DB      80 DUP(?)
BUFFER_AREA     ENDS


STACK_AREA      SEGMENT         PUBLIC
; *************************************************************
; *                        STACK_AREA                         *
; *************************************************************

STACK           DW      80H DUP(?)
TOP_OF_STACK    LABEL   WORD
STACK_AREA      ENDS
                END
```

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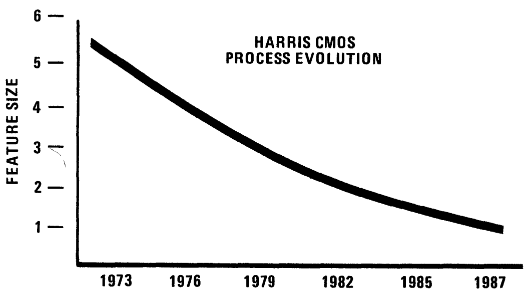
Technology Evolution

CMOS

The unique Harris SAJI (Self-Aligned Junction Isolation) CMOS process is the result of more than a decade of innovative design and manufacturing. It's a technology that's so refined, we use it throughout the Harris digital product line.

Increased Densities

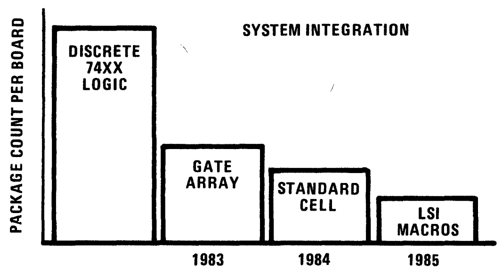
Harris CMOS technology uses industry-standard, local oxidation techniques with 2-micron effective channel lengths for improved performance. Packing densities are increased with a 2-micron feature size. Through our advanced process development program, we are increasing packing densities even further with the introduction of DLM process in 1986. This means a 30% reduction in chip sizes providing greater system integration and speed capability.



The low power requirements of CMOS allow the designer to take maximum advantage of these increased packing densities, and avoid power and heat dissipation problems associated with bipolar and NMOS devices. System speeds can be significantly improved by reducing chip-to-chip delays with the high functional level of integration offered by semicustom design.

Added System Value

Combining several functions onto a single chip provides tremendous benefits for the system designer. Harris semicustom solutions reduce part counts and simplify PC board layout and manufacture. The tight on-chip interconnect of functions minimizes parasitic capacitance, increases performance and reduces power. Lower power means increased reliability.



Simpler designs and fewer parts mean lower system cost. The addition of DLM process assures continued product and cost improvements. Harris semicustom means added value for your system.

Total Standard Cell Capabilities

STANDARD CELL LIBRARY

- Advanced LSI Cells
  - ▶ 80C86 Peripherals
  - ▶ Data Communications
  - ▶ Memory
- MSI/74XX Cells
  - ▶ Industry Standard 74XX Functions
  - ▶ Propagation Delays are Less than or Equal to 54/74XX and 54/74HC Circuits
- SSI/Primitive Cells
- I/O Cells
  - ▶ 10ns Delay into a 100pF Load
  - ▶ 6mA Source of Sink Current Over Military Temperature Range
  - ▶ TTL and CMOS Thresholds
  - ▶ Inputs, Outputs, and Bidirectionals

DESIGN AUTOMATION

- Hardware Support
  - ▶ Harris/VAX™ Super Minicomputer for Development Work
  - ▶ Workstation Compatibility *
    - — Daisy™
    - — SDA™ Workstation *
    - — Mentor™ *
    - — Other Workstations *
- Software Support
  - ▶ Schematic Capture
  - ▶ Logic/Circuit Simulation
    - — Logic and Functional Timing Simulation
    - — Testability Analysis
    - — Initial Capture of Gate Fanout and Interconnect Capacitance
    - — Fault Analysis Capability
    - — Test Program Generation
    - — Auto Place and Route Programs
  - ▶ Computer-Aided Design
    - — Parasitic Extraction-Back Annotation for Interconnect Loading
    - — Network Check Software for Interconnect Verification
    - — ERC/DRC Software Ground Rule Verification
    - — E-Beam Pattern Generator

TEST CAPABILITY

- Sentry Series VII, VIII, 20, 21
- Temperature Chambers
- IMS

BURN-IN CAPABILITY

PACKAGE OPTIONS

- Dual-In-Line Plastic
- Dual-In-Line Ceramic
- Ceramic Chip Carrier (Leadless)
- Plastic Chip Carrier (J-Leads)
- Ceramic Pin Grid Array

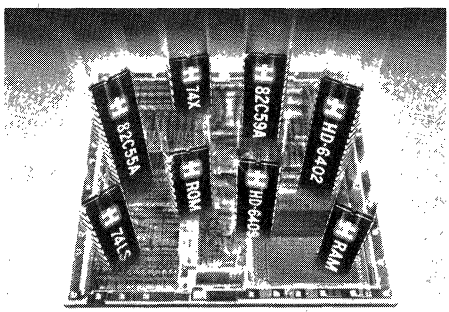
* Contact Harris for Workstation and Super Minicomputer Compatibility
VAX™ is a trademark of Digital Equipment Corporation
Daisy™ is a trademark of Daisy Systems Corporation
SDA™ is a trademark of Silicon Design Automation
Mentor™ is a trademark of Mentor Graphics

Advanced LSI Standard Cells

80C86 Peripheral LSI Cells

Harris has taken the next step in the race to keep ahead of increasing costs. Our standard microprocessor CMOS 80C86 peripheral standard cells make complex logic and microprocessor peripheral functions as easy to use as a simple NAND gate.

We've combined our 82CXX series of peripheral circuits, developed for the Harris 80C86 μP family, into advanced standard cells. Now you can take advantage of the proven reliability of these circuits in your own semicustom designs.



Data Communications/Memory

To complete the Harris family of LSI macros, we offer static RAMs, ROMs and a variety of data communications circuits. Choose an NRZ-based UART/BRG like our HD-6406 for your serial data communication needs. Or add one of our Manchester Encoder/Decoders for increased data transmission reliability.

LSI Standard Cell Library (Current and Future Cells)

CELL	DESCRIPTION	EQUIVALENT GATE COUNT
82C37A	DMA CONTROLLER	2900
82C50A	ASYNCHRONOUS COMMUNICATION ELEMENT	2680
82C50B	ASYNCHRONOUS COMMUNICATION ELEMENT	2680
82C52	UART/BRG	1899
82C54	PROGRAMMABLE INTERVAL TIMER	2540
82C55A	PARALLEL I/O	700
82C59A	PRIORITY INTERRUPT CONTROLLER	890
82C84A	CLOCK GENERATOR	385
82C85	STATIC CLOCK CONTROLLER	1540
82C88	BUS CONTROLLER	923
82C89	BUS ARBITER	754
HD4702	BAUD RATE GENERATOR	450
HD6402	UART	555
HD6406	UART/BRG/MODEM CONTROL	1899
HD6408	ASMA	600
HD6409	MANCHESTER ENCODER/DECODER	703
HD15530	MANCHESTER ENCODER/DECODER	600
HD15531	PROGRAMMABLE MANCHESTER ENCODER/DECODER	600
1K BIT	RECONFIGURABLE RAM X1, X4, X8	461
1K BIT	RECONFIGURABLE ROM X1, X4, X8	461

SSI/MSI Standard Cells

SSI/MSI

Also available are 74XX series compatible "Glue Logic" functions to provide a complete set of standard cells for your specific application. These SSI/MSI circuits are functionally compatible with industry-standard devices. In addition, our SSI/MSI standard cell library is open-ended, allowing you to define "Custom" cells for unique requirements.

MSI/74XX Standard Cell Library

MACRO	DESCRIPTION	GATE COUNT
SN7400	2 - NAND	1
SN7402	2 - NOR	1
SN7404	INVERTER	1
SN7407	BUFFER (5pF)	2
SN7408	2 - AND	2
SN7410	3 - NAND	2
SN7411	3 - AND	2
SN7420	4 - NAND	2
SN7421	4 - AND	3
SN7427	3 - NOR	2
SN7430	8 - NAND	6
SN7432	2 - OR	2
SN7442	BCD TO DECIMAL DECODER (4 TO 10)	24
SN7451	AND-OR-INVERT	7
SN7473	JK-FF W/R	14
SN7474	D-FF W/S & R	10
SN7475	4-BIT BISTABLE LATCH (Q, NOT (Q))	15
SN7476	JK-FF W/S & R	14
SN7477	4-BIT BISTABLE LATCH (Q)	13
SN7485	4-BIT MAG. COMPARATOR	48
SN7486	EXCLUSIVE OR	2
SN74109	J-NOT(K) FLIP-FLOP (S,R)	13
SN74113	NEGATIVE EDGE JK FLIP-FLOP (S)	14
SN74126	QUAD BUS BUFFERS W/THREE-STATE	8
SN74133	13-NAND	11
SN74137	3 TO 8 DECODER, WITH ADDRESS LATCHES	38
SN74138	3 TO 8 DECODER	20
SN74139	2 TO 4 DECODER	8
SN74147	10 TO 4 BCD ENCODER	31
SN74148	8 TO 3 ENCODER	28
SN74151	8 TO 1 SELECTOR (D,NOT(D))	25
SN74152	8 TO 1 SELECTOR	23
SN74153	DUAL 4 TO 1 SELECTORS W/ENABLE	20
SN74154	4 TO 16 DECODER	64
SN74157	2 TO 1 SELECTOR	13
SN74158	2 TO 1 SELECTOR (INVERT. OUTPUTS)	11
SN74160	4-BIT SYNC. DECADE COUNTER W/ASYNC. CLEAR	69
SN74161	4-BIT SYNC. BINARY COUNTER W/ASYNC. CLEAR	72
SN74162	4-BIT SYNC. DECADE COUNTER W/SYNC. CLEAR	78
SN-74163	4-BIT SYNC. BINARY COUNTER W/SYNC. CLEAR	79
SN74164	8-BIT SHIFT REGISTER	84
SN74165	8-BIT PARALLEL LOAD REGISTER	95
SN74166	8-BIT SHIFT REGISTER	108
SN74173	QUAD D FLIP-FLOP W/THREE-STATE & CLEAR	59
SN74174	HEX D FLIP-FLOPS	59
SN74175	QUAD D-FF W/R	39
SN74180	9-BIT PARITY GENERATOR	20
SN74181	4-BIT ALU	100
SN74182	LOOK AHEAD CARRY GENERATOR	32
SN74190	4-BIT SYNCHRONOUS U/D BCD COUNTER	103
SN74191	4-BIT SYNCHRONOUS U/D BIN. COUNTER	98
SN74192	4-BIT SYNCHRONOUS U/D BCD COUNTER	93
SN74193	4-BIT U/D BINARY COUNTER	81
SN74194	4-BIT UNIVERSAL SHIFT REGISTER	78
SN74195	4-BIT PARALLEL ACCESS SHIFT REGISTER	57
SN74237	3 TO 8 DECODER W/ADDRESS LATCHES	42
SN74238	3 TO 8 DECODER	29
SN74240	QUAD LINE DRIVERS (INVERTER OUTPUTS)	7
SN74241	DUAL 4-BIT BUFFERS W/THREE-STATE	17
SN74242	QUAD BUS TRANS. W/THREE-STATE (INV.)	14
SN74243	QUAD BUS TRANSCEIVERS W/THREE-STATE	18
SN74244	QUAD LINE DRIVERS	9
SN74245	OCTAL BUS TRANSCEIVERS W/THREE-STATE	32
SN74245	QUAD BUS TRANSCEIVERS W/THREE-STATE	17
SN74251	8 TO 1 SELECTOR W/THREE-STATE (D,NOT(D))	26
SN74253	DUAL 4 TO 1 SELECTORS W/THREE-STATE	21
SN74257	QUAD 2 TO 1 SELECTORS W/THREE-STATE	16
SN74258	QUAD 2 TO 1 SELECTORS (INVERTER OUTPUTS)	19
SN74259	8-BIT ADDRESSABLE LATCH	62
SN74273	OCTAL D-FF W/R	78
SN74280	9-BIT PARITY GENERATOR/CHECKER	19
SN74283	4-BIT FULL ADDER	34
SN74298	QUAD 2-INPUT MULTIPLEXERS, W/STORAGE	51
SN74352	DUAL 4 TO 1 SELECTOR	22
SN74373	OCTAL D LATCHES W/THREE-STATE	46
SN74373	OCTAL D LATCHES W/RESET	30
SN74374	OCTAL D FLIP-FLOP W/THREE-STATE OUTPUTS	90
SN74374	QUAD D FLIP-FLOPS W/THREE-STATE OUTPUTS	45
SN74377	OCTAL D-FF W/ENABLE	78
SN74393	4-BIT BINARY RIPPLE COUNTER W/R	40
SN74645	OCTAL BUS TRANSCEIVER	44
SN74670	4 x 4 RAM	107

SSI/MSI Standard Cells

SSI/Primitive Standard Cell Library

CELL	DESCRIPTION	GATE COUNT
SC1010	N - CHANNEL	.25
SC1020	P - CHANNEL	.25
SC1100	INVERTER	1
SC1110	INVERTER (2X-DRIVE)	1
SC1220	2 - NAND	1
SC1230	3 - NAND	2
SC1240	4 - NAND	2
SC1250	5 - AND	3
SC1320	2 - NOR	1
SC1330	3 - NOR	2
SC1340	4 - NOR	2
SC1420	EXCLUSIVE OR	2
SC1430	EXCLUSIVE NOR	2
SC1440	2 TO 1 MUX	3
SC1450	NOR LATCH	2
SC1460	A*NOT(B)	2
SC1470	THREE-STATE INVERTER (.5X-DRIVE)	2
SC1480	BUFFER (3X-DRIVE)	1
SC1490	THREE-STATE INVERTER (1X-DRIVE)	2
SC1510	NOT((A*B)+C)	2
SC1520	NOT((A+B)*C)	2
SC1530	D LATCH	3
SC1540	D LATCH (Q,NOT(Q))	4
SC1580	D LATCH THREE-STATE INVERTER (.5X-DRIVE)	6
SC1590	D LATCH (C,Q,R)	4
SC1610	NAND LATCH	2
SC1620	NOR LATCH WITH (2-RESETS)	3
SC1630	A+NOT(B)	2
SC1640	NOT((A+B+C)*D)	2
SC1650	NOT(A+B+CC*D))	2
SC1660	2-AND 2-NOR LATCH	2
SC1710	2-OR	2
SC1720	2-AND	2
SC1730	THREE-STATE INVERTER (NOT(C),(.5X))	2
SC1770	D-FF W/ACTIVE LOW RESET	7
SC1780	D-FF W/ACTIVE LOW RESET, NOT(Q)	8
SC1790	MUX D-FF W/ACTIVE LOW RESET	11
SC1800	SN7474 EQUIVALENT D FLIP-FLOP	10
SC1810	D-FLIP FLOP (Q,NOT(Q),R,C)	10
SC1820	D-FLIP FLOP (Q,NOT(Q),S,R,C)	10
SC1830	MUX DFF (Q,NOT(Q),S,R,C)	13
SC1840	D-FLIP FLOP (Q,NOT(Q),S,C)	10
SC1850	T FLIP FLOP W/S	10
SC1860	LOADABLE T FLIP-FLOP	12
SC1870	JK-FLIP FLOP (S)	13
SC1880	JK-FLIP FLOP (R)	13
SC1890	JK-FLIP FLOP (S,R)	13
SC1900	THREE-STATE INVERTER (2X)	2
SC1910	THREE-STATE 2-NOR	2
SC1920	NOT((A+B)*C*D*E)	3
SC1930	DELAY INVERTER (12ns)	1
SC1940	THREE-STATE 2-NOR NOT(C)	2
SC1950	ONE-SHOT (20ns PULSE)	4
SC1960	NOT(((A*B)+C)*D)	2
SC1970	NOT((A*B)+(C*D))	2
SC1980	NOT(((A+B)*C)+D)	2
SC2000	THREE-STATE INV. NOT(C)) (1X-DRIVE)	2
SC2030	3-AND	2
SC2060	NOT((A+B)*C*D)	2
SC2080	NOT((A*B*C)+D)	2
SC2090	DELAY INVERTER (6ns)	1
SC2100	NOT((A+B)*(C+D))	2
SC2110	NOT((A*B*C)+D+E)	3
SC2120	3-OR	2
SC2130	THREE-STATE INVERTER (2X-DRIVE)	2
SC2160	1-BIT FULL ADDER	9
SC2300	SCHMITT TRIGGER (INVERTER)	3
SC2310	BUS HOLD DEVICE	1
SC2320	PROGRAMMABLE DELAY ONE-SHOT	10-40

I/O Standard Cells

I/O Standard Cell Library

DESCRIPTION

- TTL Input/Pull Up
- TTL Input/Pull Down
- TTL Input
- CMOS Input
- TTL Schmitt Input
- Output - 100pF/10ns
- Open Drain P-Channel
- Open Drain N-Channel
- Bidirect/TTL Input
- Bidirect/TTL Input/Pull Up
- Bidirect/TTL Input/Pull Down
- Bidirect/CMOS Input
- Inverting Output
- Oscillator Cell, 2-30MHz

DEVELOPMENT FLOW CHART

CUSTOMER CAN ENTER AT:

(1) LOGIC DIAGRAM IN HSC FORMAT AND TRUTH TABLE

Submit Logic diagram in HSC format. With A.C. & D.C. electrical specifications and test truth table. Harris will complete the design and provide prototypes.

OR

(2) WORKSTATION LOGIC DATABASE AND TRUTH TABLE

Customer performs logic capture, and provides A.C. & D.C. electrical specifications and test word. Harris will complete the design and provide prototypes.

OR

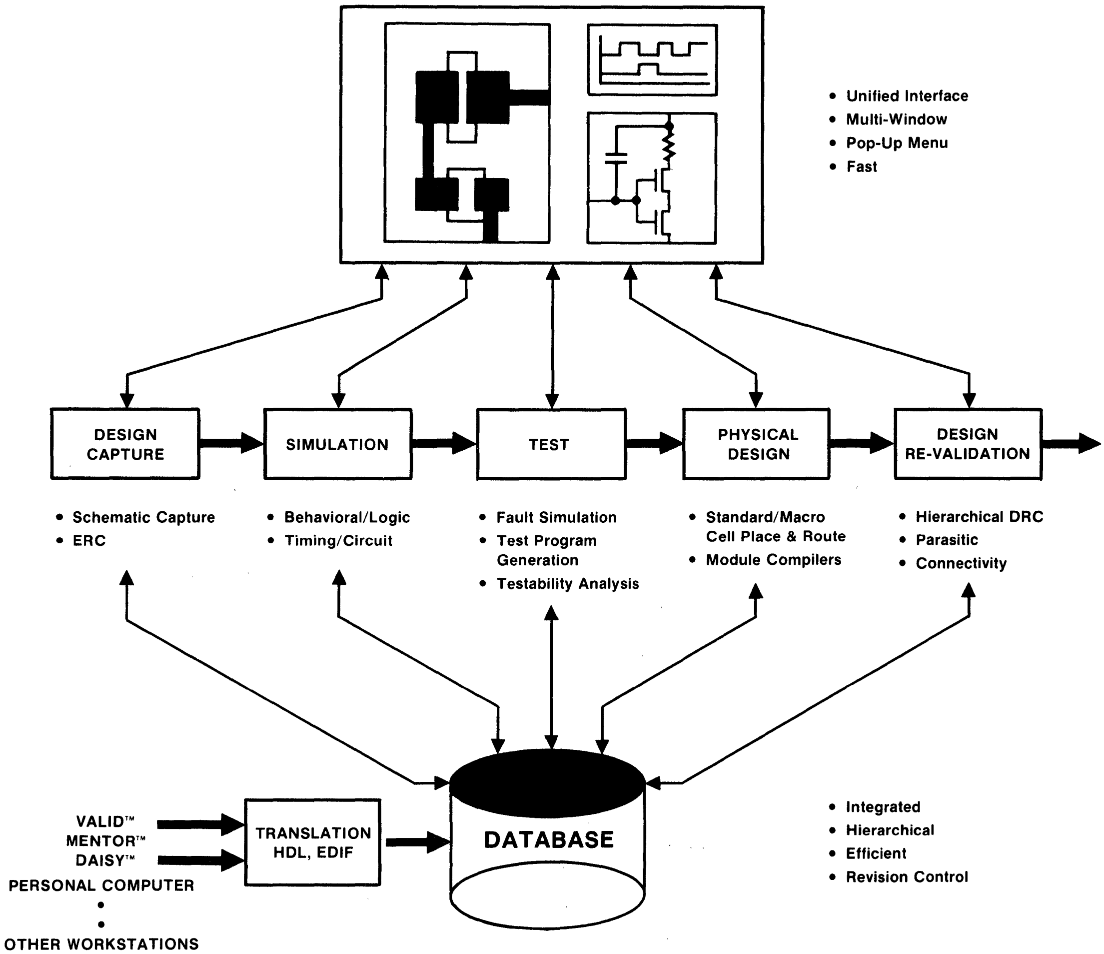
(3) WORKSTATION LOGIC, SIMULATION DATABASE AND TRUTH TABLE

Customer performs logic capture, simulation, and provides A.C. & D.C. electrical specifications and test word. Harris will complete layout and provide prototypes.

DEVELOPMENT STEP	DEVELOPMENT TASK
SCHEMATIC ENTRY TRUTH TABLE ENTRY A.C. & D.C. SPECIFICATION	Perform Schematic Capture and Truth Table Entry
LOGIC SIMULATION	Run Logic Simulator and Verify Functionality
DESIGN REVIEW	Harris and Customer Review Logic, Test Word, and Design
DEVELOP TEST PROGRAM	Run Automatic Test Program Generator
LAYOUT	Run Auto Place and Route Software-Generate Artwork
PHYSICAL AND ELECTRICAL VERIFICATION	Run Conductivity, Design and Electrical Rule Checks
TIMING VERIFICATION	Extract Interconnect Capacitance-Run Timing Verifier
LAYOUT REVIEW	Harris and Customer Hold Layout Review-Customer Approves Progress
PATTERN-GENERATION	Generate P. G. Tape
MASK FABRICATION	Produce E-Beam Mask
WAFER FABRICATION	Process Wafers at Harris Melbourne Facility
ASSEMBLY EVALUATION AND TEST	Engineering Evaluation and Test
SHIP PROTOTYPES	Quality Assurance Review and Ship Prototypes.

Harris Design System

Harris and SDA Integrated Tools



Valid™ is a trademark of Valid Logic Systems

Customer Support

Seminars

Harris is happy to provide a complete semicustom capabilities overview for you and your colleagues. Our Semicustom and System Design Seminar can be presented by field application personnel at your location or at Harris facililties. These programs will be outlined by Harris field application engineers during initial design and development.

Training

A training course is available to the system designer wishing to design standard cell integrated circuits using Harris semicustom services.

The course includes:

- Introduction to Semicustom
- Introduction to Workstations
- Preparation for Design
- Design Entering and Editing
- Logical Simulation and Testing
- Packaging and Device Test Requirements

Literature And Manuals for Each Technology Offered

- Semicustom Design Manual
- Cell Library Data Manual

Design Facilities

Harris provides in-house design capabilities at our Melbourne, Florida facility, complete with design workstations for customers preferring to work with design engineers. Workstations and design support can also be provided in the customers facilities as part of the design contract. Remote centers in key geographic locations will be established in the near future.

HARRIS

Standard Cell

HSC CMOS Cell Library

Features

- Low Power - CMOS Technology
- Single 5 Volt Supply
- Commercial-Industrial-Military Temperature Ranges
- Proven Reliable and Manufacturable Process
- CMOS and TTL Compatible Inputs and Outputs
- Large Library of SSI Primitive Cells
- 74XX Macro Function Library
- LSI Peripheral and Communication Cells
- Auto-Place and Auto-Route Capability
- I/O Cells Offer 10ns into 100 pF load
- Multiple Package Options

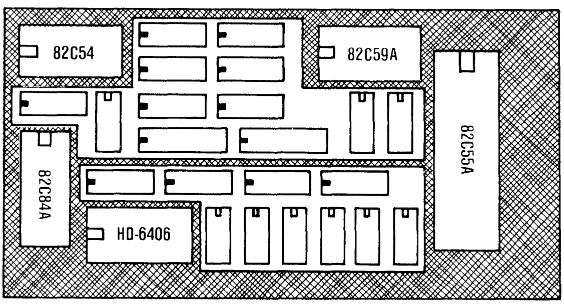
Description

The HSC STANDARD CELL LIBRARY is a proven, high performance library. It is implemented using Harris Semiconductor's advanced scaled SAJI IV CMOS process. The library offers predesigned and pre-characterized cells and macros for which the user prescribes the interconnections in order to develop an application specific IC.

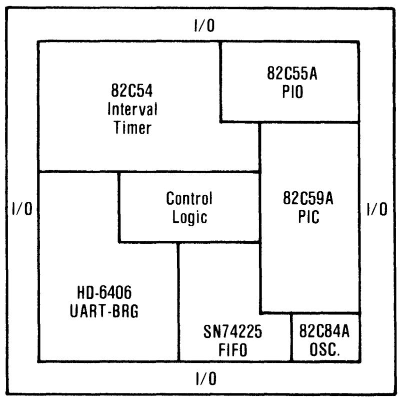
The library has a wide assortment of SSI primitive cells, 74XX macros, and a unique Harris offering of LSI cells. The LSI macros are a family of highly integrated micro processor peripheral and communication functions. The designer has the choice of intermixing cells or macros from any of the three groups to optimize the design implementation. The designer chooses the most familiar design method and group of functions.

The library is supported by design automation systems. The software includes schematic capture, logic simulation, auto-place, auto-route, electrical and design rule verification. The systems allow the users to perform the logic entry and simulation phases of the design process.

Standard Cell Solutions with LSI Macros



SSI/MSI GLUE LOGIC INTEGRATION
406 PINS



STANDARD CELL DESIGN
84 PINS

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage .... -0.5V to 7.0V
Input/Output Voltage .... VSS- 0.5V
VCC+ 0.5V
Input Diode Current 10mA
VI < 0 or VI > VCC
Output Diode Current 10mA
VO < 0 or VO > VCC
Power Dissipation 1000mW

Continuous Supply Pin Current
VCC or GND 100mA

Storage Temperature
Plastic .... -40 to $125^{o}C$
Ceramic .... -65 to $150^{o}C$
Continuous Current per Output 10mA

CAUTION: Stresses beyond those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliabilty.

Note: All applied voltages are with reference to ground (VSS).

Recommended Operating Conditions

D.C. Electrical Specifications

VCC = 5 ±10% T_A = Operating Temperature Range

SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITIONS
VCC	Operating Supply Voltage	4.5	5.5	V	
T_A	Operating Temperature				
	Commercial	0	70	C	
	Industrial	-40	85	C	
	Military	-55	125	C	
VIH	Input High Voltage TTL	2.2		V	
	CMOS	70% VCC			
VIL	Input Low Voltage TTL		0.8	V	
	CMOS		30% VCC		
II	Input Current				
	Standard	-1.0	+1.0	μA	VSS < VI < VCC
	Pull Up	-500	+1.0		
	Pull Down	-1.0	+500		
	Pull Up*	-50		μA	VI = 2.2
	Pull Down*		+50	μA	VI = 0.8
VOH	Output Voltage	2.4		V	IOH = -6.0mA
VOL	Output Voltage		0.4	V	IOL = 6.0mA
IOZ	Output Leakage	-10.0	+10.0	μA	VSS < VO < VCC HI - Z
CI**	Input Capacitance		7.0	pF	VI = VCC or VSS F = 1 MHz
CO**	Output Capacitance		10.0	pF	VO = VCC or VSS F = 1 MHz
CIO**	Input/Output Capacitance		15.0	pF	VO = VCC or VSS F = 1 MHz
ICCSB	Stand-By Supply (Inputs closed, Outputs open)		10	μA	VI = VCC or VSS II = 0; IO = 0

* Maximum input current for which specified VI will be maintained.
** Sampled and guaranteed but not 100% tested. These values may vary by package type.

A.C. Performance

The propagation delay time of a CMOS gate depends on many factors. Supply voltage, temperature, processing parameters, and output loading are the main influencing factors. Each HSC data sheet has an equation for every delay time associated with that cell to accurately predict the propagation delay for any combination of parameters. Propagation delay times can be estimated for each electrical net in the design using information such as fanout, interconnect capacitance, and the parameters listed above.

The simple example shown in Figure 1 will help illustrate the procedure. Assume that an SC1220 2-input NAND gate is driving two other inputs of a similar gate. To calculate the propagation delay for the conditions, T_A = 70 ^oC , VCC = 4.5 volts, and worst case processing parameters appropriate multipliers would be chosen for each condition from the tables below.

70^{o}C	-- 1.18
4.5 volts	-- 1.12
Worst case processing	-- 1.62

Additional assumptions include an after routing, interconnect capacitance of 0.2pF. From the data sheet for the SC1220, the equation for TPLH at 25^{o}C, 5.0 volts, and nominal process conditions is:

TPLH = 1.67ns + 0.2ns/fo + 1.14ns/pF-interconnect
TPLH = 1.67ns + 0.2ns(2) + 1.14ns(0.2)
TPLH = 2.1 ns

The effects of temperature, voltage, and processing conditions must be accounted for. By multiplying the nominal value for TPLH from above by the appropriate derating factors we get:

TPLH = 2.1ns * 1.18 * 1.12 * 1.62
TPLH = 4.5nS (70^{o}C, 4.5 volts, Worst Case Process Parameters)

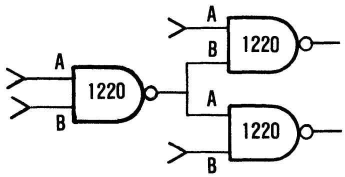


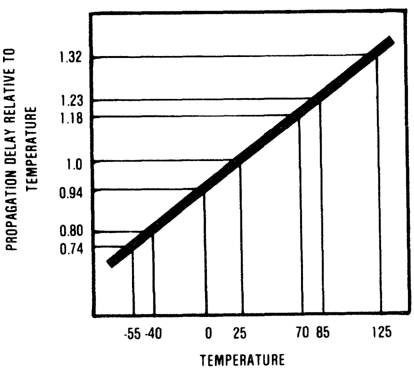
FIGURE 1.

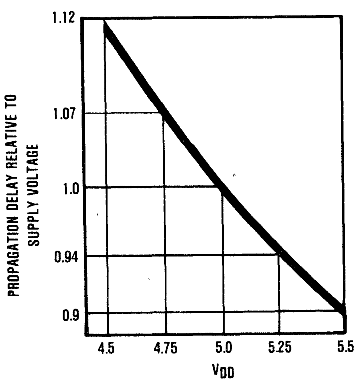
After the User has the logic in the HDL format timing calculation are performed automatically.

Derating Curves

Process Parameters Derating

P-channel	N-channel	Multiplier
Best	Best	0.76
Nominal	Nominal	1.0
Worst	Worst	1.62





CMOS

Harris Programmable Logic

6

PAGE

6 PROGRAMMABLE LOGIC

HPL-16LC8

CMOS HPL™ Harris Programmable Logic

Features

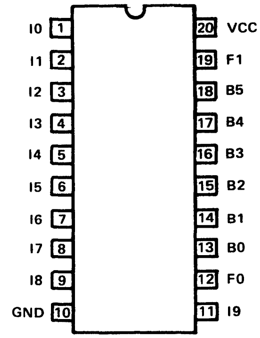
- Pin & Function Compatible with the Bipolar 16L8 and 16P8
- Scaled SAJI IV CMOS Process
- Fast Access (Input to Output) .... 125ns Max.
- Ultra-low Standby Power .... ICCSB = 150μA
- Low Operating Power .... ICCOP = 6mA/MHz
- Wide Operating Temperature Ranges:
  - HPL-16LC8-5 .... 0°C to +75°C
  - HPL-16LC8-9 .... -40°C to +85°C
  - HPL-16LC8-2/-8 .... -55°C to +125°C
- Programmable Output Polarity
- 20-pin Slimline DIP
- Security Fuse for Pattern Protection
- TTL/CMOS Compatible Inputs/Outputs for Mixed System Compatibility
- Logic Paths Tested to Insure Functionality

Applications

- Random Logic Replacement
- Code Converters
- Address Decoding
- Fault Detectors
- Boolean Function Generators
- Digital Multiplexers
- Parity Generators
- Pattern Recognition
- ROM Patching

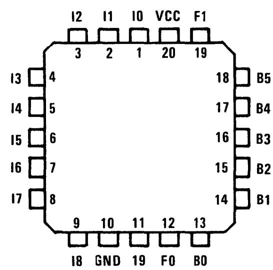
Pinouts

TOP VIEW



LCC

TOP VIEW



Description

The HPL-16LC8 is a CMOS Programmable Logic Device designed to provide a high performance, low power alternative to the industry standard 16L8 and 16P8 programmable logic devices.

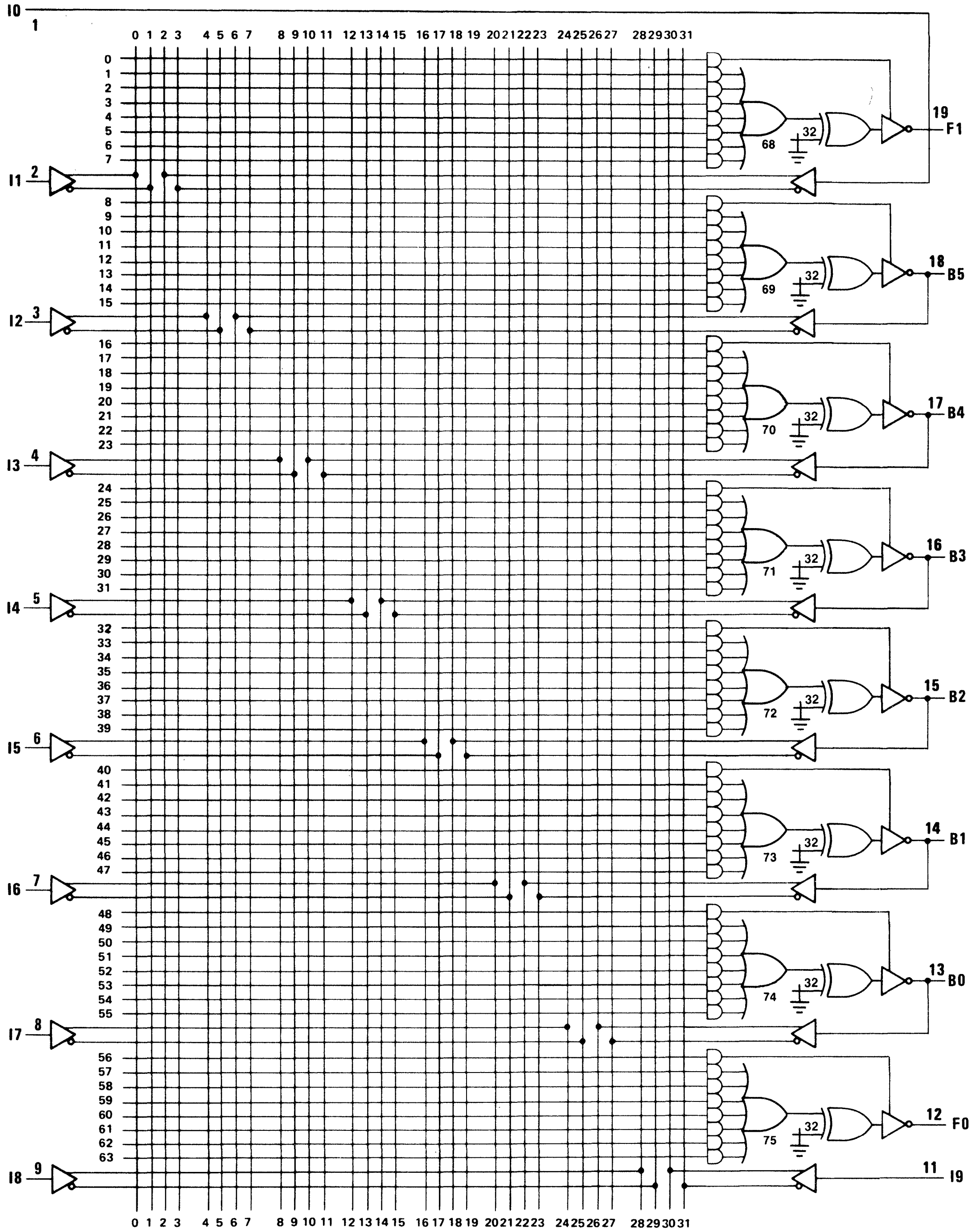
In addition to the low power advantage of this device over its bipolar counterparts the HPL-16LC8 contains programmable output polarity, allowing the user to individually select each output as either active-high or active-low. When all output polarity fuses are left intact, all active outputs are active-low.

The Harris fuse link technology provides a permanent fuse with stable storage characteristics over the full temperature ranges of 0°C to +75°C, -40°C to +85°C and -55°C to +125°C. Like all Harris Programmable Logic (HPL), this device contains unique test circuitry developed by Harris which allows AC, DC and functional testing before programming.

On-chip automatic power-down circuitry places internal circuitry into an ultra-low ICCSB power mode after output data becomes valid.

CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I. C. handling procedures should be followed.

Functional Diagram



Absolute Maximum Ratings*

Supply Voltage .... 0.00V to +8.00V
Operating Supply Voltage .... +4.00V to +6.00V
Input Voltage .... GND -0.5V to VCC +0.5V
Output Voltage .... GND -0.5V to VCC +0.5V
Storage Temperature .... -65°C to +150°C

Operating Temperature (Ambient)

Operating Temperature (Ambient):

HPL-16LC8-5 .... 0°C to +75°C
HPL-16LC8-9 .... -40°C to +85°C
HPL-16LC8-2/-8 .... -55°C to +125°C

** CAUTION: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. While programming refer to the " Programming Specifications."*

D.C. Electrical Specifications (Operating)

HPL-16LC8-5 (VCC = 5.0 V ± 10%, TA = 0°C to +75°C)
HPL-16LC8-9 (VCC = 5.0 V ± 10%, TA = -40°C to +85°C)
HPL-16LC8-2/-8 (VCC = 5.0 V ± 10%, TA = -55°C to +125°C)

SYMBOL	PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS (3)
IIH IIL	Dedicated Input Current	"1" "0"		+1 -1	μA μA	VIH = VCC MAX VIL = 0V VCC = VCC MAX
IFZH IFZL	Output Current Hi-Z State	"1" "0"		+10 -10	μA μA	VFH =VCC MAX VFL = 0V VCC = VCC MAX
IBZH IBZL	Bidirectional Hi-Z Current	"1" "0"		+10 -10	μA μA	VBH = VCC MAX VBL = 0V VCC = VCC MAX
VIH VIL	Input Threshold Voltage (1)	"1" "0"	2.0	 0.8	V V	VCC = VCC MAX VCC = VCC MIN
VOH1 VOH2 VOL	Output Voltage (2) Output Voltage	"1" "1" "0"	3.0 VCC-0.4	 0.4	V V V	IOH1 = -5.0 mA IOH2 = -1.0 mA VCC MIN, VIL MAX, VIH MIN IOL = +5.0 mA
ICCSB	Standby Power Supply Current			150	μA	VI = VCC or GND IF = 0.00 μa, VCC = VCC MAX
ICCOP	Operating Power Supply Current			6	mA/Mhz	VI = VCC or GND IF = 0.00 μa, VCC = VCC MAX

(1) These specifications apply to both Input (I) and Bidirectional (B) Pins.
(2) These specifications apply to both Output (F) and Bidirectional (B) Pins.
(3) All DC parameters tested under worst case conditions.

A.C. Switching Specifications (1) (Operating)

HPL-16LC8-5 (VCC = 5.0 V ± 10%, TA = 0°C to +75°C)
HPL-16LC8-9 (VCC = 5.0 V ± 10%, TA = -40°C to +85°C)
HPL-16LC8-2/-8 (VCC = 5.0 V ± 10%, TA = -55°C to +125°C)

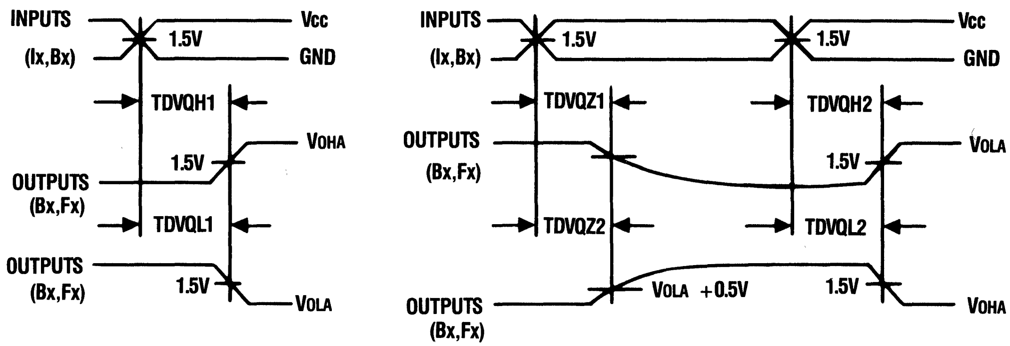
SYMBOL			HPL-16LC8-5		HPL-16LC8-9		HPL-16LC8-2/-8		
JEDEC STANDARD	OLD SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
TDVQH1	TPD	Propagation delay I or B to Output High	-	125	-	125	-	125	ns
TDVQL1	TPD	Propagation delay I or B to Output Low	-	125	-	125	-	125	ns
TDVQH2	TPZX	Enable Access Time to Output High (2)	TDVQZ1	125	TDVQZ1	125	TDVQZ1	125	ns
TDVQL2	TPZX	Enable Access Time to Output Low (2)	TDVQZ2	125	TDVQZ2	125	TDVQZ2	125	ns
TDVQZ1	TPXZ	Disable Access Time from Output High	-	125	-	125	-	125	ns
TDVQZ2	TPXZ	Disable Access Time from Output Low	-	125	-	125	-	125	ns

(1) All AC parameters are tested under worst case conditions.
(2) Enable access time is guaranteed to be greater than disable access time to avoid device contention.

Capacitance: $T_A = +25^oC$ (NOTE: Sampled and guaranteed - but not 100% tested.)

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance	5	pF	VI =VCC or GND f = 1 MHz
CF	Output Capacitance	10	pF	VF = VCC or GND f = 1 MHz
CB	Bidirectional Capacitance	12	pF	VB = VCC or GND f = 1 MHz

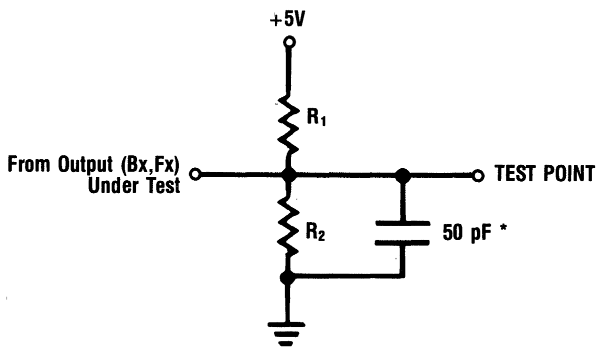
Switching Time Definitions



INPUT CONDITIONS: t_r, t_f = 5ns (10% to 90%)

NOTE: Disable access time is the time taken for the output to reach a high impedance state when the three-state product term drives the output inactive. The high impedance state is defined as a point on the waveform equal to a ΔV of 0.5V from VOHA or VOLA, the active output level.

A.C. Test Load



* Includes Jig and Probe
Total Capacitance

SYMBOL	PARAMETER	TEST LOAD VALUES R1	TEST LOAD VALUES R2
TDVQH1	Propagation Delay from Input or I/O to Active High Input	OPEN	OPEN
TDVQL1	Propagation Delay from Input or I/O to Active Low Output	OPEN	OPEN
TDVQH2	Enable Access Time to Active High Output	OPEN	920 ohms
TDVQL2	Enable Access Time to Active Low Output	920 ohms	OPEN
TDVQZ1	Disable Access Time from Actve High Output	OPEN	920 ohms
TDVQZ2	Disable Access Time from Active Low Output	920 ohms	OPEN

Programming

Following is the programming procedure which is used for the HPL-16LC8 programmable logic device. This device is manufactured with all fuses intact. Any desired fuse can be programmed by following the simple procedure shown on the following page. One may build a programmer to satisfy the specifications described in the table, or use any of the commercially available programmers which meets these specifications. Please contact Harris for a list of approved programmers.

TABLE 1

PROGRAMMING SPECIFICATIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNITS
VCCP	VCC Voltage During Programming		11.50	12.00	12.00	V
VCCV	VCC Voltage During Verify		4.75	5.00	5.25	V
ICCP	ICC Limit During Programming			100	200	mA
VNEG	Edit Enable & Mode Select Voltage		−5.00	−5.00	−7.00	V
INEG	Edit Enable & Mode Select Current				−5.00	mA
VIL	Input Voltage Low		0.00	0.00	0.80	V
VIHV	Input Voltage High	verify (1)	VCCV−2	VCCV	VCCV	V
VIHP	Input Voltage High	programming (1)	VCCP−2	VCCP	VCCP	V
IILP	Input Current Low	VIL = 0.0V		0	1	μA
IIHV	Input Current High	verify		0	1	μA
IIHP	Input Current High	programming		0	1	μA
VSI	Verify voltage	Intact Fuse	3.00	3.30		V
VSP	Verify voltage	Programmed Fuse		0.00	0.50	V
TV	Verify Pulse Delay		500	750	1000	μsec
PWP	Programming Width		4.5	5.1	5.5	msec
td	Pulse Seq. Delay		1	1	—	μsec
tr	Signal Rise Time	10% to 90%	0.01	0.1	1	μsec
tr2	VCC Rise Time	10% to 90%	0.01	0.1	5	μsec
tf1	Signal Fall Time	90% to 10%	0.01	0.1	1	μsec
tf2	VCC Fall Time	90% to 10%	0.01	0.1	5	μsec
tNEG	Mode Select Width		1	1	—	μsec
TPP	Programming Period			5.2		msec
FL	Fuse Attempts/Link		1	1	2	cycles

(1) Inputs defined as logic "1" (VIHV or VIHP) must track the VCC power supply when the supply is raised or lowered. The input levels should never exceed the level on the VCC Pin.

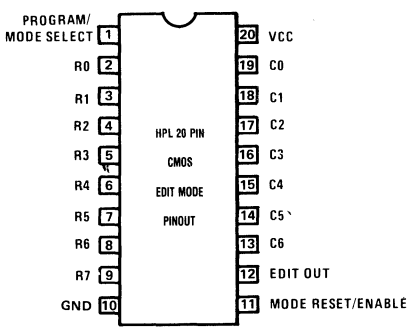


Figure 1
Edit mode pinout
HPL-16LC8

NOTES:
* While programming the CMOS HPL device, no pins should be left floating. EDIT OUT appears as an open drain output during programming. It should be tied to GND through a 1M-ohm resistor.
* CMOS HPL outputs are not put into a high impedance state (suitable for row and column address application) until the device is reset and put into the edit mode. For this reason it is recommended that the outputs be left floating until the edit mode is enabled or that the outputs be driven thru a 2k-ohm resistor.
* It is suggested that a 0.01 μf capacitor be put between VCC and GND to minimize VCC voltage spikes. Also, particular care should be exercised in regards to transients on the MODE SELECT and MODE RESET pins which could place the device in the incorrect mode.

Programming Procedure

1) Set-Up:

NOTE: Refer to the Figure 1 for the pin definitions, Table 1 for the timing and level definitions, Tables 3 & 4 for the address decoding.

a. During programming, no pins should be left floating.
b. EDIT OUT (Pin 12) should be terminated with a 1 M-ohm (± 1%) resistor to GND and stray capacitances on this pin should be ≤50 pf.
c. Set GND to 0.00 volts.
d. Outputs are only in a high impedance state (and available for addressing of edit mode rows and columns) while in Edit Modes 1 thru 4. Do not apply signals to these pins until a valid Edit Mode is entered.
e. All input and bi-directional pins should be at zero volts nominal with a maximum of 0.3 volts applied.
f. Apply VCCV to the part. No input should ever exceed the level on the VCC PIN.

2) Mode Reset/Edit Enable:

a. Wait td and reset the edit control logic by pulsing the MODE RESET PIN to VNEG for tNEG.
b. Wait td and enable Edit mode by applying VNEG to the EDIT ENABLE PIN.

3) Mode Select:

a. Wait td and select EDIT MODE 1 by pulsing the MODE SELECT PIN to VNEG for tNEG. Subsequent pulses will increment the mode to 2, 3 and 4 sequentially (sequencing the device beyond mode 4 will result in unpredictable results—if in doubt, return to STEP 2).
b. Verify entry into the proper mode by addressing column 64 and the row indicated in Table 2, waiting TV and monitoring the EDIT OUT PIN for the proper data.
c. Address column 65 and the row indicated in Table 2, wait TV and monitor the EDIT OUT PIN for the proper data. If both Steps 3b & 3c are correct, then the proper mode has been selected.
d. To re-enter a mode lower than the current mode, return to Step 2. Mode 1 can only be (re-)entered from Step 2.

4) Fuse Select:

NOTE: The voltage for a logical "1" (VIHP) must not exceed VCCP and must track VCCP as it rises from VCCV in Step 5.

a. Wait td and select a row by applying the appropriate address from Table 3.
b. Select a column by applying the appropriate address from Table 4.

5) Verify Intact Fuse:

NOTE: Skip this step for post-programming verify.

b. If EDIT OUT has indicated less than VSI, the fuse is not intact. Reject this devide for a non-blank matrix.

6) Program the Fuse:

NOTE: The PROTECT and POLARITY fuses can be accessed from either mode 1 or mode 3 by applying the addresses indicated in Tables 3 & 4.
THE 'PROTECT' FUSE SHOULD NOT BE PROGRAMMED UNTIL ALL OTHER FUSES HAVE BEEN PROGRAMMED AND VERIFIED AS PROGRAMMING THIS FUSE DEFEATS ALL FURTHER VERIFICATION!

a. Wait td and raise the VCC PIN to VCCP (allow VIHP to track this rise).
b. Wait td and pulse the PROGRAM PIN (Pin 1) to VIHP for a duration of PWP.
c. Wait td and lower the VCC PIN to VCCV (allow VIHP to track this fall).

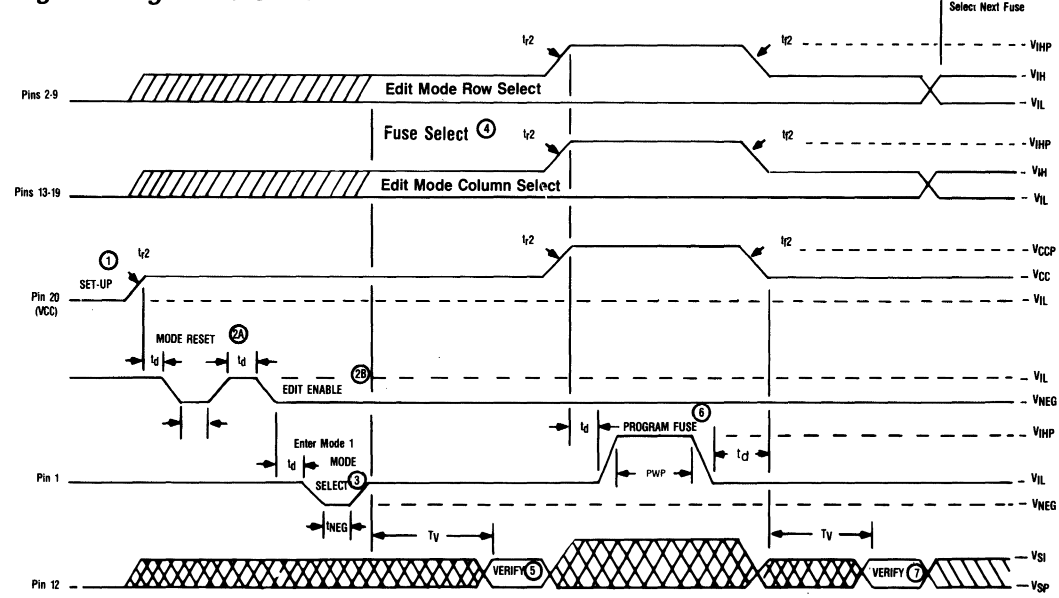
7) Verify Fuse:

a. Wait TV and monitor EDIT OUT for VSP (or VSI if verifying an intact fuse).
b. If EDIT OUT has indicated greater than VSP for an attempted programmed fuse, repeat Step 6 so that the fuse receives a maximum of FL fusing attempts.

8) Repeat Steps 4 through 7 for all addresses in a given mode.

9) Repeat Steps 3 through 8 for all modes.

Programming Waveforms



NOTE: Pins 13-19 are not necessarily three-stated and available for application of column address input signals until a valid edit mode is entered. Refer to the edit mode pinout (Figure 1) for further details.

Programming Procedure

Mode Verification
Table 2

MODE	COLUMN NUMBER	ROW NUMBER	EDIT OUT (PIN 12) LOGICAL LEVEL
1	64	0	0
	65	0	0
2	64	1	0
	65	1	1
3	64	2	1
	65	2	0
4	64	3	1
	65	3	1

NOTES: • At least two addresses must be checked to verify the proper edit mode.
• The conversion from the decimal column and row addresses in the table above to the actual pin levels can be made in Tables 3 and 4.

Edit Mode Row Select
Table 3

PROG. MODE	ROW NUMBER	R7 Pin 9	R6 Pin 8	R5 Pin 7	R4 Pin 6	R3 Pin 5	R2 Pin 4	R1 Pin 3	R0 Pin 2	VARIABLE
1	0	H	H	H	H	H	H	H	L	I1
	4	H	H	H	H	H	H	L	H	I2
	8	H	H	H	H	H	L	H	H	I3
	12	H	H	H	H	L	H	H	H	I4
	16	H	H	H	L	H	H	H	H	I5
	20	H	H	L	H	H	H	H	H	I6
	24	H	L	H	H	H	H	H	H	I7
	28	L	H	H	H	H	H	H	H	I8
2	1	L	L	L	L	L	L	L	H	/I1
	5	L	L	L	L	L	L	H	L	/I2
	9	L	L	L	L	L	H	L	L	/I3
	13	L	L	L	L	H	L	L	L	/I4
	17	L	L	L	H	L	L	L	L	/I5
	21	L	L	H	L	L	L	L	L	/I6
	25	L	H	L	L	L	L	L	L	/I7
	29	H	L	L	L	L	L	L	L	/I8
3	2	H	H	H	H	H	H	H	L	I0
	6	H	H	H	H	H	H	L	H	B5
	10	H	H	H	H	H	L	H	H	B4
	14	H	H	H	H	L	H	H	H	B3
	18	H	H	H	L	H	H	H	H	B2
	22	H	H	L	H	H	H	H	H	B1
	26	H	L	H	H	H	H	H	H	B0
	30	L	H	H	H	H	H	H	H	I9
4	3	L	L	L	L	L	L	L	H	/I0
	7	L	L	L	L	L	L	H	L	/B5
	11	L	L	L	L	L	H	L	L	/B4
	15	L	L	L	L	H	L	L	L	/B3
	19	L	L	L	H	L	L	L	L	/B2
	23	L	L	H	L	L	L	L	L	/B1
	27	L	H	L	L	L	L	L	L	/B0
	31	H	L	L	L	L	L	L	L	/I9
1 or 3	32	H	H	H	H	H	H	H	H	CONFIGURE

NOTE: The configuration row can be selected while in either mode 1 or mode 3.

Edit Mode Column Select
Table 4

COLUMN NUMBER	C6 Pin 13	C5 Pin 14	C4 Pin 15	C3 Pin 16	C2 Pin 17	C1 Pin 18	C0 Pin 19	
0	L	L	L	L	L	L	L	PRODUCT TERMS
1	L	L	L	L	L	L	H	
2	L	L	L	L	L	H	L	
3	L	L	L	L	L	H	H	
4	L	L	L	L	H	L	L	
5	L	L	L	L	H	L	H	
6	L	L	L	L	H	H	L	
7	L	L	L	L	H	H	H	
8	L	L	L	H	L	L	L	
9	L	L	L	H	L	L	H	
10	L	L	L	H	L	H	L	
11	L	L	L	H	L	H	H	
12	L	L	L	H	H	L	L	
13	L	L	L	H	H	L	H	
14	L	L	L	H	H	H	L	
15	L	L	L	H	H	H	H	
16	L	L	H	L	L	L	L	
17	L	L	H	L	L	L	H	
18	L	L	H	L	L	H	L	
19	L	L	H	L	L	H	H	
20	L	L	H	L	H	L	L	
21	L	L	H	L	H	L	H	
22	L	L	H	L	H	H	L	
23	L	L	H	L	H	H	H	
24	L	L	H	H	L	L	L	
25	L	L	H	H	L	L	H	
26	L	L	H	H	L	H	L	
27	L	L	H	H	L	H	H	
28	L	L	H	H	H	L	L	
29	L	L	H	H	H	L	H	
30	L	L	H	H	H	H	L	
31	L	L	H	H	H	H	H	
32	L	H	L	L	L	L	L	
33	L	H	L	L	L	L	H	
34	L	H	L	L	L	H	L	
35	L	H	L	L	L	H	H	
36	L	H	L	L	H	L	L	
37	L	H	L	L	H	L	H	
38	L	H	L	L	H	H	L	
39	L	H	L	L	H	H	H	
40	L	H	L	H	L	L	L	
41	L	H	L	H	L	L	H	
42	L	H	L	H	L	H	L	
43	L	H	L	H	L	H	H	
44	L	H	L	H	H	L	L	
45	L	H	L	H	H	L	H	
46	L	H	L	H	H	H	L	
47	L	H	L	H	H	H	H	
48	L	H	H	L	L	L	L	
49	L	H	H	L	L	L	H	
50	L	H	H	L	L	H	L	
51	L	H	H	L	L	H	H	
52	L	H	H	L	H	L	L	
53	L	H	H	L	H	L	H	
54	L	H	H	L	H	H	L	
55	L	H	H	L	H	H	H	
56	L	H	H	H	L	L	L	
57	L	H	H	H	L	L	H	
58	L	H	H	H	L	H	L	
59	L	H	H	H	L	H	H	
60	L	H	H	H	H	L	L	
61	L	H	H	H	H	L	H	
62	L	H	H	H	H	H	L	
63	L	H	H	H	H	H	H	
64	H	L	L	L	L	L	L	MODE VERIFY
65	H	L	L	L	L	L	H	
68	H	L	L	L	H	L	L	Pin 19 OUTPUT POLARITY
69	H	L	L	L	H	L	H	Pin 18
70	H	L	L	L	H	H	L	Pin 17
71	H	L	L	L	H	H	H	Pin 16
72	H	L	L	H	L	L	L	Pin 15
73	H	L	L	H	L	L	H	Pin 14
74	H	L	L	H	L	H	L	Pin 13
75	H	L	L	H	L	H	H	Pin 12
76	H	L	L	H	H	L	L	PROTECT

LEGEND: L = Logic Low H = Logic High.

HARRIS

HPL-16RC8
HPL-16RC6
HPL-16RC4

CMOS HPL™ Harris Programmable Logic

Features

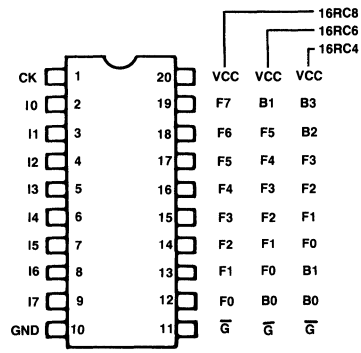
- Pin & Function Compatible with the Bipolar 16R8, 16R6 and 16R4
- Scaled SAJI IV CMOS Process
- Fast Access .... Input to Output 125ns Max.
  .... Clock to Output 60ns Max.
- Low Standby and Operating Power ▸ ICCSB = 150µA
  ▸ ICCOP = 7mA/MHz
- Wide Operating Temperature Ranges:
  - ▸ HPL-16RC8-5, HPL-16RC6-5, HPL-16RC4-5..........0°C to +75°C
  - ▸ HPL-16RC8-9, HPL-16RC6-9, HPL-16RC4-9....... -40°C to +85°C
  - ▸ HPL-16RC8-2/-8, HPL-16RC6-2/-8, HPL-16RC4-2/-8.. -55°C to +125°C
- 20 Pin Dual-In-Line Package
- Security Fuse for Pattern Protection
- TTL/CMOS Compatible Inputs/Outputs for Mixed System Compatibility
- Logic Paths Tested to Insure Functionality
- Programmable Output Polarity

Applications

- Random Logic Replacement
- Code Converters
- Address Decoding
- Custom Shift Registers
- Boolean Function Generators
- Digital Multiplexers
- Parity Generators
- Pattern Recognition
- State Machine Design

Pinouts

TOP VIEW



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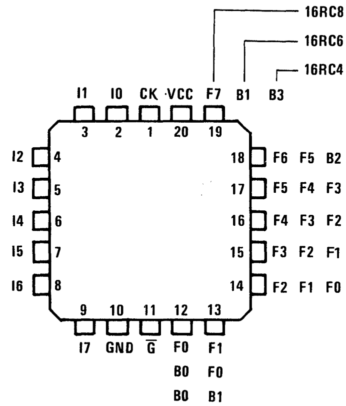
TOP VIEW



Description

The HPL-16RC8, HPL-16RC6, and HPL-16RC4 are CMOS Programmable Logic Devices designed to provide high performance, low power alternatives to the industry standard 16RC8, 16RC6, and 16RC4 bipolar programmable logic devices.

In addition to the low power advantage of these devices over their bipolar counterparts, the HPL-16RC8, HPL-16RC6, and HPL-16RC4 contain programmable output polarity, allowing the user to individually select each output as either active-high or active-low. When all output polarity fuses are left intact, all active outputs are active-low.

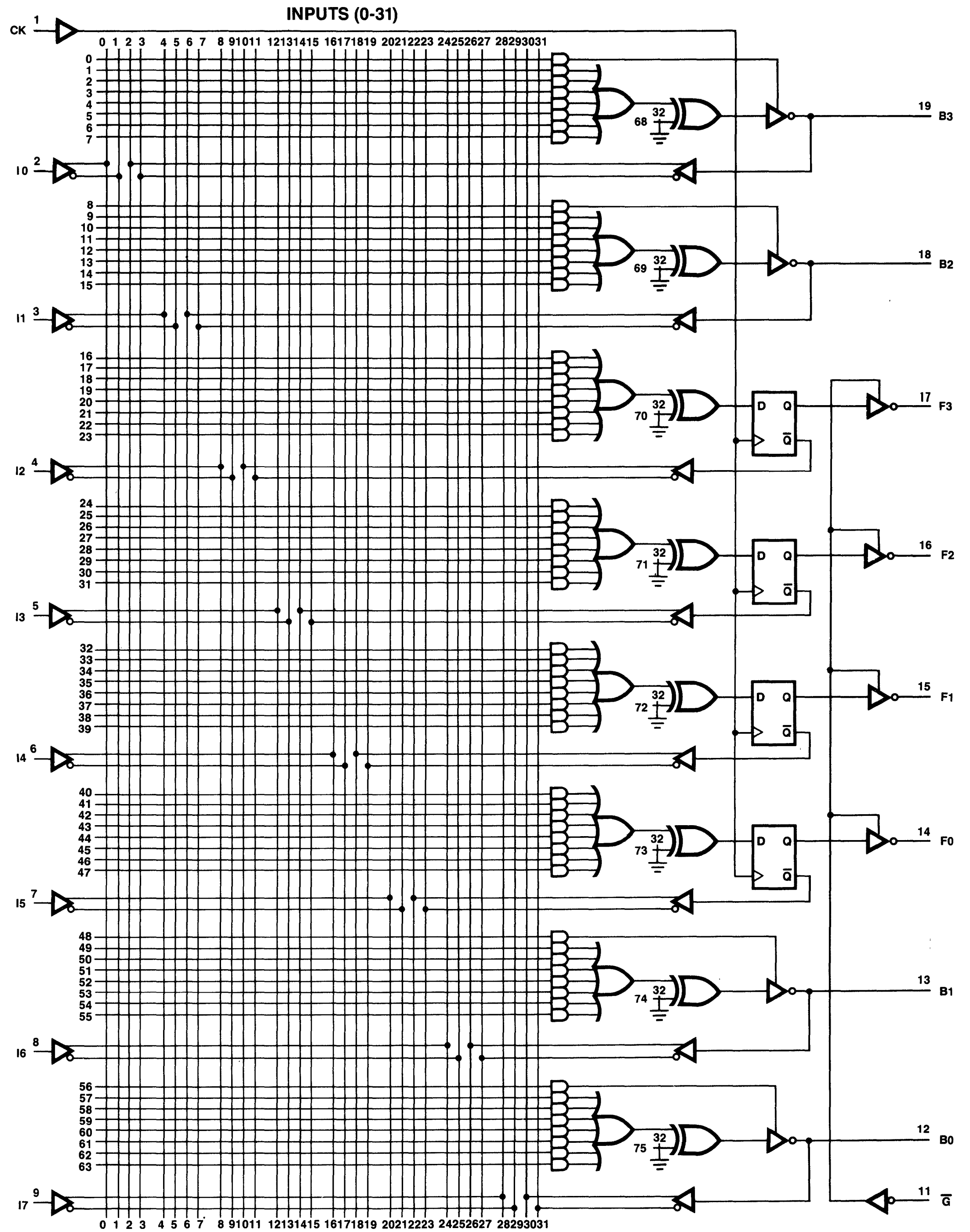
These three devices provide a choice of either eight (16RC8), six (16RC6), or four (16RC4) registered outputs with feedback, each output consisting of eight product terms. The HPL-16RC6 and the HPL-16RC4 also contain two and four bi-directional pins, respectively.

The Harris fuse link technology provides a permanent fuse with stable storage characteristics of the full temperature ranges of 0°C to +75°C, -40°C to +85°C and -55°C to +125°C. Like all Harris Programmable Logic (HPL), these devices contain unique test circuitry developed by Harris which allows AC, DC and functional testing before programming.

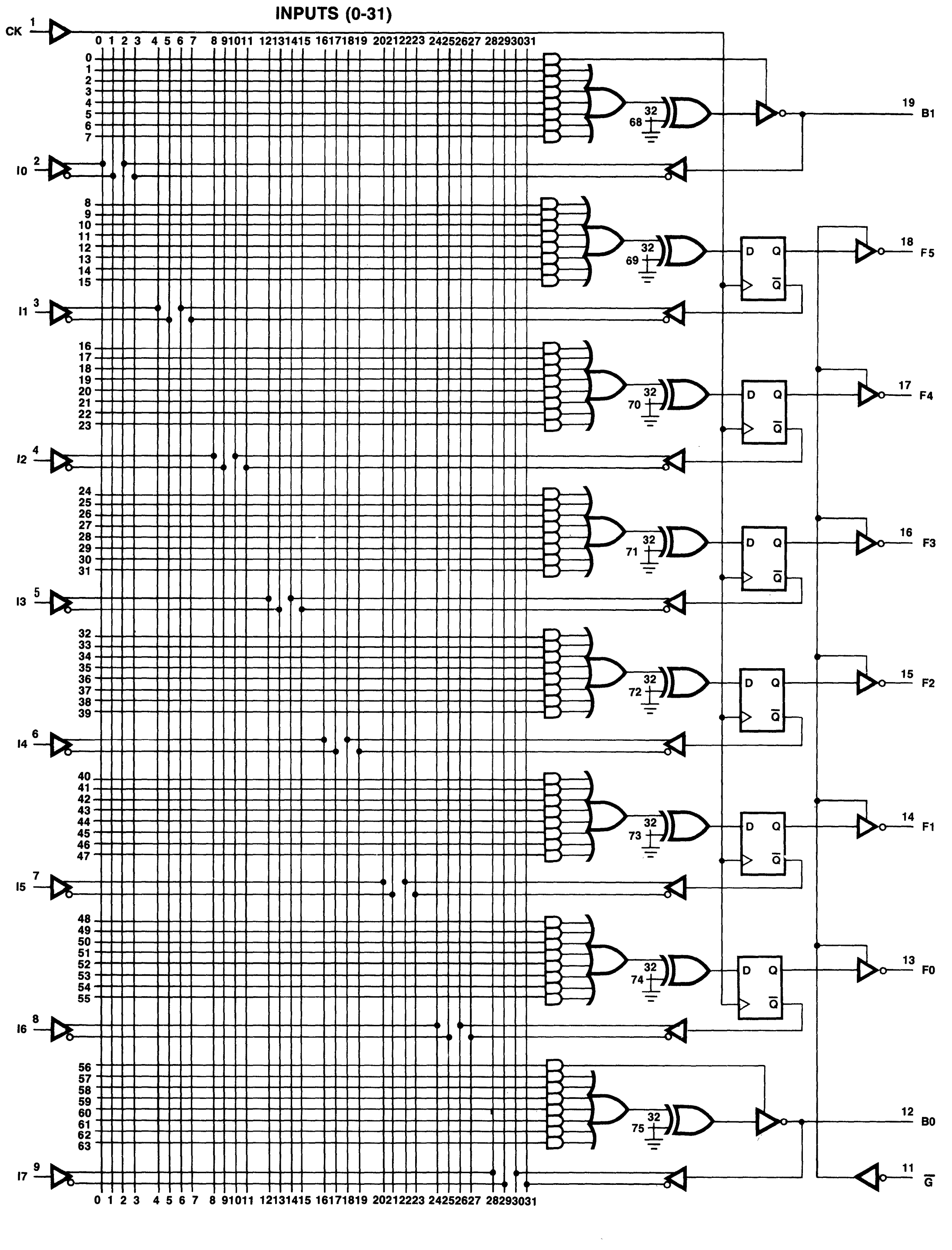
On-chip automatic power-down circuitry places internal circuitry into an ultra-low ICCSB power mode after output data becomes valid.

CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

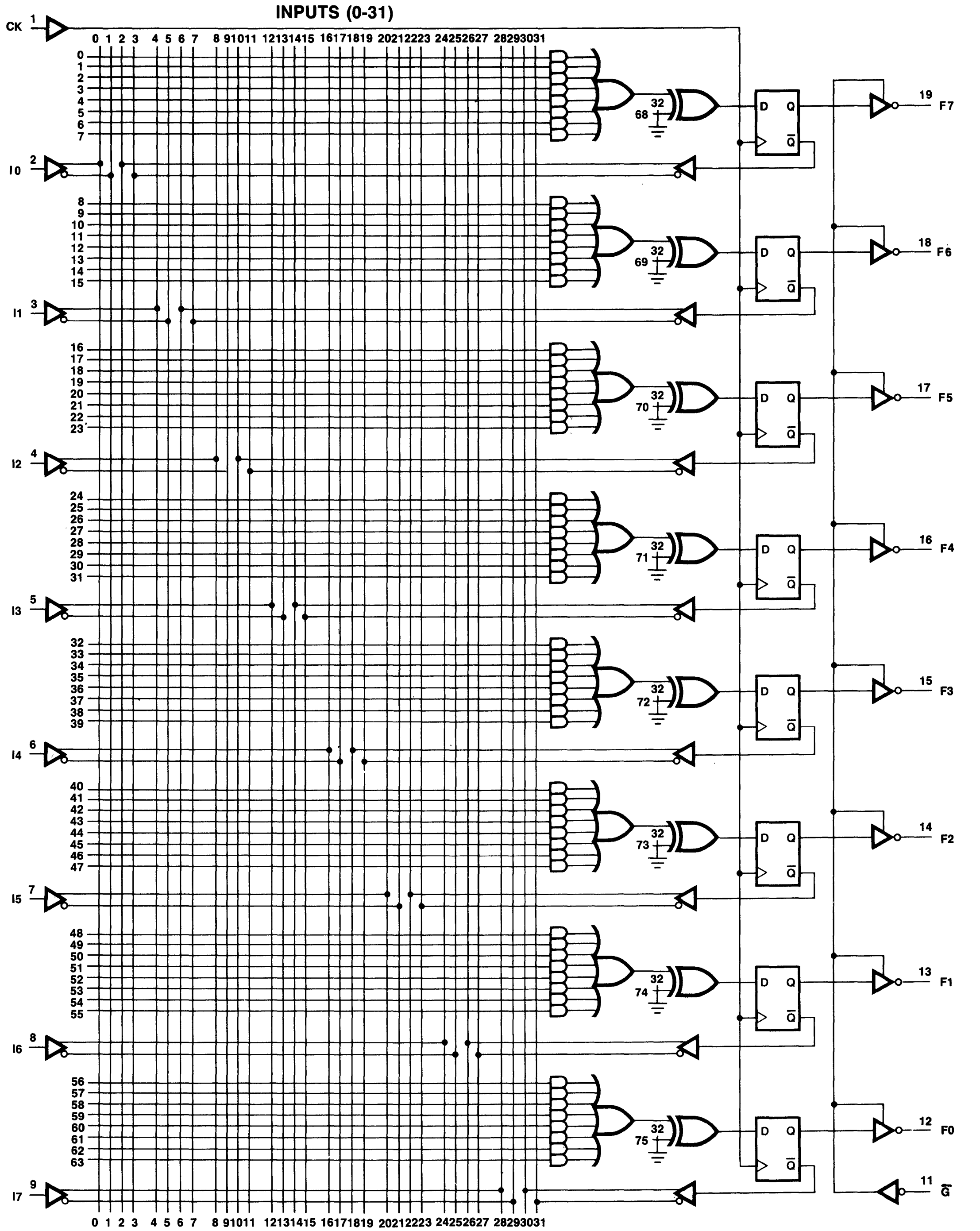
Functional Diagram



Functional Diagram



Functional Diagram



Absolute Maximum Ratings*

Supply Voltage	0.0V to +8.0V
Operating Supply Voltage	+4.0V to +6.0V
Input Voltage	GND −0.5V to VCC +0.5V
Output Voltage	GND −0.5V to VCC +0.5V
Storage Temperature	−65°C to +150°C

Operating Conditions

Operating Temperature (Ambient)

HPL-16RC8,6,4-5	0°C to +75°C
HPL-16RC8,6,4-9	−40°C to +85°C
HPL-16RC8,6,4-2/-8	−55°C to +125°C

*CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. While programming refer to the "Programming Specifications".

D.C. Electrical Specifications

(Operating)

HPL-16RC8,6,4-5 (VCC = 5.0 V ± 10%, TA = 0°C to + 75°C)
HPL-16RC8,6,4-9 (VCC = 5.0 V ± 10%, TA = −40°C to + 85°C)
HPL-16RC8,6,4-2/-8 (VCC = 5.0 V ± 10%, TA = −55°C to + 125°C)

SYMBOL	PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS (3)	
IIH	Dedicated	"1"		+1	μA	VIH = VCC MAX	
IIL	Input Current	"0"		−1	μA	VIL = 0 V	VCC = VCC MAX
IFZH	Output Current	"1"		+10	μA	VFH = VCC MAX	
IFZL	Hi-Z State	"0"		−10	μA	VFL = 0V	VCC = VCC MAX
IBZH	Bidirectional	"1"		+10	μA	VBH = VCC MAX	
IBZL	Hi-Z Current	"0"		−10	μA	VBL = 0V	VCC =VCC MAX
VIH	Input Threshold	"1"	2.0		V	VCC = VCC MAX	
VIL	Voltage (1)	"0"		0.8	V	VCC = VCC MIN	
VOH1	Output Voltage	"1"	3.0		V	IOH1 = −5.0 mA	
VOH2	(2)	"1"	VCC-0.4		V	IOH2 = −1.0 mA VCC MIN, VIL MAX, VIH MIN	
VOL	Output Voltage	"0"		0.4	V	IOL = +5.0 mA	
ICCSB	Standby Power Supply Current			150	μA	VI = VCC or GND IF = 0μA, VCC = VCC MAX	
ICCOP	Operating Power Supply Current			7	mA/MHz	VI = VCC or GND IF = 0μA, VCC = VCC MAX	

(1) These specifications apply to both Input (I) and Bidirectional (B) Pins.
(2) These specifications apply to both Output (F) and Bidirectional (B) Pins.
(3) All DC parameters are tested under worst case conditions.

Capacitance TA = 25°C*

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance	5	pF	VI = VCC or GND, f = 1 MHz
CF	Output Capacitance	10	pF	VF = VCC or GND, f = 1MHz
CB	Bidirectional Capacitance	12	pF	VB = VCC or GND, f = 1 MHz

*NOTE: Sampled and guaranteed – but not 100% tested.

A.C. Switching Specifications (1)

(Operating)

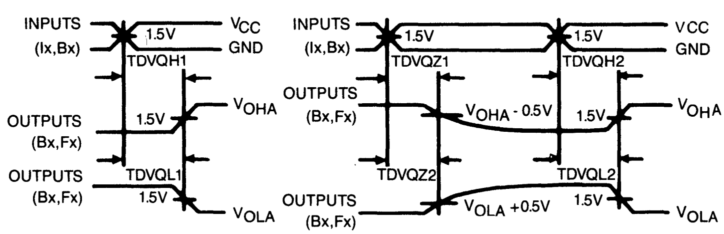
HPL-16RC8,6,4-5 (VCC = 5.0 V ± 10%, TA = 0°C to + 75°C)
HPL-16RC8,6,4-9 (VCC = 5.0 V ± 10%, TA = −40°C to + 85°C)
HPL-16RC8,6,4-2/-8 (VCC = 5.0 V ± 10%, TA = −55°C to +125°C)

SYMBOL			HPL-16RC8,6,4-5		HPL-16RC8,6,4-9		HPL-16RC8,6,4-2/-8		
JEDEC STANDARD	OLD SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
TDVQH1	TPD	Propagation delay Input or I/O to Active High Output	-	125	-	125	-	125	ns
TDVQL1	TPD	Propagation delay Input or I/O to Active Low Output	-	125	-	125	-	125	ns
TDVQH2 (2)	TPZX	Enable Access Time to Active High Output - Product Term Controlled	TDVQZ1	125	TDVQZ1	125	TDVQZ1	125	ns
TDVQL2 (2)	TPZX	Enable Access Time to Active Low Output-Product Term Controlled	TDVQZ2	125	TDVQZ2	125	TDVQZ2	125	ns
TDVQZ1	TPXZ	Disable Access Time from Active High Output-Product Term Controlled	-	125	-	125	-	125	ns
TDVQZ2	TPXZ	Disable Access Time from Active Low Output-Product Term Controlled	-	125	-	125	-	125	ns
TCHQH	TCLK	Propagation delay Clock to Active High	-	60	-	60	-	60	ns
TCHQL	TCLK	Propagation delay Clock to Active Low	-	60	-	60	-	60	ns
TGLQH (2)	TPZX	Enable Access Time to Active High Output - Enable Pin Controlled	TGHQZ1	60	TGHQZ1	60	TGHQZ1	60	ns
TGLQL (2)	TPZX	Enable Access Time to Active Low Output - Enable Pin Controlled	TGHQZ2	60	TGHQZ2	60	TGHQZ2	60	ns
TGHQZ1	TPXZ	Disable Access Time from Active High Output - Enable Pin Controlled	-	60	-	60	-	60	ns
TGHQZ2	TPXZ	Disable Access Time from Active Low Output - Enable Pin Controlled	-	60	-	60	-	60	ns
TDVCH	TSU	Data Setup Time	125	-	125	-	125	-	ns
TCHDX	TH	Data Hold Time	0	-	0	-	0	-	ns
TCHCL	TW	Clock Pulse Width (High)	25	-	25	-	25	-	ns
TCLCH	TW	Clock Pulse Width (Low)	25	-	25	-	25	-	ns
fMAX	fMAX	Maximum Frequency	-	5	-	5	-	5	MHz

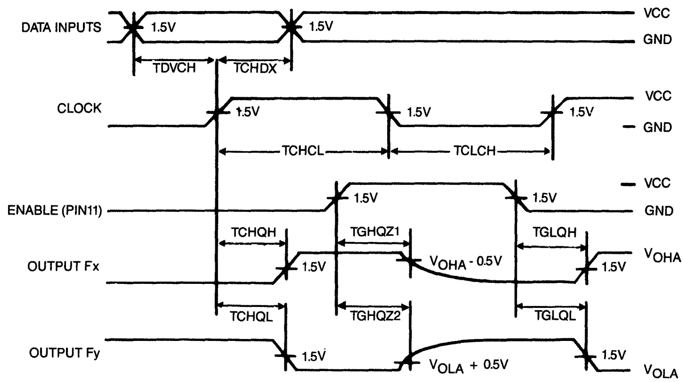
(1) All AC parameters are tested under worst case conditions.
(2) Enable access time is guaranteed to be greater than disable access time to avoid device contention.

Switching Time Definitions

Asynchronous Outputs



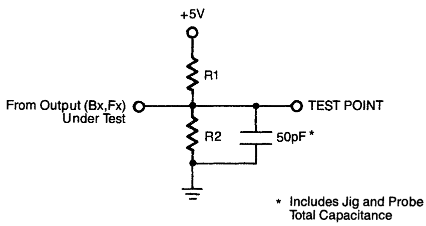
Synchronous Outputs



INPUT CONDITIONS: t_r, t_f = 5ns (10% to 90%)

NOTE: Disable access time is the time taken for the output to reach a high impedance state when the three-state product term or the output enable pin drives the output inactive. The high impedance state is defined as a point on the output waveform equal to a Δ V of 0.5V from VOHA or VOLA, the active output level.

A.C. Test Load



SYMBOL	PARAMETER	TEST LOAD VALUES R1	R2
TDVQH1	Propagation Delay from Input or I/O to Active High Output	∞	∞
TDVQL1	Propagation Delay from Input or I/O to Active Low Output	∞	∞
TDVQH2	Enable Access Time to Active High Output (Product Term Controlled)	∞	920Ω
TDVQL2	Enable Access Time to Active Low Output (Product Term Controlled)	920Ω	∞
TDVQZ1	Disable Access Time from Active High Output (Product Term Controlled)	∞	920Ω
TDVQZ2	Disable Access Time from Active Low Output (Product Term Controlled)	920Ω	∞
TCHQH	Propagation Delay from Clock to Active High Output	∞	∞
TCHQL	Propagation Delay from Clock to Active Low Output	∞	∞
TGLQH	Enable Access Time to Active High Output (Enable Pin Controlled)	∞	920Ω
TGLQL	Enable Access Time to Active Low Output (Enable Pin Controlled)	920Ω	∞
TGHQZ1	Disable Access Time from Active High Output (Enable Pin Controlled)	∞	920Ω
TGHQZ2	Disable Access Time from Active Low Output (Enable Pin Controlled)	920Ω	∞

Programming

Following is the programming procedure used for the HPL-16RC8,6,4 programmable logic devices. These devices are manufactured with all fuses intact. Any desired fuse can be programmed by following the simple procedure shown on the following page. One may build a programmer to satisfy the specifications described in the table, or use any of the commercially available programmers which meets these specifications. Please contact Harris for a list of approved programmers.

TABLE 1
PROGRAMMING SPECIFICATIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
VCCP	VCC Voltage During Programming		11.50	12.00	12.00	V
VCCV	VCC Voltage During Verify		4.75	5.00	5.25	V
ICCP	IC Limit During Programming			100	200	mA
VNEG	Edit Enable & Mode Select Voltage		-5.00	-5.00	-7.00	V
INEG	Edit Enable & Mode Select Current				-5.00	mA
VIL	Input Voltage Low		0.00	0.00	0.80	V
VIHV	Input Voltage High	Verify	(1) VCCV-2	VCCV	VCCV	V
VIHP	Input Voltage High	Programming	(1) VCCP-2	VCCP	VCCP	V
IILP	Input Current Low	VIL = 0.0V		0	1	μA
IIHV	Input Current High	Verify		0	1	μA
IIHP	Input Current High	Programming		0	1	μA
VSI	Verify voltage	Intact Fuse	3.00	3.30		V
VSP	Verify voltage	Programmed Fuse		0.00	0.50	V
TV	Verify Pulse Delay		500	750	1000	μsec
PWP	Programming Width		4.5	5.0	5.5	msec
td	Pulse Seq. Delay		1	1	10	μsec
tr1	Signal Rise Time	10% to 90%	0.01	0.1	1	μsec
tr2	VCC Rise Time	10% to 90%	0.01	0.1	5	μsec
tf1	Signal Fall Time	90% to 10%	0.01	0.1	1	μsec
tf2	VCC Fall Time	90% to 10%	0.01	0.1	5	μsec
tNEG	Mode Select Width		1	1	5	μsec
TPP	Programming Period			5.1		msec
FL	Fuse Attempts/Link		1	1	2	cycles

(1) Inputs defined as logic "1" (VIHV or VIHP) must track the VCC power supply when the supply is raised or lowered. The input levels should never exceed the level on the VCC PIN.

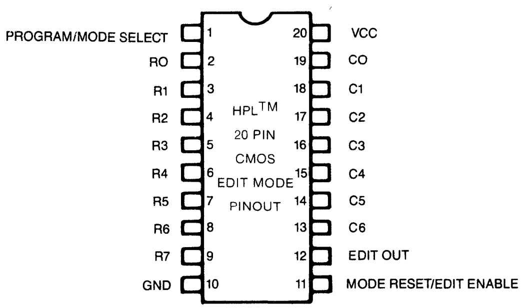


FIGURE 1
EDIT MODE PINOUT
HPL-16RC8,6,4

NOTES:
- While programming the CMOS HPL™ device, no pins should be left floating. EDIT OUT appears as an open drain output during programming. It should be tied to GND through a 1M-ohm resistor.
- CMOS HPL outputs are not put into a high impedance state (suitable for row and column address application) until the device is reset and put into the edit mode. For this reason it is recommended that the outputs be left floating until the edit mode is enabled or that the outputs be driven thru a 2k-ohm resistor.
- It is suggested that a 0.01μF capacitor be put between VCC and GND to minimize VCC voltage spikes. Also, particular care should be exercised in regard to transients on the MODE SELECT and MODE RESET pins, which could place the device in the incorrect mode.

Programming Procedure

1) Set-Up:

NOTE: Refer to the Figure 1 for the pin definitions, Table 1 for the timing and level definitions, Table 2 for the mode decode, and Tables 3 & 4 for the address decoding.

a. During programming, no pins should be left floating.
b. EDIT OUT(Pin 12) should be terminated with a 1 M-ohm (± 1%) resistor to GND and stray capacitances on this pin should be ≤50 pF.
c. Set GND to 0.00 volts.
d. Outputs are only in a high impedance state (and available for addressing of edit mode rows and columns) while in Edit Modes 1 thru 4. Do not apply signals to these pins until a valid Edit Mode is entered.
e. All input and bi-directional pins should be at zero volts nominal with a maximum of 0.3 volts applied.
f. Apply VCCV to the part. No input should ever exceed the level on the VCC PIN.

2) Mode Reset/Edit Enable:

a. Wait td and reset the edit control logic by pulsing the MODE RESET PIN to VNEG for tNEG.
b. Wait td and enable Edit mode by applying VNEG to the EDIT ENABLE PIN.

3) Mode Select:

a. Wait td and select EDIT MODE 1 by pulsing the MODE SELECT PIN to VNEG for tNEG. Subsequent pulses will increment the mode to 2, 3 and 4 sequentially (sequencing the device beyond mode 4 will result in unpredictable results --- if in doubt, return to STEP 2).
b. Verify entry into the proper mode by addressing column 64 and the row indicated in Table 2, waiting TV and monitoring the EDIT OUT PIN for the proper data.
c. Address column 65 and the row indicated in Table 2, wait TV and monitor the EDIT OUT PIN for the proper data. If both steps 3b and 3c are correct, then the proper mode has been selected.
d. To re-enter a mode lower than the current mode, return to step 2. Mode 1 can only be (re-)entered from step 2.

4) Fuse select:

NOTE: The voltage for a logical "1" (VIHP) must not exceed VCCP and must track VCCP as it rises from VCCV in step 5.

a. wait td and select a row by applying the appropriate address from Table 3.
b. Select a column by applying the appropriate address from Table 4.

5) Verify Intact Fuse:

NOTE: Skip this step for post-programming verify.

a. Wait TV and monitor EDIT OUT (Pin 12) for VSI.
b. If EDIT OUT has indicated less than VSI, the fuse is not intact. Reject this device for a non-blank matrix.

6) Program the Fuse:

NOTE: The PROTECT and POLARITY fuses can be accessed from either mode 1 or mode 3 by applying the addresses indicated in Tables 3 & 4.
THE 'PROTECT' FUSE SHOULD NOT BE PROGRAMMED UNTIL ALL OTHER FUSES HAVE BEEN PROGRAMMED AND VERIFIED AS PROGRAMMING THIS FUSE DEFEATS ALL FURTHER VERIFICATION!!

a. Wait td and raise the VCC PIN to VCCP (allow VIHP to track this rise).
b. Wait td and pulse the PROGRAM PIN(Pin 1) to VIHP for a duration of PWP.
c. Wait td and lower the VCC PIN to VCCV (allow VIHP to track this fall)

7) Verify Fuse:

a. Wait TV and monitor EDIT OUT for VSP (or VSI if verifying an intact fuse).
b. If EDIT OUT has indicated greater than VSP for an attempted programmed fuse, repeat step 6 so that the fuse receives a maximum of FL fusing attempts.

8) Repeat steps 4 through 7 for all addresses in a given mode.....

9) Repeat steps 3 through 8 for all modes.

Programming Waveforms

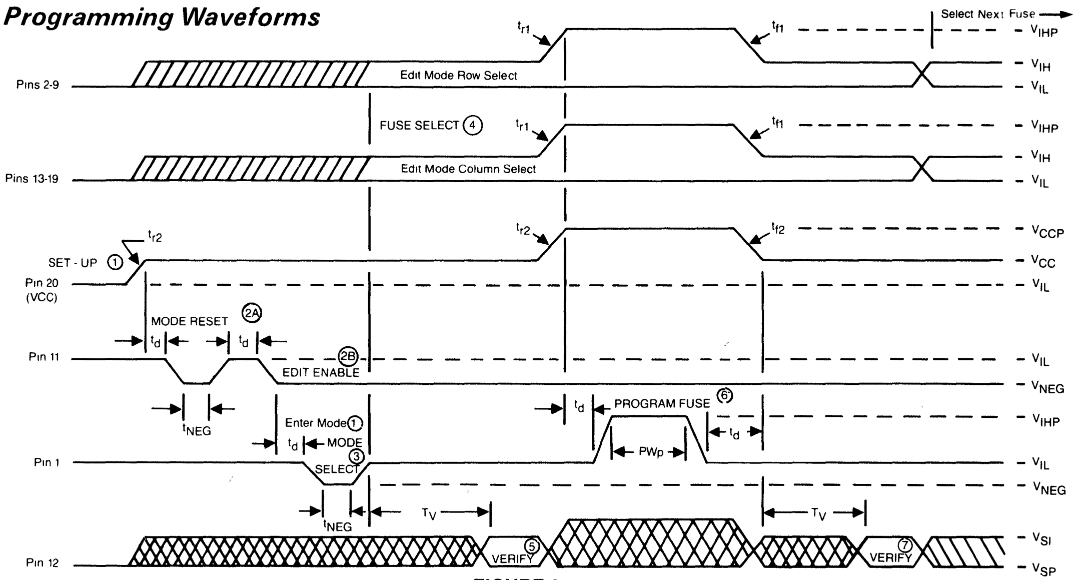


FIGURE 2

NOTE: Pins 13-19 are not necessarily three-stated and available for application of column address input signals until a valid edit mode is entered. Refer to the edit mode pinout (Figure 1) for further details.

MODE VERIFICATION TABLE 2

MODE	COLUMN NUMBER	ROW NUMBER	EDIT OUT(PIN 12) LOGICAL LEVEL
1	64	0	0
	65	0	0
2	64	1	0
	65	1	1
3	64	2	1
	65	2	0
4	64	3	1
	65	3	1

NOTE: *At least two addresses must be checked to verify the proper edit mode.
*The conversion from the decimal column and row addresses in the table above to the actual pin levels can be made in Tables 3 and 4.

EDIT MODE ROW SELECT TABLE 3 HPL-16RC8,6,4

PROG. MODE	ROW NUMBER	R7 Pin 9	R6 Pin 8	R5 Pin 7	R4 Pin 6	R3 Pin 5	R2 Pin 4	R1 Pin 3	R0 Pin 2	VARIABLE 16RC8	16RC6	16RC4
1	0	H	H	H	H	H	H	H	L	I0	I0	I0
	4	H	H	H	H	H	H	L	H	I1	I1	I1
	8	H	H	H	H	H	L	H	H	I2	I2	I2
	12	H	H	H	H	L	H	H	H	I3	I3	I3
	16	H	H	H	L	H	H	H	H	I4	I4	I4
	20	H	H	L	H	H	H	H	H	I5	I5	I5
	24	H	L	H	H	H	H	H	H	I6	I6	I6
	28	L	H	H	H	H	H	H	H	I7	I7	I7
2	1	L	L	L	L	L	L	L	H	/I0	/I0	/I0
	5	L	L	L	L	L	L	H	L	/I1	/I1	/I1
	9	L	L	L	L	L	H	L	L	/I2	/I2	/I2
	13	L	L	L	L	H	L	L	L	/I3	/I3	/I3
	17	L	L	L	H	L	L	L	L	/I4	/I4	/I4
	21	L	L	H	L	L	L	L	L	/I5	/I5	/I5
	25	L	H	L	L	L	L	L	L	/I6	/I6	/I6
	29	H	L	L	L	L	L	L	L	/I7	/I7	/I7
3	2	H	H	H	H	H	H	H	L	F7	B1	B3
	6	H	H	H	H	H	H	L	H	F6	F5	B2
	10	H	H	H	H	H	L	H	H	F5	F4	F3
	14	H	H	H	H	L	H	H	H	F4	F3	F2
	18	H	H	H	L	H	H	H	H	F3	F2	F1
	22	H	H	L	H	H	H	H	H	F2	F1	F0
	26	H	L	H	H	H	H	H	H	F1	F0	B1
	30	L	H	H	H	H	H	H	H	F0	B0	B0
4	3	L	L	L	L	L	L	L	H	/F7	/B1	/B3
	7	L	L	L	L	L	L	H	L	/F6	/F5	/B2
	11	L	L	L	L	L	H	L	L	/F5	/F4	/F3
	15	L	L	L	L	H	L	L	L	/F4	/F3	/F2
	19	L	L	L	H	L	L	L	L	/F3	/F2	/F1
	23	L	L	H	L	L	L	L	L	/F2	/F1	/F0
	27	L	H	L	L	L	L	L	L	/F1	/F0	/B1
	31	H	L	L	L	L	L	L	L	/F0	/B0	/B0
1 or 3	32	H	H	H	H	H	H	H	H	CONFIGURE		

LEGEND: L = Logic Low H = Logic high.

NOTE: The configure row can be selected while in either mode 1 or mode 3.

EDIT MODE COLUMN SELECT TABLE 4

COLUMN NUMBER	C6 Pin 13	C5 Pin 14	C4 Pin 15	C3 Pin 16	C2 Pin 17	C1 Pin 18	C0 Pin 19	
0	L	L	L	L	L	L	L	
1	L	L	L	L	L	L	H	
2	L	L	L	L	L	H	L	
3	L	L	L	L	L	H	H	
4	L	L	L	L	H	L	L	P
5	L	L	L	L	H	L	H	
6	L	L	L	L	H	H	L	
7	L	L	L	L	H	H	H	
8	L	L	L	H	L	L	L	R
9	L	L	L	H	L	L	H	
10	L	L	L	H	L	H	L	
11	L	L	L	H	L	H	H	
12	L	L	L	H	H	L	L	O
13	L	L	L	H	H	L	H	
14	L	L	L	H	H	H	L	
15	L	L	L	H	H	H	H	
16	L	L	H	L	L	L	L	
17	L	L	H	L	L	L	H	D
18	L	L	H	L	L	H	L	
19	L	L	H	L	L	H	H	
20	L	L	H	L	H	L	L	
21	L	L	H	L	H	L	H	U
22	L	L	H	L	H	H	L	
23	L	L	H	L	H	H	H	
24	L	L	H	H	L	L	L	
25	L	L	H	H	L	L	H	
26	L	L	H	H	L	H	L	C
27	L	L	H	H	L	H	H	
28	L	L	H	H	H	L	L	
29	L	L	H	H	H	L	H	
30	L	L	H	H	H	H	L	T
31	L	L	H	H	H	H	H	
32	L	H	L	L	L	L	L	
33	L	H	L	L	L	L	H	
34	L	H	L	L	L	H	L	
35	L	H	L	L	L	H	H	
36	L	H	L	L	H	L	L	
37	L	H	L	L	H	L	H	
38	L	H	L	L	H	H	L	
39	L	H	L	L	H	H	H	T
40	L	H	L	H	L	L	L	
41	L	H	L	H	L	L	H	
42	L	H	L	H	L	H	L	
43	L	H	L	H	L	H	H	
44	L	H	L	H	H	L	L	E
45	L	H	L	H	H	L	H	
46	L	H	L	H	H	H	L	
47	L	H	L	H	H	H	H	
48	L	H	H	L	L	L	L	R
49	L	H	H	L	L	L	H	
50	L	H	H	L	L	H	L	
51	L	H	H	L	L	H	L	
52	L	H	H	L	H	L	L	
53	L	H	H	L	H	L	H	M
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55	L	H	H	L	H	H	H	
56	L	H	H	H	L	L	L	
57	L	H	H	H	L	L	H	S
58	L	H	H	H	L	H	L	
59	L	H	H	H	L	H	H	
60	L	H	H	H	H	L	L	
61	L	H	H	H	H	L	H	
62	L	H	H	H	H	H	L	
63	L	H	H	H	H	H	H	
64	H	L	L	L	L	L	L	MODE
65	H	L	L	L	L	L	H	VERIFY
68	H	L	L	L	H	L	L	Pin 19 P
69	H	L	L	L	H	L	H	Pin 18 O O
70	H	L	L	L	H	H	L	Pin 17 U L
71	H	L	L	L	H	H	H	Pin 16 T A
72	H	L	L	H	L	L	L	Pin 15 P R
73	H	L	L	H	L	L	H	Pin 14 U I
74	H	L	L	H	L	H	L	Pin 13 T T
75	H	L	L	H	L	H	H	Pin 12 Y
76	H	L	L	H	H	L	L	PROTECT

LEGEND: L = Logic Low H = Logic High.

HARRIS HPL-82C339

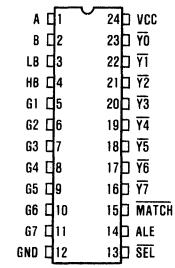
Programmable Chip Select Decoder (PCSD™)

Features

- Memory or I/O Chip Select Decoding, Replaces 3-7 ICs
- Superset of the Industry Standard 74138/74139
- Microprocessor Bus Oriented Interface
- Address "Match" Output Facilitates Bus Arbitration and "Wait-state" Timing Generation
- Harris Advanced Scaled SAJI IV CMOS Process
- Faster than Low-Power Schottky at CMOS Power Consumption
- 24 Pin Slimline DIP
- Wide Operating Temperature Ranges:
  - HPL-82C339-5 ....0°C to +75°C
  - HPL-82C339-9 .... -40°C to +85°C
  - HPL-82C339-2/-8 .... -55°C to +125°C
- Simple Programming Algorithm
- Mask Programmable for Volume Users

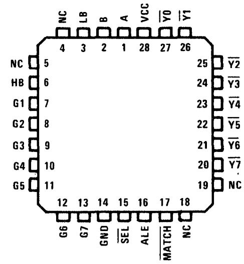
Pinouts

TOP VIEW



LCC

TOP VIEW



Description

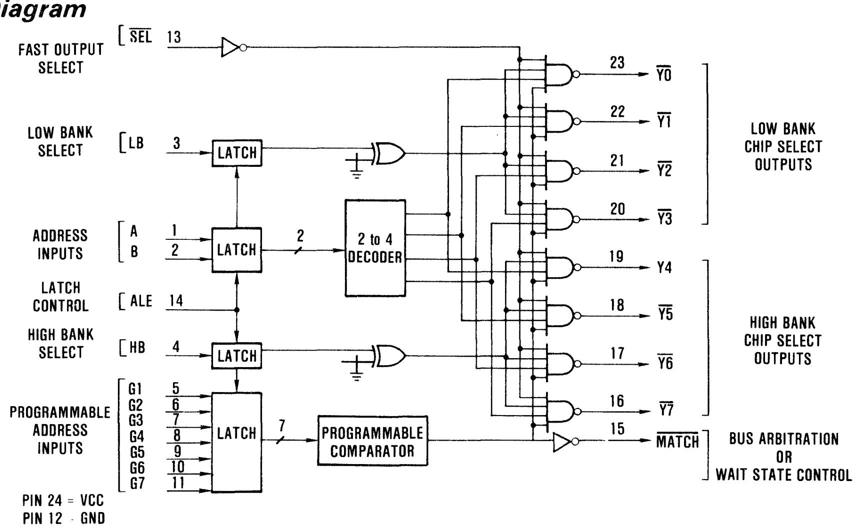
The HPL™-82C339 is a high performance Programmable Chip Select Decoder (PCSD) which is intended to be used for both memory and I/O chip select decoder applications. Utilizing the Harris advanced scaled SAJI IV CMOS process, this circuit provides bipolar speed with CMOS power consumption.

In a typical application, this circuit can replace a 24-pin Programmable Logic Device (PLD) and two octal latches. The associated reductions in board area, chip count and power consumption result in a substantial increase in system reliability and an attendant decrease in system cost.

The seven "Gx" inputs are field programmable for either high or low true address decoding. The High and Low Band (HB, LB) Select inputs are also programmable. This permits the PCSD to be optimized for either 8-bit or 16-bit microprocessor applications. The Harris fuse link technology used in this product provides a permanent fuse with stable storage characteristics over the full temperature ranges of 0°C to +75°C, -40°C to +85°C, and -55°C to +125°C.

Transparent latches are utilized on all address inputs which permits the PCSD to be used with both multiplexed and non-multiplexed address/data bus microprocessors.

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow standard IC Handling Procedures.

HPL, PCSD are trademarks of Harris Corporation.

Absolute Maximum Ratings*

Supply Voltage .... 0.0V to +8.0V
Operating Supply Voltage .... +4.0V to +6.0V
Input Voltage .... GND -0.5V to VCC +0.5V
Output Voltage .... GND -0.5V to VCC +0.5V
Storage Temperature .... -65°C to +150°C

Operating Temperature (Ambient)

HPL-82C339-5 .... 0°C to +75°C
HPL-82C339-9 .... -40°C to +85°C
HPL-82C339-2/-8 .... -55°C to +125°C

** CAUTION: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. While programming refer to the " Programming Specifications."*

D.C. Electrical Specifications

(Operating)

HPL-82C339-5 (VCC = 5.0V ± 10%, TA = 0°C to +75°C)
HPL-82C339-9 (VCC = 5.0V ± 10%, TA = -40°C to +85°C)
HPL-82C339-2/-8 (VCC = 5.0V ± 10%, TA = -55°C to +125°C)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
IIH IIL	Dedicated "1" Input Current "0"		+1 -1	μA μA	VIH = VCC MAX VIL = 0V VCC = VCC MAX
VIH VIL	Input Threshold "1" "1" Voltage "0"	2.0 2.2	 0.8	V V V	VCC = VCC MAX HPL-82C339-5/-9 VCC = VCC MAX HPL-82C339-2/-8 VCC = VCC MIN
VOH1 VOH2 VOL	Output Voltage "1" "1" Output Voltage "0"	3.0 VCC-0.4	 0.4	V V V	IOH1 = -5mA IOH2 = -1mA VCC MIN, VIL MAX, VIH MIN IOL = +5mA
ICCSB*	Standby Power Supply Current		50	μA	VIH = VCC MAX IF = 0.0μA, VCC = VCC MAX
ICCOP*	Operating Power Supply Current		2	mA/MHz	VI = VCC or GND IF = 0.0μA, VCC = VCC MAX

* ICCSB, ICCOP specifications are achieved only after complete programming of the device. These specifications are sampled and guaranteed but not 100% tested. While testing these specifications, output pins should be left open circuit.

A.C. Switching Specifications

(Operating)

HPL-82C339-5 (VCC = 5.0V ± 10%, TA = 0°C to +75°C)
HPL-82C339-9 (VCC = 5.0V ± 10%, TA = -40°C to +85°C)
HPL-82C339-2/-8 (VCC = 5.0V ± 10%, TA = -55°C to +125°C)

SYMBOL	PARAMETER	HPL-82C339-5		HPL-82C339-9		HPL-82C339-2/-8		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
TAVYL	Propagation delay A, B, LB, HB, or G to Output Low	—	50	—	50	—	50	ns
TGVML	Propagation delay G to Match Output Low	—	50	—	50	—	50	ns
TSLYL	Select Access Time to Output Low	—	35	—	35	—	35	ns
TSHYH	Select Access Time to Output High	—	35	—	35	—	35	ns
TGXMH	Match De-Select Propagation Delay	—	50	—	50	—	50	ns
TAVLL	Address Set-Up to ALE Trailing Edge	15	—	15	—	15	—	ns
TLLAX	Address Hold From ALE Trailing Edge	15	—	15	—	15	—	ns
TAVSL	Address Set-Up to SEL Low (Glitch-Free Operation)	15	—	15	—	15	—	ns
TSHAX	Address Hold From SEL High (Glitch-Free Operation)	15	—	15	—	15	—	ns
TLHLL	ALE Pulse Width	15	—	15	—	15	—	ns

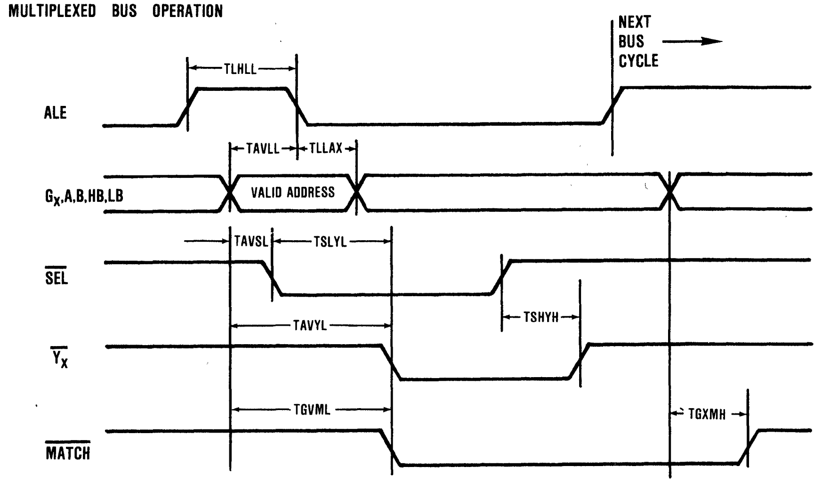
All AC parameters are tested under worst case conditions, with C_L = 50pF.

Capacitance: T_A +25°C (NOTE: Sampled and guaranteed - but not 100% tested.)

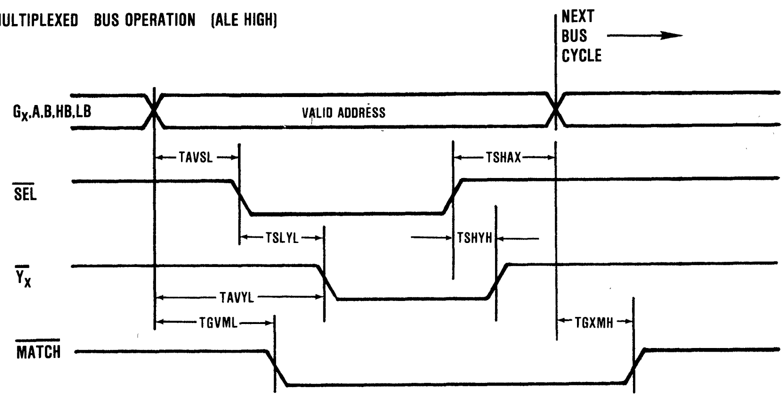
SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance	5	pF	VI = VCC or GND, f = 1 MHz
CO	Output Capacitance	10	pF	VO = VCC or GND, f = 1 MHz

Switching Time Definitions

MULTIPLEXED BUS OPERATION

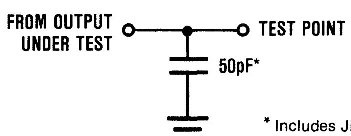


DEMULTIPLEXED BUS OPERATION (ALE HIGH)



NOTES: 1. In order to ensure glitch-free operation of the $\overline{Yx}$ outputs, set-up and hold times should be observed.
2. The $\overline{SEL}$ input controls the $\overline{Yx}$ outputs only and has no effect on the $\overline{MATCH}$ output.
3. AC switching characteristics are measured with inputs switching between GND and 3.0V. t_r, t_f = 5ns (10%–90%).

A.C. Test Load



* Includes Jig and Probe Total Capacitance.

Programming

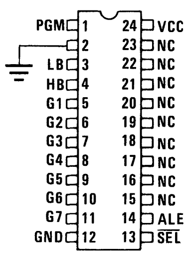
Following is the programming procedure which is used for the HPL-82C339 programmable logic device. This device is manufactured with all fuses intact. Any desired fuse can be programmed by following the simple procedure shown on the following page. One may build a programmer to satisfy the specifications described in the table, or use any of the commercially available programmers which meets these specifications. Please contact Harris for a list of approved programmers.

Programming Specifications

TABLE 1.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
VCCP	VCC Voltage During Programming		11.50	12.00	12.00	V
VCCV	VCC Voltage During Verify		4.75	5.00	5.25	V
ICCP	ICC Limit During Programming		—	100	200	mA
VNEG	Edit Enable & Mode Select Voltage		-6.00	-6.00	-7.00	V
INEG	Edit Enable & Mode Select Current		—	—	-5.00	mA
VIL	Input Voltage Low		0.00	0.00	0.80	V
VIHV	Input Voltage High	verify ①	VCCV-2	VCCV	VCCV	V
VIHP	Input Voltage High	programming ①	VCCP-2	VCCP	VCCP	V
IILP	Input Current Low	VIL = 0.0V	—	0	1	μA
IIHV	Input Current High	verify	—	0	1	μA
IIHP	Input Current High	programming	—	0	1,	μA
PWP	Programming Width		4.5	5.0	5.5	msec
TD	Pulse Seq. Delay		1	1	—	μsec
tr1	Signal Rise Time	10% to 90%	0.01	0.1	1	μsec
tr2	VCC Rise Time	10% to 90%	0.01	0.1	5	μsec
tf1	Signal Fall Time	90% to 10%	0.01	0.1	1	μsec
tf2	VCC Fall Time	90% to 10%	0.01	0.1	5	μsec
TPP	Programming Period		—	5.1	—	msec
FL	Fuse Attempts/Link		1	1	2	cycles

① Inputs defined as logic "1" (VIHV or VIHP) must track the VCC power supply when the supply is raised or lowered. The input levels should never exceed the level on the VCC Pin.



NOTE: While programming the CMOS HPL device, no input pins should be left floating. Output pins (15-23) should be left unconnected. It is suggested that a 0.1μF capacitor be placed between VCC and GND to minimize VCC voltage spikes.

FIGURE 1. HPL-82C339 EDIT MODE PINOUT

Programming Procedure

Set Up:

a. During programming or operation, no input pins should be left floating.

b. No input pin voltage should ever be greater than the voltage applied to the device VCC pin.

c. The device should be decoupled with a 0.1μF or greater capacitor located at the device socket and placed between the VCC and GND pins.

Power up:

a. Initially, all input pins including power supply pins should be at ground potential.

b. Normally, the input pins (pins 3-11, 13, 14) are driven with an open collector driver with a pull-up resistor to the VCC pin (pin 24) so that these inputs automatically track the voltage on the VCC pin when they are set to the high state. This prevents the voltage level on the input pins from exceeding the voltage applied to the VCC pin.

c. Ramp the VCC pin (pin 24) to VCCV and the input pins (pins 3-11, 13, 14) to VIHV.

Programming Sequence

a. After a delay TD, the programming mode is entered by taking the programming enable pin (pin 1) to VNEG. Pin 1 must remain at VNEG throughout the entire programming sequence.

b. Wait TD and raises pin 24 to VCCP and pins 3-11, 14 to VIHP. At the same time, the $\overline{SEL}$ input (pin 13) is set to either VIHP or VIL in order to select the desired polarity of the input which is to be programmed. When $\overline{SEL}$ is at VIHP, the input will be programmed high true. When $\overline{SEL}$ is at VIL, the input will be programmed low true.

c. Wait TD and pulse the input to be programmed to ground for PWP milliseconds. It should be noted that only one input should be programmed at a time.

d. After a delay TD, return pin 24 to VCCV and pins 3-11, 14 to VIHV.

e. Repeat steps b), c), and d) until pins 3-11 have been programmed with the appropriate polarity.

f. When all inputs have been programmed as explained above, wait TD and return the programming enable pin (pin 1) to VIL.

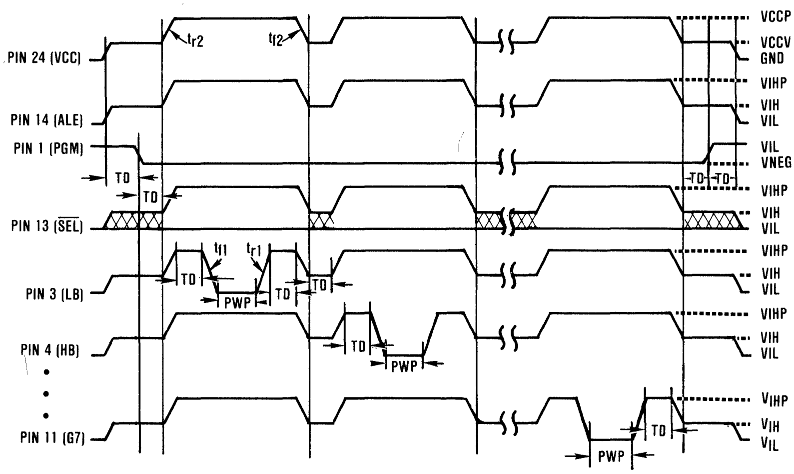
Fuse Integrity Testing

a. Correct programming of the device should be verified by applying test vectors to the input pins.

b. Fuse integrity is tested by applying VCC to the device and measuring the static power consumption of the device. With all inputs at VCC or GND and the output pins unloaded, the measured ICCSB of the device should be less than 50 μA at VCC = 5V and T = 25°C. This guarantees that all fuses have been blown to a final state which is not marginal and will not create a reliability problem over the life of the device. NOTE: Any device which fails this test should be rejected even if it passes functional testing in order to ensure no future reliability problems associated with marginally blown fuses.

IMPORTANT: All nine inputs must be programmed regardless of desired high or low input polarity. The advanced design of the fuse select circuitry (Patent Pending) provides for ultra-low post programming ICCSB and requires that one fuse on each input be programmed.

Programming Waveforms



HPL-82C338

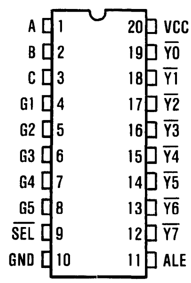
Programmable Chip Select Decoder (PCSD™)

Features

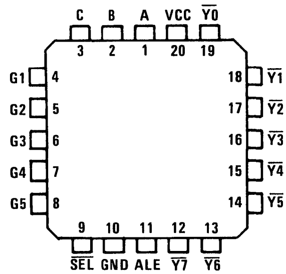
- Memory or I/O Chip Select Decoding, Replaces 3-6 ICs
- Superset of the Industry Standard 74138
- Microprocessor Bus Oriented Interface
- Harris Advanced Scaled SAJI IV CMOS Process
- Faster than Low-Power Schottky at CMOS Power Consumption
- 20 Pin Slimline DIP
- Wide Operating Temperature Ranges:
  - HPL-82C338-5 ....0°C to +75°C
  - HPL-82C338-9 .... -40°C to +85°C
  - HPL-82C338-2/-8 .... -55°C to +125°C
- Simple Programming Algorithm
- Mask Programmable for Volume Users

Pinouts

TOP VIEW



LCC
TOP VIEW



Description

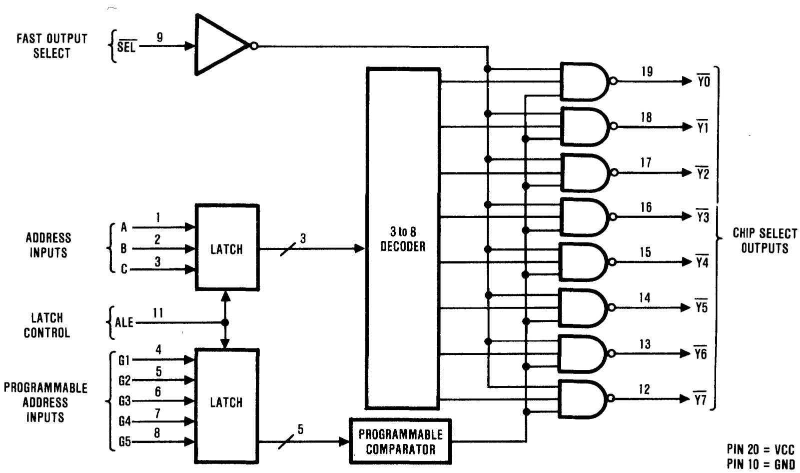
The HPL-82C338 is a high performance Programmable Chip Select Decoder (PCSD) which is intended to be used for both memory and I/O chip select decoder applications. Utilizing the Harris advanced scaled SAJI IV CMOS process, this circuit provides bipolar speed with CMOS power consumption.

In a typical application, this circuit can replace six 74HCXX SSI/MSI ICs. The associated reductions in board area, chip count and power consumption result in a substantial increase in system reliability and an attendant decrease in system cost. A speed improvement of a factor of four over an equivalent implementation with 74HCXX logic is also realized. The faster decode provided by the 82C338 can result in improved system performance or a dramatic reduction in total system cost since less expensive, slower memories and I/O devices can be used.

The five "Gx" inputs are field programmable for either high or low true address decoding. The Harris fuse link technology used in this product provides a permanent fuse with stable storage characteristics over the full temperature ranges of 0°C to +75°C, -40°C to +85°C and -55°C to +125°C.

Transparent latches are utilized on all address inputs which permits the 82C338 to be used with both multiplexed and non-multiplexed address/data bus microprocessors.

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow standard IC Handling Procedures.

HPL, PCSD are trademarks of Harris Corporation

Absolute Maximum Ratings*

Supply Voltage .... 0.0V to +8.0V
Operating Supply Voltage .... +4.0V to +6.0V
Input Voltage .... GND -0.5V to VCC +0.5V
Output Voltage .... GND -0.5V to VCC +0.5V
Storage Temperature .... -65°C to +150°C

Operating Temperature (Ambient)

HPL-82C338-5 .... 0°C to +75°C
HPL-82C338-9 .... -40°C to +85°C
HPL-82C338-2/-8 .... -55°C to +125°C

** CAUTION: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. While programming refer to the " Programming Specifications."*

D.C. Electrical Specifications

(Operating)

HPL-82C338-5 (VCC = 5.0V ± 10%, TA = 0°C to +75°C)
HPL-82C338-9 (VCC = 5.0V ± 10%, TA = -40°C to +85°C)
HP-82C338-2/-8 (VCC = 5.0V ± 10%, TA = -55°C to +125°C)

SYMBOL	PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS
IIH IIL	Dedicated Input Current	"1" "0"		+1 -1	μA μA	VIH = VCC MAX VIL = 0V VCC = VCC MAX
VIH VIL	Input Threshold Voltage	"1" "1" "0"	2.0 2.2	 0.8	V V V	VCC = VCC MAX HPL-82C338-5/-9 VCC = VCC MAX HPL-82C338-2/-8 VCC = VCC MIN
VOH1 VOH2 VOL	Output Voltage Output Voltage	"1" "1" "0"	3.0 VCC-0.4	 0.4	V V V	IOH1 = -5mA IOH2 = -1mA VCC MIN, VIL MAX, VIH MIN IOL = +5mA
ICCSB*	Standby Power Supply Current			50	μA	VIH = VCC MAX IF = 0.0μA, VCC = VCC MAX
ICCOP*	Operating Power Supply Current			2	mA/MHz	VI = VCC or GND IF = 0.0μA, VCC = VCC MAX

* ICCSB, ICCOP specifications are achieved only after complete programming of the device. These specifications are sampled and guaranteed but not 100% tested. While testing these specifications, output pins should be left open circuit.

A.C. Switching Specifications

(Operating)

HPL-82C338-5 (VCC = 5.0V ± 10%, TA = 0°C to +75°C)
HPL-82C338-9 (VCC = 5.0V ± 10%, TA = -40°C to +85°C)
HPL-82C338-2/-8 (VCC = 5.0V ± 10%, TA = -55°C to +125°C)

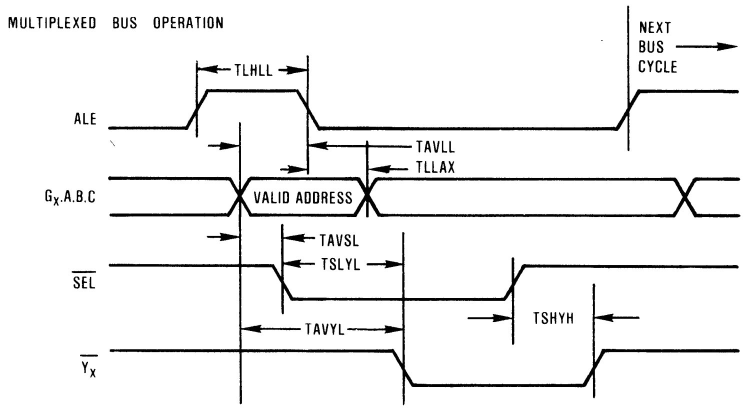
SYMBOL	PARAMETER	HPL-82C338-5		HPL-82C338-9		HPL-82C338-2/-8		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
TAVYL	Propagation delay A, B, C, or G to Output Low	—	50	—	50	—	50	ns
TSLYL	Select Access Time to Output Low	—	35	—	35	—	35	ns
TSHYH	Select Access Time to Output High	—	35	—	35	—	35	ns
TAVLL	Address Set-Up to ALE Trailing Edge	15	—	15	—	15	—	ns
TLLAX	Address Hold From ALE Trailing Edge	15	—	15	—	15	—	ns
TAVSL	Address Set-Up to SEL Low (Glitch-Free Operation)	15	—	15	—	15	—	ns
TSHAX	Address Hold From SEL High (Glitch-Free Operation)	15	—	15	—	15	—	ns
TLHLL	ALE Pulse Width	15	—	15	—	15	—	ns

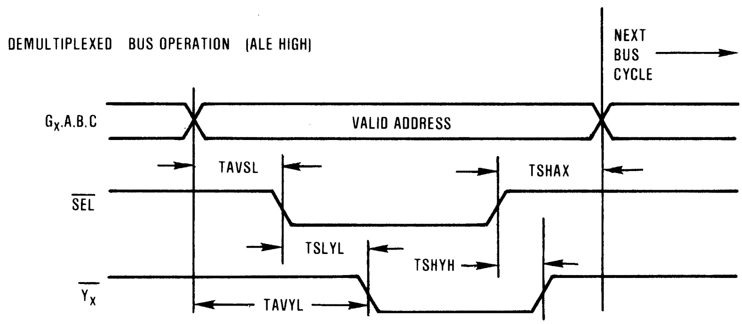
*All AC parameters are tested under worst case conditions, with C_L = 50pF

Capacitance T_A = +25°C (NOTE: Sampled and guaranteed - but not 100% tested.)

SYMBOL	PARAMETER	TYP	UNITS	TEST CONDITIONS
CI	Input Capacitance	5	pF	VI = VCC or GND, f = 1 MHz
CO	Output Capacitance	10	pF	VO = VCC or GND, f = 1 MHz

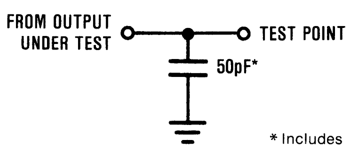
Switching Time Definitions





NOTES: 1. In order to ensure glitch-free operation of the $\overline{Yx}$ outputs, set-up and hold times should be observed.
2. AC switching characteristics are measured with inputs switching between GND and 3.0V. t_r, t_f = 5ns (10% -90%).

A.C. Test Load



* Includes Jig and Probe Total Capacitance.

Programming

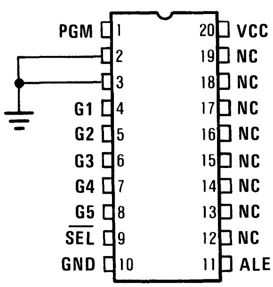
Following is the programming procedure which is used for the HPL-82C338 programmable logic device. This device is manufactured with all fuses intact. Any desired fuse can be programmed by following the simple procedure shown on the following page. One may build a programmer to satisfy the specifications described in the table, or use any of the commercially available programmers which meets these specifications. Please contact Harris for a list of approved programmers.

Programming Specifications

TABLE 1.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNITS
VCCP	VCC Voltage During Programming		11.50	12.00	12.00	V
VCCV	VCC Voltage During Verify		4.75	5.00	5.25	V
ICCP	ICC Limit During Programming		—	100	200	mA
VNEG	Edit Enable & Mode Select Voltage		-6.00	-6.00	-7.00	V
INEG	Edit Enable & Mode Select Current		—	—	-5.00	mA
VIL	Input Voltage Low		0.00	0.00	0.80	V
VIHV	Input Voltage High	verify ①	VCCV-2	VCCV	VCCV	V
VIHP	Input Voltage High	programming ①	VCCP-2	VCCP	VCCP	V
IILP	Input Current Low	VIL = 0.0V	—	0	1	μA
IIHV	Input Current High	verify	—	0	1	μA
IIHP	Input Current High	programming	—	0	1	μA
PWP	Programming Width		4.5	5.0	5.5	msec
TD	Pulse Seq. Delay		1	1	—	μsec
tr1	Signal Rise Time	10% to 90%	0.01	0.1	1	μsec
tr2	VCC Rise Time	10% to 90%	0.01	0.1	5	μsec
tf1	Signal Fall Time	90% to 10%	0.01	0.1	1	μsec
tf2	VCC Fall Time	90% to 10%	0.01	0.1	5	μsec
TPP	Programming Period		—	5.1	—	msec
FL	Fuse Attempts/Link		1	1	2	cycles

① Inputs defined as logic "1" (VIHV or VIHP) must track the VCC power supply when the supply is raised or lowered. The input levels should never exceed the level on the VCC Pin.



NOTE: While programming the CMOS HPL device, no input pins should be left floating. Output pins (12-19) should be left unconnected. It is suggested that a 0.1μF capacitor be placed between VCC and GND to minimize VCC voltage spikes.

FIGURE 1. HPL-82C338 EDIT MODE PINOUT

Programming Procedure

1. Set Up:

a. During programming or operation, no input pins should be left floating.

b. No input pin voltage should ever be greater than the voltage applied to the device VCC pin.

c. The device should be decoupled with a 0.1μF or greater capacitor located at the device socket and placed between the VCC and GND pins.

2. Power up:

a. Initially, all input pins including power supply pins should be at ground potential.

b. Normally, the input pins (pins 4-9, 11) are driven with an open collector driver with a pull-up resistor to the VCC pin (pin 20) so that these inputs automatically track the voltage on the VCC pin when they are set to the high state. This prevents the voltage level on the input pins from exceeding the voltage applied to the VCC pin.

c. Ramp the VCC pin (pin 20) to VCCV and the input pins (pins 4-9, 11) to VIHV.

3. Programming Sequence

a. After a delay TD, the programming mode is entered by taking the programming enable pin (pin 1) to VNEG. Pin 1 must remain at VNEG throughout the entire programming sequence.

b. Wait TD and raises pin 20 to VCCP and pins 4-8, 11 to VIHP. At the same time, the $\overline{\text{SEL}}$ input (pin 9) is set to either VIHP or VIL in order to select the desired polarity of the input which is to be programmed. When $\overline{\text{SEL}}$ is at VIHP, the input will be programmed high true. When $\overline{\text{SEL}}$ is at VIL, the input will be programmed low true.

c. Wait TD and pulse the input to be programmed to ground for PWP milliseconds. It should be noted that only one input should be programmed at a time.

d. After a delay TD, return pin 20 to VCCV and pins 4-8, 11 to VIHV.

e. Repeat steps b), c), and d) until pins 4-8 have been programmed with the appropriate polarity.

f. When all inputs have been programmed as explained above, wait TD and return the programming enable pin (pin 1) to VIL.

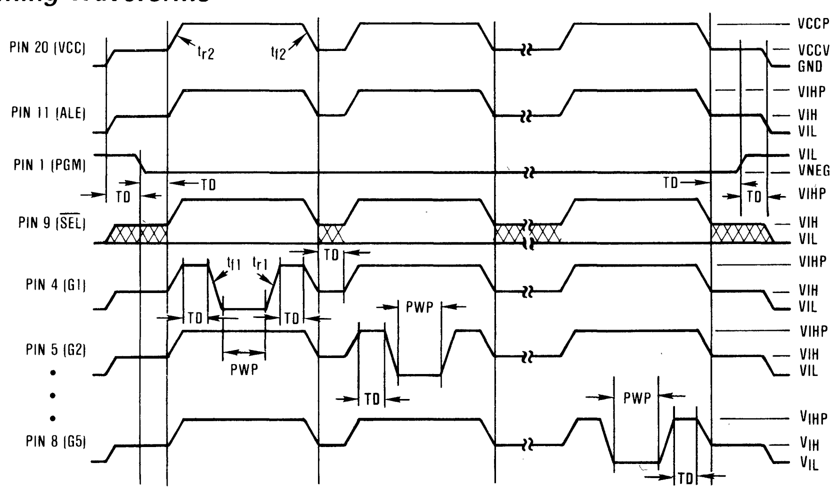
4. Fuse Integrity Testing

a. Correct programming of the device should be verified by applying test vectors to the input pins.

b. Fuse integrity is tested by applying VCC to the device and measuring the static power consumption of the device. With all inputs at VCC or GND and the output pins unloaded, the measured ICCSB of the device should be less than 50 μA at VCC = 5V and T = 25°C. This guarantees that all fuses have been blown to a final state which is not marginal and will not create a reliability problem over the life of the device. NOTE: Any device which fails this test should be rejected even if it passes functional testing in order to ensure no future reliability problems associated with marginally blown fuses.

IMPORTANT: All five inputs must be programmed regardless of desired high or low input polarity. The advanced design of the fuse select circuitry (Patent Pending) provides for ultra-low post programming ICCSB and requires that one fuse on each input be programmed.

Programming Waveforms



HARRIS HPL™-82C139

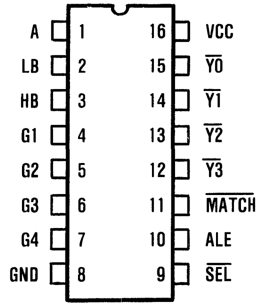
Programmable Chip Select Decoder (PCSD™)

Features

- Memory or I/O Chip Select Decoding, Replaces 2-3 ICs
- Similar to Industry Standard 74139
- Architecture Optimized for "Bootstrap Decoding"
- Microprocessor Bus Oriented Interface
- Harris Advanced Scaled SAJI IV CMOS Process
- Faster than Low-Power Schottky at CMOS Power Consumption
- 16-Pin Ceramic Dual-in-Line Package
- Wide Temperature Ranges: (0°C to +75°C)
  (-40°C to +85°C)
  (-55°C to +125°C)
- Simple Programming Algorithm
- Mask Programmable for Volume Users

Pinout

TOP VIEW



Description

The HPL-82C139 is a high performance Programmable Chip Select Decoder (PCSD) which is intended to be used for both memory and I/O chip select decoder applications. Utilizing the Harris advanced scaled SAJI IV CMOS process, this circuit provides bipolar speed with CMOS power consumption.

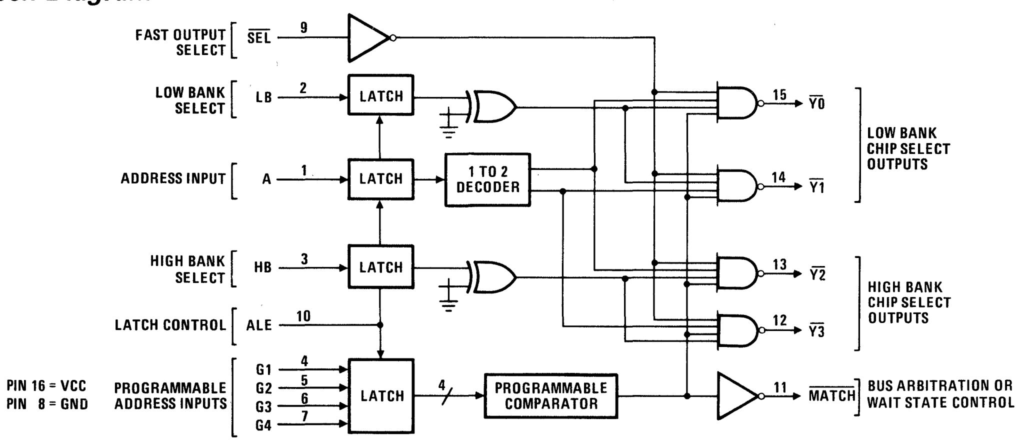
In a typical application, this circuit can replace two to three 74HCXX SSI/MSI ICs. The associated reductions in board area, chip count and power consumption result in a substantial increase in system reliability and an attendant decrease in system cost. A speed improvement of a factor of three to four over an equivalent implementation with 74HCXX logic is also realized. The fast decode provided by the 82C139 can result in improved system performance or a dramatic reduction in total system cost since less expensive, slower memories and I/O devices can be used.

The HPL-82C139 is ideal for 16-bit microprocessor applications as a "bootstrap" PROM decoder or other memory and I/O decoder applications where four or fewer devices require selection within a section of address space.

The four "GX" inputs are field programmable for either high or low true address decoding. The Harris fuse link technology used in this product provides a permanent fuse with stable storage characteristics over the full temperature ranges of 0° to +75°C, -40°C to +85°C, and -55°C to +125°C.

Transparent latches are utilized on all address inputs which permits the 82C139 to be used with both multiplexed and non-multiplexed address/data bus microprocessors.

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow standard IC Handling Procedures.

HPL, PCSD are Trademarks of Harris Corporation

Absolute Maximum Ratings*

Supply Voltage .... 0.0V to +8.0V
Operating Supply Voltage .... +4.0V to +6.0V
Input Voltage .... GND -0.5V to VCC +0.5V
Output Voltage .... GND -0.5V to VCC +0.5V
Storage Temperature .... -65°C to +150°C

Operating Temperature (Ambient)

HPL-82C139-5 .... 0°C to +75°C
HPL-82C139-9 .... -40°C to +85°C
HPL-82C139-2/-8 .... -55°C to +125°C

** CAUTION: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. While programming refer to the " Programming Specifications."*

D.C. Electrical Specifications

(Operating)

HPL-82C139-5 (VCC = 5.0V ± 10%, TA = 0°C to +75°C)
HPL-82C139-9 (VCC = 5.0V ± 10%, TA = -40°C to +85°C)
HPL-82C139-2/-8 (VCC = 5.0V ± 10%, TA = -55°C to +125°C)

SYMBOL	PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS
IIH	Dedicated	"1"		+1	μA	VIH = VCC MAX
IIL	Input Current	"0"		-1	μA	VIL = 0V, VCC = VCC MAX
VIH	Input Threshold	"1"	2.0		V	VCC = VCC MAX HPL-82C139-5/-9
		"1"	2.2		V	VCC = VCC MAX HPL-82C139-2/-8
VIL	Voltage	"0"		0.8	V	VCC = VCC MIN
VOH1	Output Voltage	"1"	3.0		V	IOH1 = -5mA
VOH2		"1"	VCC-0.4		V	IOH2 = -1mA
						VCC MIN, VIL MAX, VIH MIN
VOL	Output Voltage	"0"		0.4	V	IOL = +5mA
ICCSB*	Standby Power Supply Current			50	μA	VIH = VCC MAX IF = 0.0μA, VCC = VCC MAX
ICCOP*	Operating Power Supply Current			2	mA/MHz	VI = VCC or GND IF = 0.0μA, VCC = VCC MAX

* ICCSB, ICCOP specifications are achieved only after complete programming of the device. These specifications are sampled and guaranteed but not 100% tested. While testing these specifications, output pins should be left open circuit.

A.C. Switching Specifications

(Operating)

HPL-82C139-5 (VCC = 5.0V ± 10%, TA = 0°C to +75°C)
HPL-82C139-9 (VCC = 5.0V ± 10%, TA = -40°C to +85°C)
HPL-82C139-2/-8 (VCC = 5.0V ± 10%, TA = -55°C to +125°C)

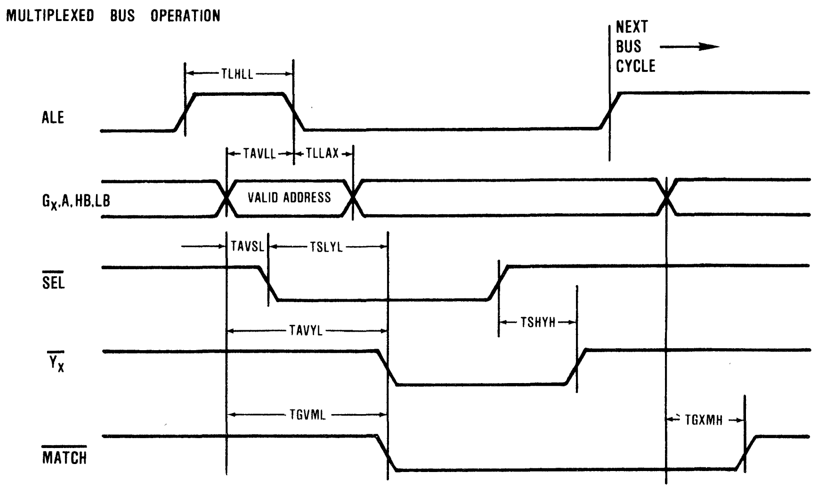
SYMBOL	PARAMETER	HPL-82C139-5		HPL-82C139-9		HPL-82C139-2/-8		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
TAVYL	Propagation delay A, LB, HB, or G to Output Low	—	50	—	50	—	50	ns
TGVML	Propagation delay G to Match Output Low	—	50	—	50	—	50	ns
TSLYL	Select Access Time to Output Low	—	35	—	35	—	35	ns
TSHYH	Select Access Time to Output High	—	35	—	35	—	35	ns
TGXMH	Match De-Select Propagation Delay	—	50	—	50	—	50	ns
TAVLL	Address Set-Up to ALE Trailing Edge	15	—	15	—	15	—	ns
TLLAX	Address Hold From ALE Trailing Edge	15	—	15	—	15	—	ns
TAVSL	Address Set-Up to SEL Low (Glitch-Free Operation)	15	—	15	—	15	—	ns
TSHAX	Address Hold From SEL High (Glitch-Free Operation)	15	—	15	—	15	—	ns
TLHLL	ALE Pulse Width	15	—	15	—	15	—	ns

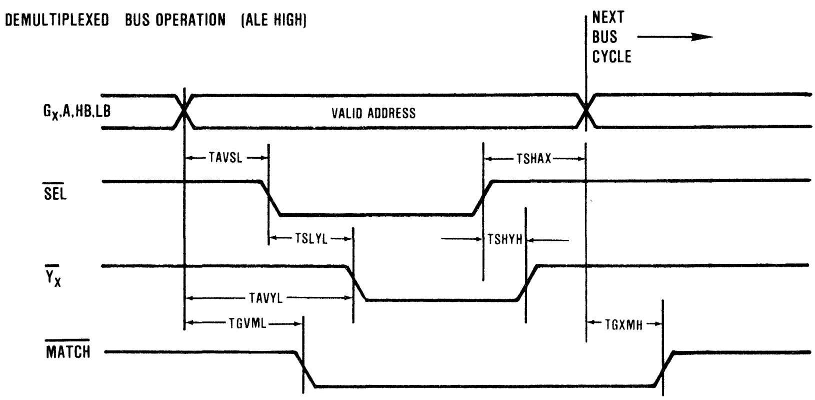
All AC parameters are tested under worst case conditions, with C_L = 50pF.

Capacitance T_A = + 25°C (NOTE: Sampled and guaranteed - but not 100% tested.)

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance	5	pF	VI = VCC or GND, f = 1 MHz
CO	Output Capacitance	10	pF	VO = VCC or GND, f = 1 MHz

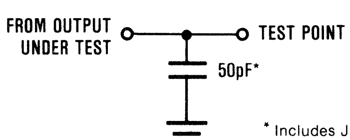
Switching Time Definitions





NOTES
1. In order to ensure glitch-free operation of the $\overline{Yx}$ outputs, set-up and hold times should be observed.
2. The $\overline{SEL}$ input controls the $\overline{Yx}$ outputs only and has no effect on the $\overline{MATCH}$ output
3. AC switching characteristics are measured with inputs switching between GND and 3.0V t_r, t_f 5ns (10%–90%).

A.C. Test Load



* Includes Jig and Probe Total Capacitance.

Programming

Following is the programming procedure which is used for the HPL-82C139 programmable logic device. This device is manufactured with all fuses intact. Any desired fuse can be programmed by following the simple procedure shown on the following page. One may build a programmer to satisfy the specifications described in the table, or use any of the commercially available programmers which meets these specifications. Please contact Harris for a list of approved programmers.

Programming Specifications

TABLE 1.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNITS
VCCP	VCC Voltage During Programming		11.50	12.00	12.00	V
VCCV	VCC Voltage During Verify		4.75	5.00	5.25	V
ICCP	ICC Limit During Programming		—	100	200	mA
VNEG	Edit Enable & Mode Select Voltage		-6.00	-6.00	-7.00	V
INEG	Edit Enable & Mode Select Current		—	—	-5.00	mA
VIL	Input Voltage Low		0.00	0.00	0.80	V
VIHV	Input Voltage High	verify ①	VCCV-2	VCCV	VCCV	V
VIHP	Input Voltage High	programming ①	VCCP-2	VCCP	VCCP	V
IILP	Input Current Low	VIL = 0.0V	—	0	1	μA
IIHV	Input Current High	verify	—	0	1	μA
IIHP	Input Current High	programming	—	0	1	μA
PWP	Programming Width		4.5	5.0	5.5	msec
TD	Pulse Seq. Delay		1	1	—	μsec
tr1	Signal Rise Time	10% to 90%	0.01	0.1	1	μsec
tr2	VCC Rise Time	10% to 90%	0.01	0.1	5	μsec
tf1	Signal Fall Time	90% to 10%	0.01	0.1	1	μsec
tf2	VCC Fall Time	90% to 10%	0.01	0.1	5	μsec
TPP	Programming Period		—	5.1	—	msec
FL	Fuse Attempts/Link		1	1	2	cycles

① Inputs defined as logic "1" (VIHV or VIHP) must track the VCC power supply when the supply is raised or lowered. The input levels should never exceed the level on the VCC Pin.

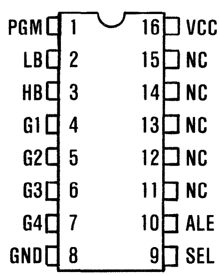


FIGURE 1. HPL-82C139 EDIT MODE PINOUT

NOTE: While programming the CMOS HPL device, no input pins should be left floating. Output pins (11-15) should be left unconnected. It is suggested that a 0.1μF capacitor be placed between VCC and GND to minimize VCC voltage spikes.

Programming Procedure

Set Up:

a. During programming or operation, no input pins should be left floating.

b. No input pin voltage should ever be greater than the voltage applied to the device VCC pin.

c. The device should be decoupled with a 0.1μF or greater capacitor located at the device socket and placed between the VCC and GND pins.

Power up:

a. Initially, all input pins including power supply pins should be at ground potential.

b. Normally, the input pins (pins 2-7, 9, 10) are driven with an open collector driver with a pull-up resistor to the VCC pin (pin 16) so that these inputs automatically track the voltage on the VCC pin when they are set to the high state. This prevents the voltage level on the input pins from exceeding the voltage applied to the VCC pin.

c. Ramp the VCC pin (pin 16) to VCCV and the input pins (pins 2-7, 9, 10) to VIHV.

Programming Sequence

a. After a delay TD, the programming mode is entered by taking the programming enable pin (pin 1) to VNEG. Pin 1 must remain at VNEG throughout the entire programming sequence.

b. Wait TD and raise pin 16 to VCCP and pins 2-7, 10 to VIHP. At the same time, the SEL input (pin 9) is set to either VIHP or VIL in order to select the desired polarity of the input which is to be programmed. When SEL is at VIHP, the input will be programmed high true. When SEL is at VIL, the input will be programmed low true.

c. Wait TD and pulse the input to be programmed to ground for PWP milliseconds. It should be noted that only one input should be programmed at a time.

d. After a delay TD, return pin 16 to VCCV and pins 2-7, 10 to VIHV.

e. Repeat steps b), c), and d) until pins 2-7 have been programmed with the appropriate polarity.

f. When all inputs have been programmed as explained above, wait TD and return the programming enable pin (pin 1) to VIL.

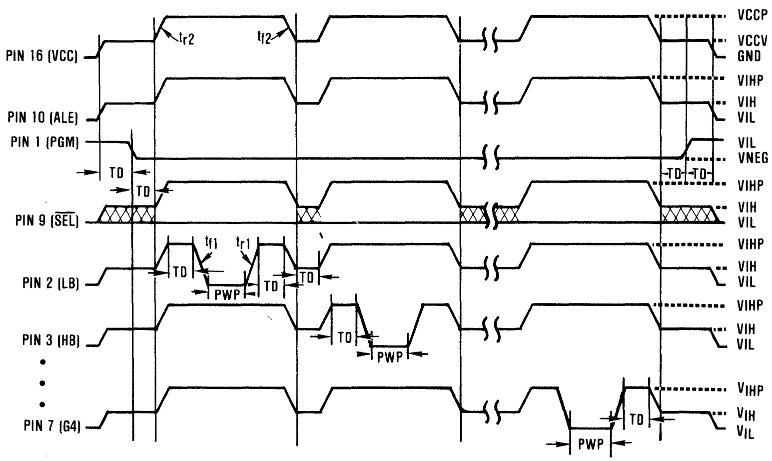
Fuse Integrity Testing

a. Correct programming of the device should be verified by applying test vectors to the input pins.

b. Fuse integrity is tested by applying VCC to the device and measuring the static power consumption of the device. With all inputs at VCC or GND and the output pins unloaded, the measured ICCSB of the device should be less than 50 μA at VCC = 5V and T = 25°C. This guarantees that all fuses have been blown to a final state which is not marginal and will not create a reliability problem over the life of the device. NOTE: Any device which fails this test should be rejected even if it passes functional testing in order to ensure no future reliability problems associated with marginally blown fuses.

IMPORTANT: All six inputs must be programmed regardless of desired high or low input polarity. The advanced design of the fuse select circuitry (Patent Pending) provides for ultra-low post programming ICCSB and requires that one fuse on each input be programmed.

Programming Waveforms



HARRIS HPL™-82C138

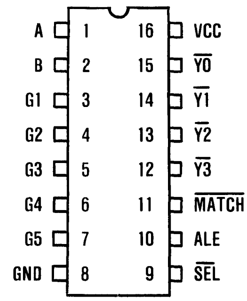
Programmable Chip Select Decoder (PCSD™)

Features

- Memory or I/O Chip Select Decoding, Replaces 2-3 ICs
- Similar to Industry Standard 74138
- Architecture Optimized for "Bootstrap Decoding"
- Microprocessor Bus Oriented Interface
- Harris Advanced Scaled SAJI IV CMOS Process
- Faster than Low-Power Schottky at CMOS Power Consumption
- 16-Pin Ceramic Dual-in-Line Package
- Wide Temperature Ranges: (0°C to +75°C) (-40°C to +85°C) (-55°C to +125°C)
- Simple Programming Algorithm
- Mask Programmable for Volume Users

Pinout

TOP VIEW



Description

The HPL-82C138 is a high performance Programmable Chip Select Decoder (PCSD) which is intended to be used for both memory and I/O chip select decoder applications. Utilizing the Harris advanced scaled SAJI IV CMOS process, this circuit provides bipolar speed with CMOS power consumption.

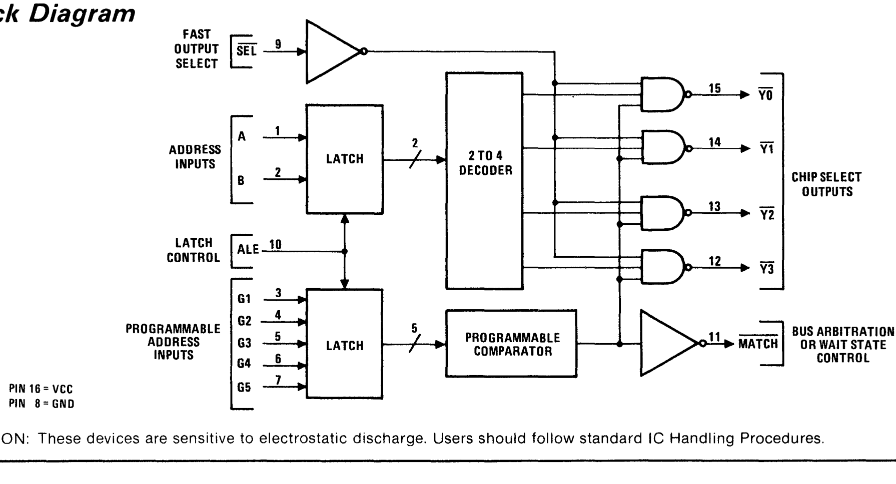
In a typical application, this circuit can replace two to three 74HCXX SSI/MSI ICs. The associated reductions in board area, chip count and power consumption result in a substantial increase in system reliability and an attendant decrease in system cost. A speed improvement of a factor of three to four over an equivalent implementation with 74HCXX logic is also realized. The fast decode provided by the 82C138 can result in improved system performance or a dramatic reduction in total system cost since less expensive, slower memories and I/O devices can be used.

The HPL-82C138 is ideal for either eight or sixteen bit microprocessor applications as a "bootstrap" PROM decoder or other memory and I/O decoder applications where four or fewer devices require selection within a section of address space.

The five "GX" inputs are field programmable for either high or low true address decoding. The Harris fuse link technology used in this product provides a permanent fuse with stable storage characteristics over the full temperature ranges of 0° to +75°C, -40°C to +85°C, and -55°C to +125°C.

Transparent latches are utilized on all address inputs which permits the 82C138 to be used with both multiplexed and non-multiplexed address/data bus microprocessors.

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow standard IC Handling Procedures.

Absolute Maximum Ratings*

Supply Voltage .... 0.0V to +8.0V
Operating Supply Voltage .... +4.0V to +6.0V
Input Voltage .... GND -0.5V to VCC +0.5V
Output Voltage .... GND -0.5V to VCC +0.5V
Storage Temperature .... -65°C to +150°C

Operating Temperature (Ambient)

HPL-82C138-5 .... 0°C to +75°C
HPL-82C138-9 .... -40°C to +85°C
HPL-82C138-2/-8 .... -55°C to +125°C

** CAUTION: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. While programming refer to the " Programming Specifications."*

D.C. Electrical Specifications

(Operating)

HPL-82C138-5 (VCC = 5.0V ± 10%, TA = 0°C to +75°C)
HPL-82C138-9 (VCC = 5.0V ± 10%, TA = -40°C to +85°C)
HPL-82C138-2/-8 (VCC = 5.0V ± 10%, TA = -55°C to +125°C)

SYMBOL	PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS
IIH	Dedicated	"1"		+1	μA	VIH = VCC MAX
IIL	Input Current	"0"		-1	μA	VIL = 0V, VCC = VCC MAX
VIH	Input Threshold	"1"	2.0		V	VCC = VCC MAX HPL-82C138-5/-9
		"1"	2.2		V	VCC = VCC MAX HPL-82C138-2/-8
VIL	Voltage	"0"		0.8	V	VCC = VCC MIN
VOH1	Output Voltage	"1"	3.0		V	IOH1 = -5mA
VOH2		"1"	VCC-0.4		V	IOH2 = -1mA
						VCC MIN, VIL MAX, VIH MIN
VOL	Output Voltage	"0"		0.4	V	IOL = +5mA
ICCSB*	Standby Power Supply Current			50	μA	VIH = VCC MAX IF = 0.0μA, VCC = VCC MAX
ICCOP*	Operating Power Supply Current			2	mA/MHz	VI = VCC or GND IF = 0.0μA, VCC = VCC MAX

* ICCSB, ICCOP specifications are achieved only after complete programming of the device. These specifications are sampled and guaranteed but not 100% tested. While testing these specifications, output pins should be left open circuit.

A.C. Switching Specifications

(Operating)

HPL-82C138-5 (VCC = 5.0V ± 10%, TA = 0°C to +75°C)
HPL-82C138-9 (VCC = 5.0V ± 10%, TA = -40°C to +85°C)
HPL-82C138-2/-8 (VCC = 5.0V ± 10%, TA = -55°C to +125°C)

		HPL-82C138-5		HPL-82C138-9		HPL-82C138-2/-8		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
TAVYL	Propagation delay A, B, or G to Output Low	—	50	—	50	—	50	ns
TGVML	Propagation delay G to Match Output Low	—	50	—	50	—	50	ns
TSLYL	Select Access Time to Output Low	—	35	—	35	—	35	ns
TSHYH	Select Access Time to Output High	—	35	—	35	—	35	ns
TGXMH	Match De-Select Propagation Delay	—	50	—	50	—	50	ns
TAVLL	Address Set-Up to ALE Trailing Edge	15	—	15	—	15	—	ns
TLLAX	Address Hold From ALE Trailing Edge	15	—	15	—	15	—	ns
TAVSL	Address Set-Up to $\overline{SEL}$ Low (Glitch-Free Operation)	15	—	15	—	15	—	ns
TSHAX	Address Hold From $\overline{SEL}$ High (Glitch-Free Operation)	15	—	15	—	15	—	ns
TLHLL	ALE Pulse Width	15	—	15	—	15	—	ns

All AC parameters are tested under worst case conditions, with C_L = 50pF.

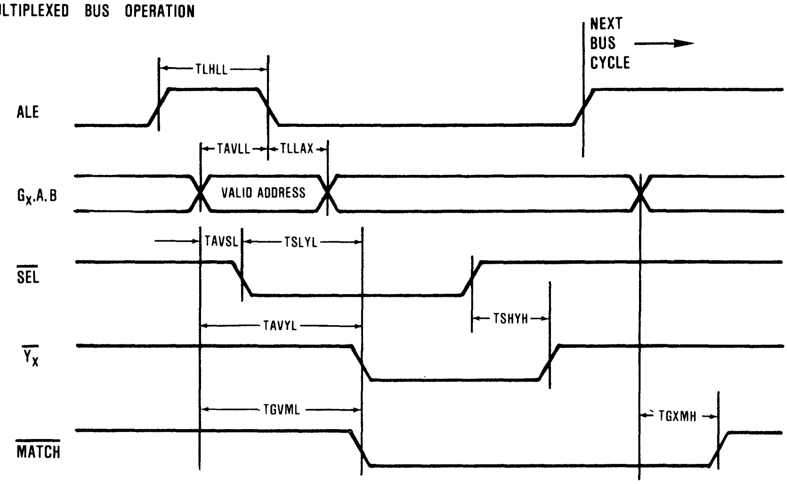
Capacitance

T_A = + 25°C (NOTE: Sampled and guaranteed - but not 100% tested.)

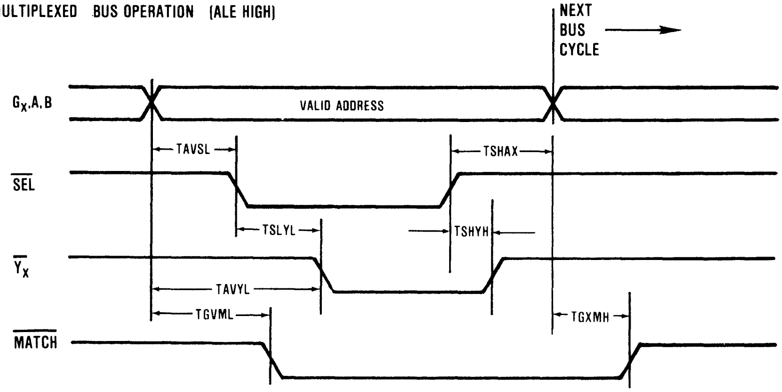
SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance	5	pF	VI = VCC or GND, f = 1 MHz
CO	Output Capacitance	10	pF	VO = VCC or GND, f = 1 MHz

Switching Time Definitions

MULTIPLEXED BUS OPERATION



DEMULTIPLEXED BUS OPERATION (ALE HIGH)

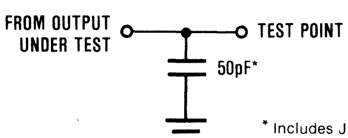


NOTES 1 In order to ensure glitch-free operation of the $\overline{Yx}$ outputs, set-up and hold times should be observed.

2 The $\overline{SEL}$ input controls the $\overline{Yx}$ outputs only and has no effect on the $\overline{MATCH}$ output

3 AC switching characteristics are measured with inputs switching between GND and 3 0V t_r, t_f 5ns (10%–90%)

A.C. Test Load



* Includes Jig and Probe Total Capacitance.

Programming

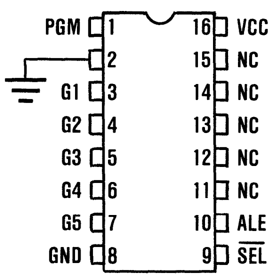
Following is the programming procedure which is used for the HPL-82C138 programmable logic device. This device is manufactured with all fuses intact. Any desired fuse can be programmed by following the simple procedure shown on the following page. One may build a programmer to satisfy the specifications described in the table, or use any of the commercially available programmers which meets these specifications. Please contact Harris for a list of approved programmers.

Programming Specifications

TABLE 1.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
VCCP	VCC Voltage During Programming		11.50	12.00	12.00	V
VCCV	VCC Voltage During Verify		4.75	5.00	5.25	V
ICCP	ICC Limit During Programming		—	100	200	mA
VNEG	Edit Enable & Mode Select Voltage		-6.00	-6.00	-7.00	V
INEG	Edit Enable & Mode Select Current		—	—	-5.00	mA
VIL	Input Voltage Low		0.00	0.00	0.80	V
VIHV	Input Voltage High	verify (1)	VCCV-2	VCCV	VCCV	V
VIHP	Input Voltage High	programming (1)	VCCP-2	VCCP	VCCP	V
IILP	Input Current Low	VIL = 0.0V	—	0	1	μA
IIHV	Input Current High	verify	—	0	1	μA
IIHP	Input Current High	programming	—	0	1	μA
PWP	Programming Width		4.5	5.0	5.5	msec
TD	Pulse Seq. Delay		1	1	—	μsec
tr1	Signal Rise Time	10% to 90%	0.01	0.1	1	μsec
tr2	VCC Rise Time	10% to 90%	0.01	0.1	5	μsec
tf1	Signal Fall Time	90% to 10%	0.01	0.1	1	μsec
tf2	VCC Fall Time	90% to 10%	0.01	0.1	5	μsec
TPP	Programming Period		—	5.1	—	msec
FL	Fuse Attempts/Link		1	1	2	cycles

(1) Inputs defined as logic "1" (VIHV or VIHP) must track the VCC power supply when the supply is raised or lowered. The input levels should never exceed the level on the VCC Pin.



NOTE: While programming the CMOS HPL device, no input pins should be left floating. Output pins (11-15) should be left unconnected. It is suggested that a 0.1μF capacitor be placed between VCC and GND to minimize VCC voltage spikes.

FIGURE 1. HPL-82C138 EDIT MODE PINOUT

Programming Procedure

Set Up:

a. During programming or operation, no input pins should be left floating.

b. No input pin voltage should ever be greater than the voltage applied to the device VCC pin.

c. The device should be decoupled with a 0.1μF or greater capacitor located at the device socket and placed between the VCC and GND pins.

Power up:

a. Initially, all input pins including power supply pins should be at ground potential.

b. Normally, the input pins (pins 3-7, 9, 10) are driven with an open collector driver with a pull-up resistor to the VCC pin (pin 16) so that these inputs automatically track the voltage on the VCC pin when they are set to the high state. This prevents the voltage level on the input pins from exceeding the voltage applied to the VCC pin.

c. Ramp the VCC pin (pin 16) to VCCV and the input pins (pins 3-7, 9, 10) to VIHV.

Programming Sequence

a. After a delay TD, the programming mode is entered by taking the programming enable pin (pin 1) to VNEG. Pin 1 must remain at VNEG throughout the entire programming sequence.

b. Wait TD and raise pin 16 to VCCP and pins 3-7, 10 to VIHP. At the same time, the $\overline{SEL}$ input (pin 9) is set to either VIHP or VIL in order to select the desired polarity of the input which is to be programmed. When $\overline{SEL}$ is at VIHP, the input will be programmed high true. When $\overline{SEL}$ is at VIL, the input will be programmed low true.

c. Wait TD and pulse the input to be programmed to ground for PWP milliseconds. It should be noted that only one input should be programmed at a time.

d. After a delay TD, return pin 16 to VCCV and pins 3-7, 10 to VIHV.

e. Repeat steps b), c), and d) until pins 3-7 have been programmed with the appropriate polarity.

f. When all inputs have been programmed as explained above, wait TD and return the programming enable pin (pin 1) to VIL.

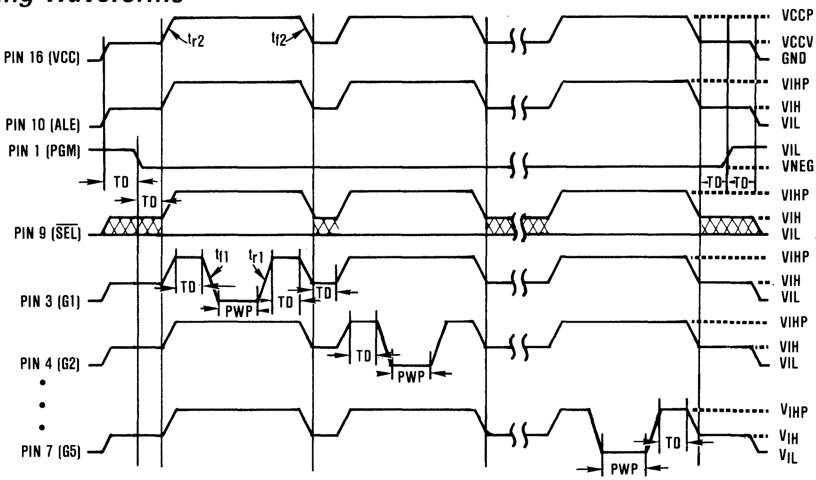
Fuse Integrity Testing

a. Correct programming of the device should be verified by applying test vectors to the input pins.

b. Fuse integrity is tested by applying VCC to the device and measuring the static power consumption of the device. With all inputs at VCC or GND and the output pins unloaded, the measured ICCSB of the device should be less than 50 μA at VCC = 5V and T = 25°C. This guarantees that all fuses have been blown to a final state which is not marginal and will not create a reliability problem over the life of the device. NOTE: Any device which fails this test should be rejected even if it passes functional testing in order to ensure no future reliability problems associated with marginally blown fuses.

IMPORTANT: All five inputs must be programmed regardless of desired high or low input polarity. The advanced design of the fuse select circuitry (Patent Pending) provides for ultra-low post programming ICCSB and requires that one fuse on each input be programmed.

Programming Waveforms



HARRIS Mini-HPL™ Family

PREVIEW

CMOS HPL™
Programmable Logic

Features

- Equal to or Better than 74ALSXX Speeds when Replacing Three or More Levels of Logic.
- TTL/CMOS Compatible
- 16-Pin Dual In-Line Package
- Micro-Amp Standby Power
- Lower Operating Power than Possible with 74HCXX Logic in Most Applications

Applications

- Random Logic Replacement of 74HCXX, 4000, 74XX, 74LSXX, 74ALSXX, and 74FXX Logic Families
- Battery Operated Systems
- High-Rel Sealed Enclosure Systems
- Military Systems

Mini-HPL Family

PART NUMBER	NUMBER OF INPUTS	NUMBER OF OUTPUTS
HPL-74HC2L	12 Data	2 Logical
HPL-74HC4L	10 Data	4 Logical
HPL-74HC6L	8 Data	6 Logical
HPL-74HC2R	8 Data, 2 Clock, 2 Preset/Clear	2 Registered
HPL-74HC4R	8 Data, 1 Clock, 1 Preset/Clear	4 Registered
HPL-74HCRL	7 Data, 2 Clock, 1 Preset/Clear	2 Registered, 2 Logical

Description

The Harris Mini-HPL family of Programmable Logic Devices represents a fresh, new approach to programmable logic. This family consists of a total of six part types (16-pin DIP) which have been designed to efficiently replace 74HCXX and 4000 series SSI devices. The programmable approach provides a highly flexible, high-performance, low-power alternative to discrete logic. Utilizing the Harris advanced scaled SAJI IV CMOS process, this circuit can provide bipolar speeds with CMOS power consumption.

The design approach implemented in this family of parts incorporates a new "macro-cell" concept (patent pending) for both inputs and outputs. Input macro-cells are multiple-input/single-output structures which have the capability of being programmed to implement any basic gate such as AND, OR, NAND, NOR, or INVERT (see Figure 1). This is accomplished by selectively programming both input and output polarity as well as providing the capability of deselecting any individual input.

The logical results of the input macro-cells are used as inputs to the output macro-cells. Output macro-cells can also accomodate multiple inputs (see Figure 2). The purpose of the output macro-cell is to logically combine one or more input macro-cells in order to either increase the number of variables on a given output function (thereby widening the gate) or to increase the number of logic levels replaced. Complex structures such as "AND-OR-INVERT", etc. can also be realized with this approach.

In a typical application, this circuit can replace 3-6 ICs while providing the equivalent of two to four levels of logic. The resultant speed of the design will often be two to three times faster than an equivalent 74HCXX implementation. The obvious benefits to the user include a reduced chip count, a reduction in board space, and decreased power dissipation. This adds up to increased system reliabilty and an attendant decrease in system cost.

Macro-Cell Diagrams

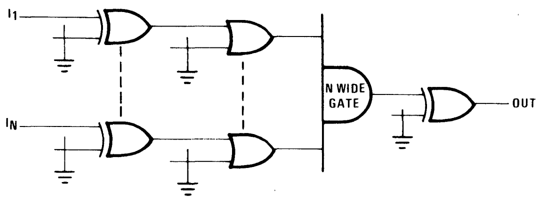


FIGURE 1. INPUT MACRO-CELL

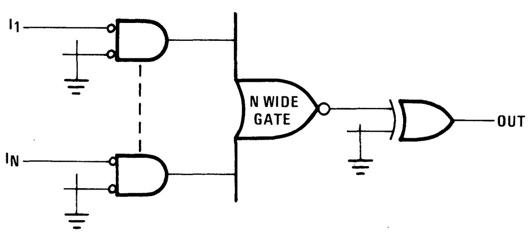


FIGURE 2. OUTPUT MACRO-CELL

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

CMOS

64XX Bus Interface Circuits

7

PAGE

CMOS BUS DRIVER DATA SHEETS

HARRIS

HD-6431

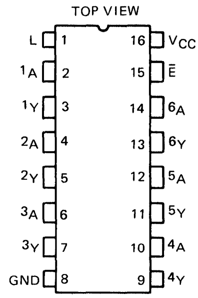
Not Recommended
For New Designs
See 82C82/82C83H

CMOS Hex Latching Bus Driver

Features

- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY 300pF
- SOURCE CURRENT 4mA
- SINK CURRENT 6mA
- PROPAGATION DELAY 75nsec MAX.

Pinout



Description

The HD-6431 is a self-aligned silicon gate CMOS Latching Three-State Bus Driver. This circuit consists of 6 non-inverting latching drivers with separate input and output. A high on the strobe line L allows data to go through the latches and a transition to low latches the data. A high on the Three-State control Ē forces the buffers to the high impedance mode without disturbing the latched data. New data may be latched in while the buffers are in the high impedance mode.

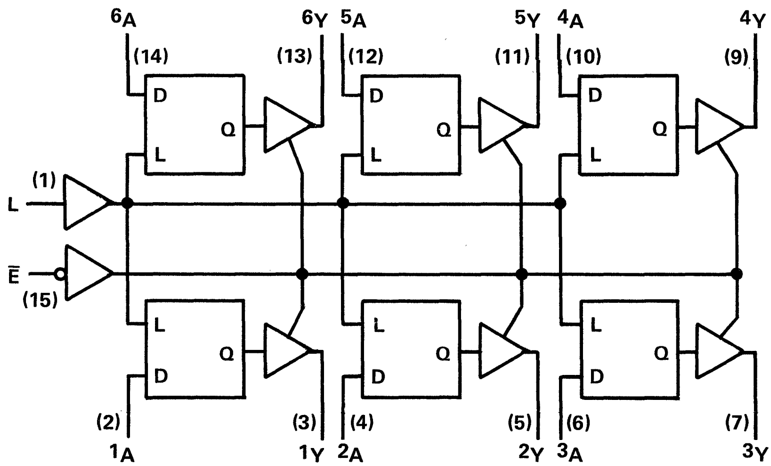
Outputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

Truth Table

CONTROL INPUTS		DATA PORT STATUS	
Ē	L	A	Y
H	L	X	HI-Z*
H	H	X	HI-Z
L	↓	X	*
L	H	L	L
L	H	H	H

* Data is latched to the value of the last input
X = Don't Care
HI-Z = High Impedance
↓ = Transition from High to Low level

Functional Diagram



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

HARRIS

HD-6432

CMOS Hex Bi-Directional Bus Driver

Not Recommended For New Designs See 82C86H/82C87H

HD-6432

Features

- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY 300pF
- SOURCE CURRENT 4mA
- SINK CURRENT 6mA
- PROPAGATION DELAY 55nsec MAX.

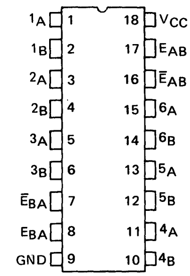
Description

The HD-6432 is a self-aligned silicon gate CMOS bi-directional bus driver. This circuit consists of 12 drivers organized as 6 bi-directional pairs. Four enable lines select drive direction or Three-State mode.

Outputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

Pinout

TOP VIEW



Truth Table

CONTROL INPUTS				DATA PORT STATUS	
E_{AB}	$\overline{E}_{AB}$	E_{BA}	$\overline{E}_{BA}$	A	B
L	X	H	L	O	I
X	H	H	L	O	I
H	L	X	H	I	O
H	L	L	X	I	O
L	X	L	X	ISOLATED	
X	H	X	H	ISOLATED	
L	X	X	H	ISOLATED	
X	H	L	X	ISOLATED	
H	L	H	L	NOT ALLOWED	

I = Input, O = Output, X = Don't Care

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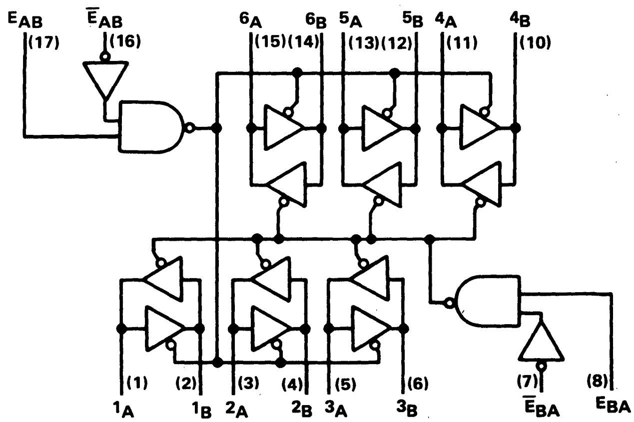
64XX BUS INTERFACE CIRCUITS

Functional Diagram



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

HARRIS

HD-6433

CMOS Quad Bus Separator/Driver

Not Recommended For New Designs

Features

- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY 300pF
- SOURCE CURRENT 4mA
- SINK CURRENT 6mA
- PROPAGATION DELAY 50nsec MAX.

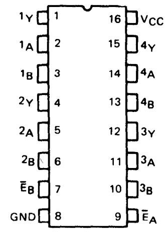
Description

The HD-6433 is a self-aligned silicon gate CMOS bus separator/driver. This circuit consists of 8 drivers organized as 4 pairs of bus separators which allow a unidirectional input bus and a unidirectional output bus to be interfaced with a bi-directional bus.

Outputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

Pinout

TOP VIEW

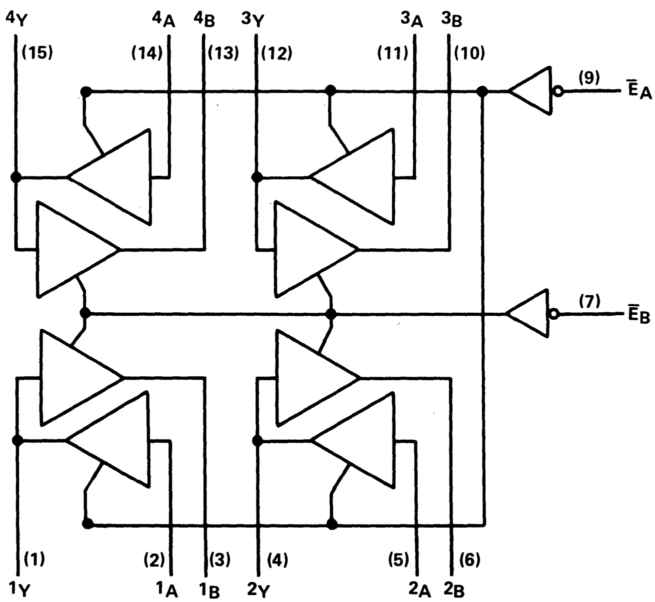


Truth Table

CONTROL INPUTS		FUNCTION		
$\overline{E}_A$	$\overline{E}_B$	A	B	Y
L	L	I	O	O
L	H	I	D	O
H	L	D	O	I
H	H	ISOLATED		

I = Input, O = Output, D = Disconnected

Functional Diagram



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

HARRIS

HD-6434

CMOS Octal Resettable Latched Bus Driver

Not Recommended For New Designs See 82C82/82C83H

Features

- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY 300pF
- SOURCE CURRENT 6mA
- SINK CURRENT 9mA
- PROPAGATION DELAY 50nsec MAX.

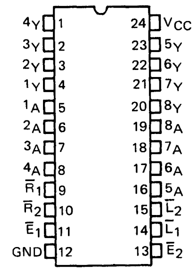
Description

The HD-6434 is a self-aligned silicon gate CMOS latching Three State bus driver. This circuit consists of 8 non-inverting latching drivers with separate input and output. A low on both strobe lines ($\overline{L}$) allows data to go through the latches and a transition to high latches the data. A high on either Three State control ($\overline{E}$) forces the buffers to the high impedance mode without disturbing the latched data. A low on either reset line ($\overline{R}$) forces each of the latches to a low level. New data may be latched in while the buffers are in the high impedance mode.

Outputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

Pinout

TOP VIEW

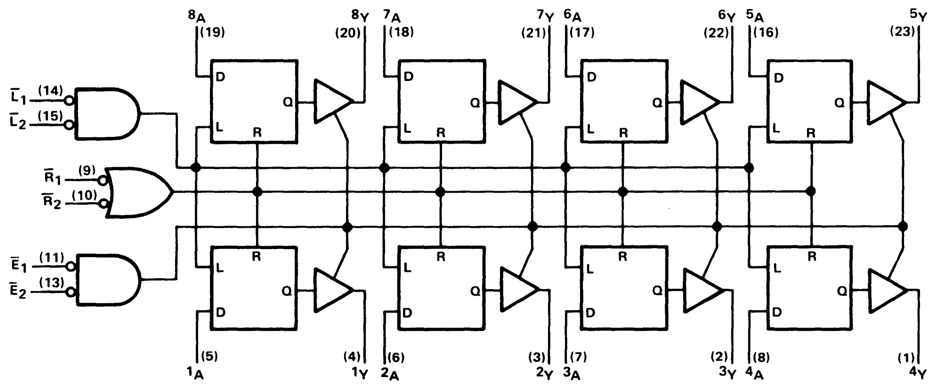


Truth Table

CONTROL INPUTS						DATA	
$\overline{R}_1$	$\overline{R}_2$	$\overline{E}_1$	$\overline{E}_2$	$\overline{L}_1$	$\overline{L}_2$	A	Y
X	X	H	X	X	X	X	Hi-Z
X	X	X	H	X	X	X	Hi-Z
L	X	L	L	X	X	X	L
X	L	L	L	X	X	X	L
H	H	L	L	L	L	L	L
H	H	L	L	L	L	H	H
H	H	L	L	↑	L	X	*
H	H	L	L	L	↑	X	*

X = Don't Care Hi-Z = High Impedance L = Low
H = High * = Data is latched to the val e of the last input
↑ = Transition from a Low to High level

Functional Diagram



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64XX BUS INTERFACE CIRCUITS

HARRIS

HD-6436

CMOS Octal Bus Buffer/Driver

Not Recommended For New Designs See 82C82/82C83H

Features

- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY 300pF
- SOURCE CURRENT 6mA
- SINK CURRENT 9mA
- PROPAGATION DELAY 55nsec MAX.

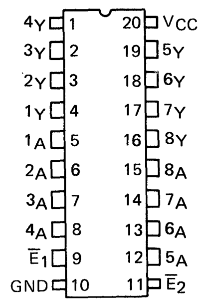
Description

The HD-6436 is a self-aligned silicon gate CMOS Three State buffer driver. The circuit consists of 8 noninverting buffers with separate inputs and outputs which permit this driver to be used for bi-directional or uni-directional busing. A high on either Three State control line $\overline{E}_1$ or $\overline{E}_2$ will force the drivers to the high impedance mode.

Outputs guaranteed valid at V_{CC} = 2.0V for Battery Backup Applications.

Pinout

TOP VIEW

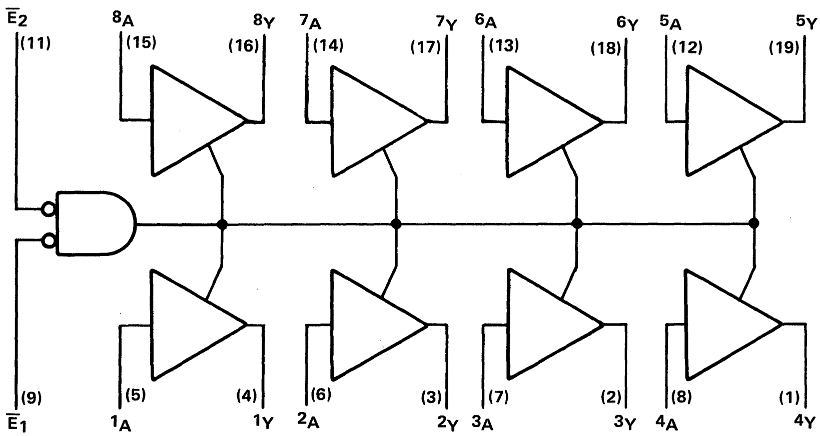


Truth Table

CONTROL INPUTS		INPUT	OUTPUT
$\overline{E}_1$	$\overline{E}_2$	A	Y
L	L	L	L
L	L	H	H
L	H	X	Hi-Z
H	L	X	Hi-Z
H	H	X	Hi-Z

L = Low, H = High
X = Don't Care
Hi-Z = High Impedance

Functional Diagram



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

HARRIS

HD-6440

CMOS Latched 3 to 8 Line Decoder-Driver

Not Recommended For New Designs See HPL-82C338

Features

- HIGH SPEED DECODING FOR M...
- INCORPORATES 3 ENABLE INPU... ...PLIFY EXPANSION
- LOW POWER . . . . TYPICALLY<50μW @ 5V STANBDY
- HIGH NOISE IMMUNITY
- AVAILABLE IN BOTH MILITARY AND INDUSTRIAL TEMPERATURE RANGE
- HIGH CAPACITANCE DRIVE 200pF
- HIGH OUTPUT DRIVE . . . . I_{OH} = -2mA, I_{OL} = 2.4mA
- SINGLE POWER SUPPLY

Description

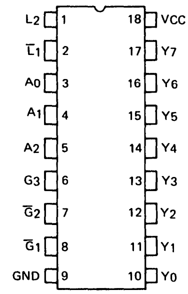
The HD-6440 is a self aligned silicon CMOS gate latched decoder. One of 8 output lines is decoded, and brought to a low state, from the 3 input lines. There are two latch enables ($\overline{L_1}$, L_2), one complemented and one not, to eliminate the need for external gates. The output is enabled by three different output enables ($\overline{G_1}$, $\overline{G_2}$, G_3), two of them complemented and one not. Each output remains in a high state until it is selected, at which time it will go low.

When using high speed CMOS memories, the delay time of the HD-6440 and the enable time of the memory is usually less than the access time of the memory. This assures that memory access time will not be lengthened by the use of the HD-6440 latched decoder driver. The latch is useful for memory mapping or for systems which use a multiplexed bus.

Outputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

Pinout

TOP VIEW



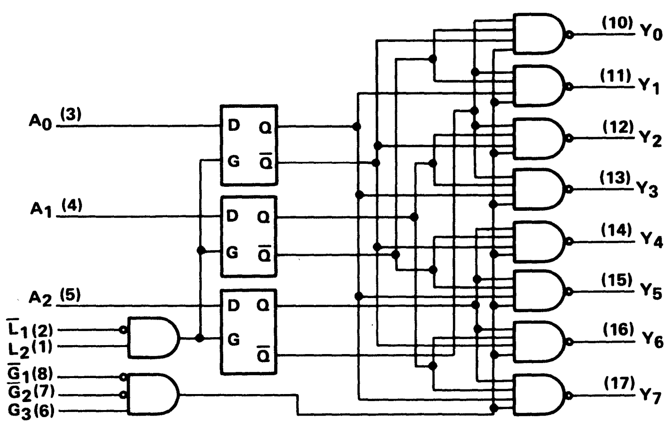
Truth Table

INPUTS								OUTPUTS								
ENABLE					ADDRESS											
$\overline{G_1}$	$\overline{G_2}$	G_3	$\overline{L_1}$	L_2	A_2	A_1	A_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	FUNCTION
X	X	L	X	X	X	X	X	H	H	H	H	H	H	H	H	DISABLE
X	H	X	X	X	X	X	X	H	H	H	H	H	H	H	H	DISABLE
H	X	X	X	X	X	X	X	H	H	H	H	H	H	H	H	DISABLE
L	L	H	L	H	L	L	L	L	H	H	H	H	H	H	H	DECODE
L	L	H	L	H	L	L	H	H	L	H	H	H	H	H	H	DECODE
L	L	H	L	H	L	H	L	H	H	L	H	H	H	H	H	DECODE
L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	DECODE
L	L	H	L	H	H	L	L	H	H	H	H	L	H	H	H	DECODE
L	L	H	L	H	H	L	H	H	H	H	H	H	L	H	H	DECODE
L	L	H	L	H	H	H	L	H	H	H	H	H	H	L	H	DECODE
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	DECODE
L	L	H	X	L	X	X	X	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	LATCHED
L	L	H	H	X	X	X	X	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	LATCHED

L = Low, H = High, X = Don't Care

Y_n = Data is latched to the value of the last input

Functional Diagram



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

HARRIS

HD-6495

CMOS Hex Bus Driver

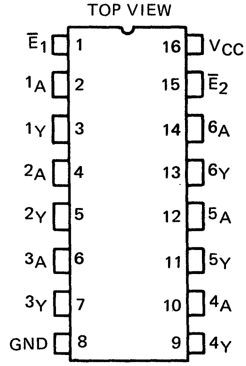
Not Recommended For New Designs See 82C82/82C83H

Features

- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY 300pF
- SOURCE CURRENT 4mA
- SINK CURRENT 6mA
- PROPAGATION DELAY 45nsec MAX.

Pinout

TOP VIEW



Description

The HD-6495 is a self aligned silicon gate CMOS Three-State buffer driver. The circuit consists of 6 non-inverting buffers with separate inputs and outputs which permit this driver to be used for bi-directional or uni-directional busing. A high on either Three-State control line $\overline{E}_1$ or $\overline{E}_2$ will force the drivers to the high impedance mode.

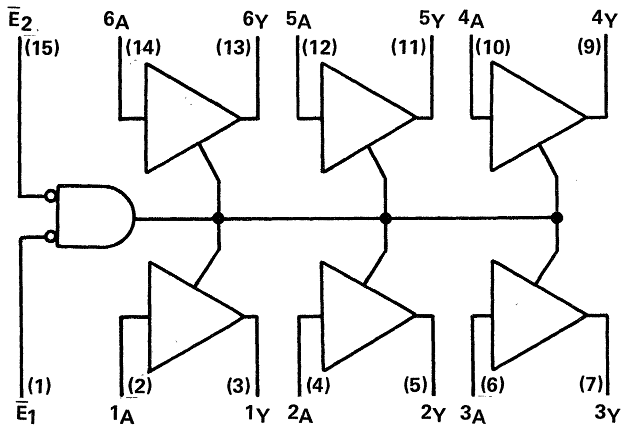
Outputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

Truth Table

CONTROL INPUTS		INPUT	OUTPUT
$\overline{E}_1$	$\overline{E}_2$	A	Y
L	L	L	L
L	L	H	H
L	H	X	HI-Z
H	L	X	HI-Z
H	H	X	HI-Z

X = DON'T CARE
HI-Z = HIGH IMPEDANCE

Functional Diagram



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

CMOS

Article Reprints

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PAGE

8- and 16-bit processors round out high-level C-MOS architecture options

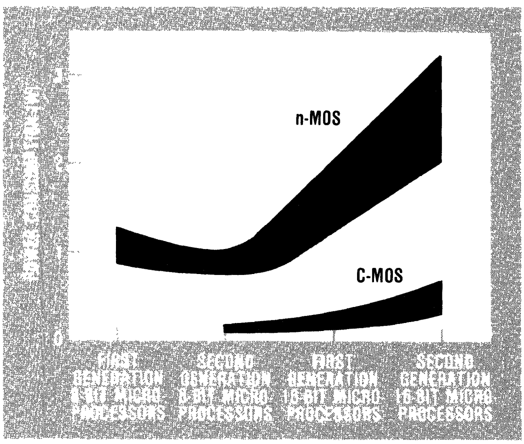
By selecting appropriately from the microprocessor variety, designers can build for either low parts count or full multiprocessor capabilities

by Walter J. Niewierski, *Harris Semiconductor Corp., Melbourne, Fla.*

□ In the past, designers were stuck between a rock and a hard place when choosing between complementary-MOS and n-channel MOS microprocessors. Designing with n-MOS circuitry ensured relatively high speeds, but its high power consumption required that extra measures be taken to dissipate heat. On the chip level, this meant both higher die temperatures, which degraded reliability, and large packaging, which used up precious board real estate. On the system level, heat sinks, fans, and vents were needed to cope with the greater heat, and these components necessitated larger enclosures.

An end to the heat problem

As more and more transistors are packaged together, the power-dissipation problems associated with n-MOS increase exponentially (Fig. 1). This is pushing the industry toward C-MOS, because its performance, measured in terms of speed and capacity, compares favorably with n-MOS, yet its power requirements are much less—meaning that chip densities can be increased with no penalty in heat dissipation.



1. N-MOS power dissipation. The exponential growth of power required by ever-denser n-channel MOS is being reversed by the move to low-power complementary-MOS. Greater device densities in C-MOS stem from its lower power dissipation.

Though slower, C-MOS requires less power, and thus has none of the heat-dissipation problems of n-MOS. Chips can be designed in smaller packages, and the system becomes lighter and more compact.

For example, the C-MOS J-11 self-aligned junction-isolated (SAJI) chip set [*Electronics,* Dec. 15, 1982, p. 131] designed by Harris Corp. for Digital Equipment Corp. consists of a data chip and a control chip that together emulate the hardware and software capabilities of the DEC PDP-11/70 minicomputer. The J-11 requires less than 1 watt of power with a single +5-volt power supply, while the equivalent logic for the PDP-11/70 minicomputer is contained on 20 printed-circuit boards that require 800 W. An equivalent microprocessor in n-MOS probably could not be produced because of its high power dissipation.

High-density packaging

The high power requirements of n-MOS and bipolar chips have another drawback. The heat generated in many of these parts cannot be dispersed adequately by the standard ceramic leadless chip-carriers or low-cost plastic packages. The 16-bit 80C86 and the 8-bit 80C88 families from Harris, fabricated with the SAJI C-MOS process, can be housed in industry-standard chip-carriers as well as in plastic and ceramic dual-in-line packages. Work is currently under way to provide plastic leaded chip-carriers for the 80C86/88 products to further simplify—and cut the cost of—high-density packaging.

Increased densities can be extended beyond the chip level by creating modular systems using chip-carriers and ceramic DIP substrates. For example, several chip-carrier-packaged circuits can be mounted onto a ceramic substrate to provide a high level of integration in a single package. In the standard J-11 configuration, the control and data chips are mounted atop a 60-pin substrate housed in 84-pad chip-carriers, but two additional control chips can be attached to the underside of the package. This type of arrangement comes in handy when, for example, an expanded instruction set is needed.

High-density memory modules can be assembled in a similar fashion. The Harris HM-92570 buffered C-MOS random-access-memory module combines 16 HM-6516 16-K C-MOS RAMs on one DIP substrate, along with address decoders and signal buffers. An entire 265-K system is on one 1.3-by-2.66-inch 48-pin DIP substrate.

Besides achieving n-MOS density levels, modern-day C-MOS can hit comparable speeds. Both the 16-bit 80C86 and the 8-bit 80C88 microprocessors operate at 5 megahertz, matching the speeds of n-MOS, and 8-MHz versions will be available during the third quarter of 1984. Both chips have a full complement of support circuits for peripherals and buses at the 5-MHz level, and some of these support chips operate at 8 MHz.

Static design

Even more compelling for the designer weighing the benefits of C-MOS versus n-MOS is the fact that C-MOS is more amenable to use in static designs. Static processors, such as the 80C86, 80C88 and J-11, maintain internal register and data values with the clock stopped, resuming operation immediately after the clock is restarted. With entire systems stopped and power reduced to the sub-milliampere standby-current level, battery life is lengthened and system current requirements drop. System analysis is also simpler, since complex bus operations can be stepped one clock cycle at a time.

C-MOS also lets the designer customize the speed and power characteristics of the product while maintaining the maximum performance. C-MOS operating power is often specified in terms of milliamperes per megahertz because power is a function of switching frequency—that is, as chip switching frequency decreases, so does power (and vice versa). However, defining this relationship early on is a key to a successful low-power, and thus lightweight and compact, design.

A direct comparison of C-MOS and n-MOS power requirements, using worst-case operating- and standby-current specifications, shows C-MOS system operating power is often less than 10% of the worst case n-MOS requirement (table). For example, the 80C86's operating current is specified 50 mA at 5 MHz, compared with 340 mA for the n-MOS part (Fig. 2).

An even larger power savings—nearly three orders of magnitude—is achieved in the standby mode, when the clock to the microprocessor system is stopped and all chips go into standby. Both the 80C86 and 80C88 have a 500-microampere guaranteed standby-current specification. The 80C86 peripheral product line—including the 82C55A programmable peripheral interface and the 82C59A priority-interrupt controller—have standby currents of less than 10 μA.

Simply swapping C-MOS circuits directly for n-MOS and bipolar circuits in existing designs will not show a system cost savings. Such a strategy may reduce power requirements, but it will not achieve the degree of savings that flow from a system approach to C-MOS design. By comparing n-MOS and C-MOS systems, it is easy to see the ripple effect that high operating power can have on system design.

For example, in an prototypical n-MOS system based on the 16-bit 8086, the power dissipation is 1.7 W. If n-MOS memory and a combination of n-MOS and bipolar peripherals are added to support the 8086, power must then be increased from 25 to 30 W, depending upon the system's size. In fact, if future expansion is a possibility, a fairly large and heavy 50-W power supply might be mandated. Die temperatures in such a system will rise significantly, typically in the 40-to-60°C range. Fans and heat sinks are needed to compensate for these increases, and with a filter for the fan plus vents, the enclosure expands. It thus becomes more difficult to assemble and heavier to transport.

The boons of current reduction

If the same system is redesigned in C-MOS, it becomes evident how the effects of current reduction ripple throughout a system. Moreover, because the 80C86 maintains the same processor architecture as its n-MOS counterpart, the considerable expense involved in system hardware and software redevelopment has been avoided.

The first design decision to make is whether the system must run at all times. If there are periods when it is simply waiting for inputs or other events, power requirements may be cut significantly by shutting down the system clock oscillator.

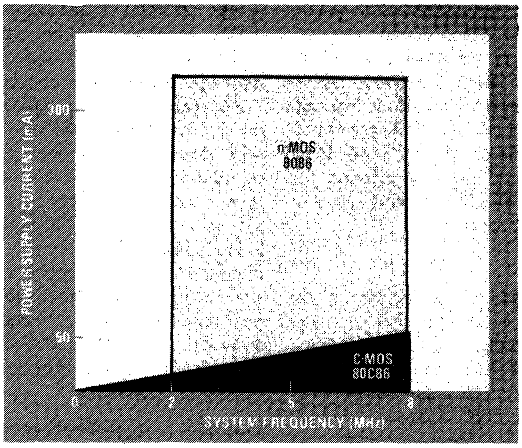
The next step in redesign is choosing memory and peripherals. C-MOS devices frequently attain performance equal to their n-MOS and bipolar equivalents but with a significant reduction in current. The switch to C-MOS buys power savings of 50:1 for peripherals and 5:1 for

WORST-CASE POWER USE

n-MOS/bipolar		C-MOS		
Part number	Operating current, I cc OP (mA)	Part number	Operating current, I cc OP (mA)	Standby current, I cc SB (μA)
8086	340	80C86	50	500
8251A	100	82C52	3	10
8254	140	82C54	10	10
8255A	120	82C55A	3	10
8259A	85	82C59A	3	10
8282 (2)	320	82C82 (2)	6	20
8283 (2)	320	82C83 (2)	6	20
8286 (2)	320	82C86 (2)	6	20
8287 (2)	320	82C87 (2)	6	20
8284A	162	82C84A	40	10
8288	230	82C88	5	10
2-K-by-8-bit RAM (2)	180	HM-6516	20	100
2-K-by-8-bit-ROM (2)	125	HM-6616	30	100
Total	2,762 mA	I cc OP / I cc SB	188 mA	840 μA

memories. Overall system power can be reduced by more than 90% by using C-MOS parts.

In fact, power needs could be so low that even battery operation can be specified. Low-power operation reduces die operating temperatures, which ups reliability. Typical die-temperature increases for C-MOS are in the 2-to-5°C range, obviating cooling fans and heat sinks. Vents can be closed to ensure clean operating conditions in harsh environments and the sealed enclosures can be designed smaller and lighter. At final assembly the C-MOS system is portable, lightweight, sealed from the outside environment, and has the same computing power as its n-MOS equivalent.



2. C-MOS vs. n-MOS. Low-power complementary-MOS technology combined with static design features give the 16-bit 80C86 microprocessor lower current requirements and increased operating-frequency range, compared with n-channel MOS parts.

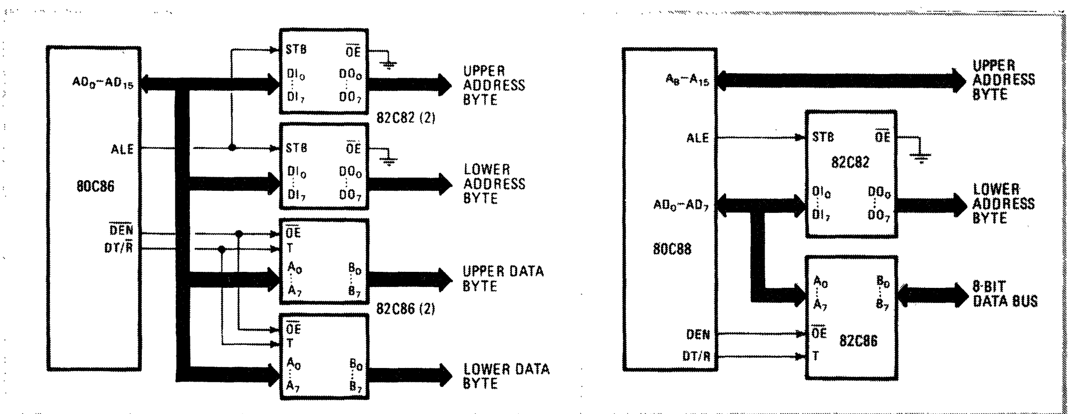
Bus-configuration considerations

A wide range of systems can be configured using the the 80C86 and the 80C88, all sharing the low power dissipation of C-MOS. The 80C88 lends itself to building stand-alone systems with a minimum component count, while multiprocessor systems are best handled with the 80C86.

The single most important difference between the 80C86 and 80C88 microprocessors is in the interface with the external world (Fig. 3). The 80C86 communicates in 16-bit words using a multiplexed address and data bus. The 80C88 also has a multiplexed bus, but it is only 8 bits wide. Moreover, the lower half of the 80C88 bus multiplexes addresses and data, whereas the redesigned upper half is dedicated to addresses.

Several important system-level tradeoffs flow from this redefinition of the 80C88 bus. One involves the question of throughput. Since both chips are 16-bit machines internally and run the same software, 16 bits of data are usually transferred between the central processing unit and memory. In the 80C86, this takes place on the 16-bit bus and is usually completed in a single bus cycle, but in the 80C88 and its 8-bit data bus, a 16-bit transfer requires two bus cycles to acquire the same data. The 8-bit bus architecture of the 80C88 would appear to result in severe performance penalties, but there are two mitigating factors. First, the pipelined architecture of the 80C88 optimizes performance. Both the 80C86 and the 80C88 use an instruction queue within the processor to store data, permitting the 80C88 bus interface unit to prefetch data while the execution unit runs the current instruction. This arrangement cuts system-bus dead time so that the 80C88's 8-bit bus can perform nearly as well as the 80C86's full 16-bit bus. Typical throughput of the 80C88 is approximately 75% to 90% that of the 80C86.

The second mitigating factor in the 8-bit bus—and probably its biggest advantage—is the reduced hardware required to implement it. The 16-bit 80C86 interface



3. Parts count. The 16-bit bus of the 80C86 (a) requires more parts than the 8-bit bus of the 80C88 (b). Since both are 16-bit machines internally, the 80C88 requires two bus cycles to complete a transfer, but its pipelining means it can run at 75% to 90% of the speed of the 16-bit chip.

requires three 82C82/83 C-MOS address latches and two 82C86/87 C-MOS bus transceivers to properly demultiplex the bus, more than twice as many as an 80C88 8-bit bus. Since lines A_8-A_{15} of the 80C86 are dedicated to addresses and are present at all times during the bus cycle, no latch or transceiver is needed. The bus-interface component count is cut in half.

The reduced component count in the system designed with the 80C88 has several important advantages, not the least of which is reduced cost. Of course, a decreased component count is an obvious factor in decreasing cost. The savings in board real estate and the consequent manufacturing costs must also be factored into a cost-savings equation.

Minimum and maximum operating modes

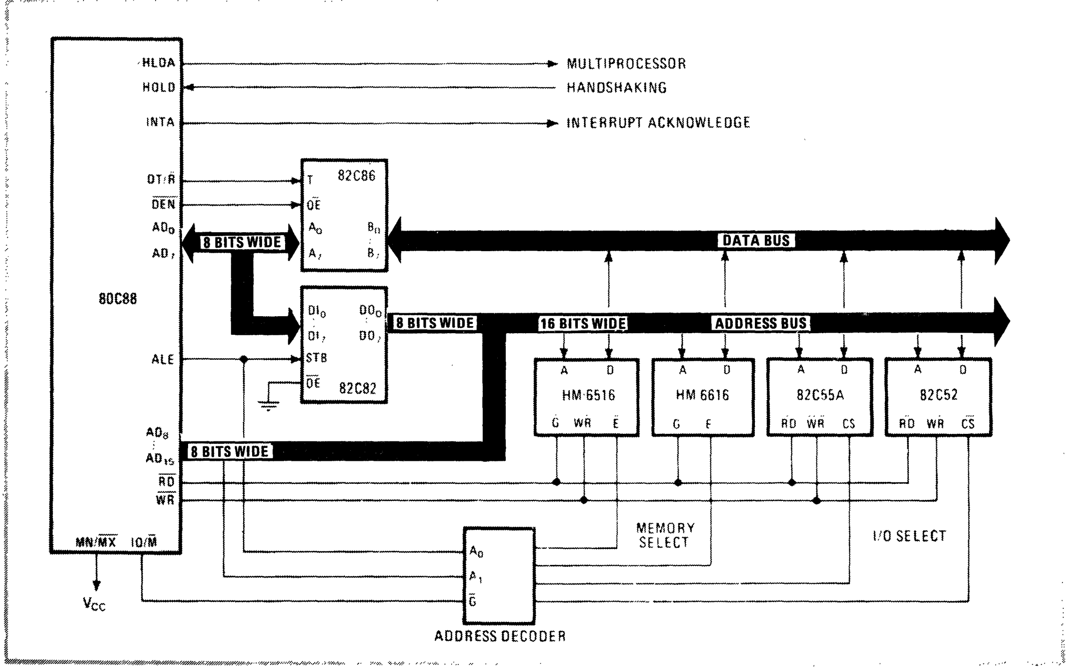
Opting for a reduced component count is made easier by the architectures of the 80C86 and the 80C88. With both architectures, the designer can decide the level of chip and system complexity required by the application. Given the choice of two operating structures, the minimum and maximum modes, the designer can configure systems based on the 80C86 and 80C88 microprocessors for each application.

The two mode names are indicative of their functions. In the minimum mode, the CPU provides all the control and interface signals necessary to achieve a minimum component count. Operation in the maximum mode uses additional bus-interface and control chips to make large system design and expansion simpler and more efficient.

When either the 80C86 or the 80C88 are operating in the minimum mode, pins provide all necessary input/output and memory control signals. Figure 4 shows a minimum configuration for a stand-alone remote controller using the 80C88 system. Three lines—data-transmit-/receive ($DT/\overline{R}$), data-enable ($\overline{DEN}$), and address-latch-enable (ALE)—provide all address-latch and data-transceiver control. Input/output memory ($IO/\overline{M}$) and write ($\overline{WR}$) are used for memory and I/O data transfer, respectively. The interrupt-acknowledge line (INTA) is available for incorporating interrupt capabilities with the 82C59A C-MOS priority-interrupt controller. The HOLD and HLDA (hold acknowledge) lines provide low-level multiprocessor support.

Minimum power in minimum systems

As Fig. 4 shows, using the minimum mode for small systems can be very efficient. The operating-system firmware is contained in the Harris HM-6616, a 2-K-by-8-bit C-MOS programmable read-only memory that requires only 15 mA of current at an enable rate of 1 MHz. The 10-mA HM-6516 16-K C-MOS RAM also consumes very little operating power. The synchronous design of these two memories keys internal switching of transistors to the chip-enable signal transition. This arrangement results in a significantly lower operating current than does an asyn-



4. Minimum-mode operation. When configured in minimum mode, the CPU provides all control signals necessary in this stand-alone controller. Such C-MOS features as on-chip address latches in synchronous memories make it possible to eliminate the external 82C82 and the 82C86.

chronous scheme implemented in either n-MOS or C-MOS.

The 82C52 serial controller interface provides high-speed asynchronous serial data communications at a rate up to 1 megabaud with only a 1-mA/MHz current requirement. The 82C55A programmable peripheral interface provides parallel interfacing to I/O devices. The 82C82 and 82C86 bus-interface circuits are needed to demultiplex the 80C88 bus and increase address- and data-signal driving capability.

In the 5-MHz 80C88 system configuration shown in Fig. 4, worst-case power dissipation is 130 mA. The equivalent n-MOS or bipolar power dissipation would be between 1,100 and 1,200 mA. In the minimum mode, the parts count can be reduced, especially when a designer takes advantage of some special features available on many C-MOS chips. For example, the on-chip address latches could be used to eliminate the 82C82 address latch and the 82C86 bus transceiver.

However, minimum-mode designs are usually optimized for specific applications and often prove inflexible. As systems change, these designs are not easily upgraded to accommodate new requirements. If the specification requires that expansion or changes be easy to implement, then the maximum mode should be investigated.

In larger systems, or those that will require upgrading, the maximum mode is the most efficient way to use the available CPU pins to control system transactions. In Fig. 5, the eight control lines used in the minimum configuration have changed functions (the minimum-mode pin functions are shown in parentheses).

Three lines (S_0, S_1, and S_2) send CPU status information to the 82C88 C-MOS bus controller. The 82C88, in turn, decodes the 80C88 status lines and sends out bus, memory, and I/O control signals. The six minimum-mode bus interface signals $\overline{WR}$, ALE, $\overline{INTA}$, $\overline{DEN}$, DT/$\overline{R}$, and IO/$\overline{M}$ are passed to the 82C88, where $\overline{WR}$ and IO/$\overline{M}$ combine to produce three sets of signals expanding system capability: memory and I/O read, advanced memory and I/O write, and memory and I/O write.

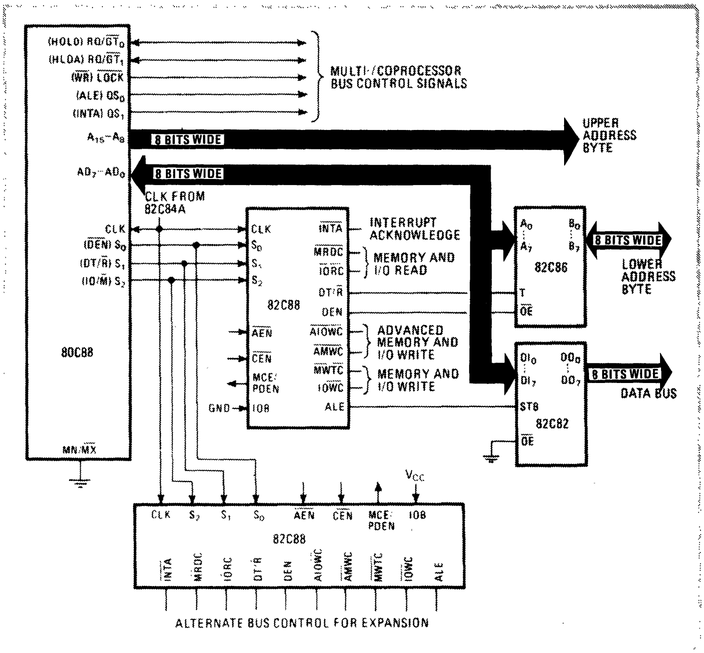
Two multiprocessor interface signals (HOLD and HLDA) are replaced by two dual-function request/grant pins ($RQ/\overline{GT}_0$ and $RQ/\overline{GT}_1$) and a $\overline{LOCK}$ output. These three control signals can handle a significantly higher level of multiprocessing coordination than the minimum-mode signals. In addition, the 80C88 maximum-mode pinout includes two queue-status lines (QS_0 and QS_1), which allow easy integration of coprocessors to increase system throughout.

Simple expansion

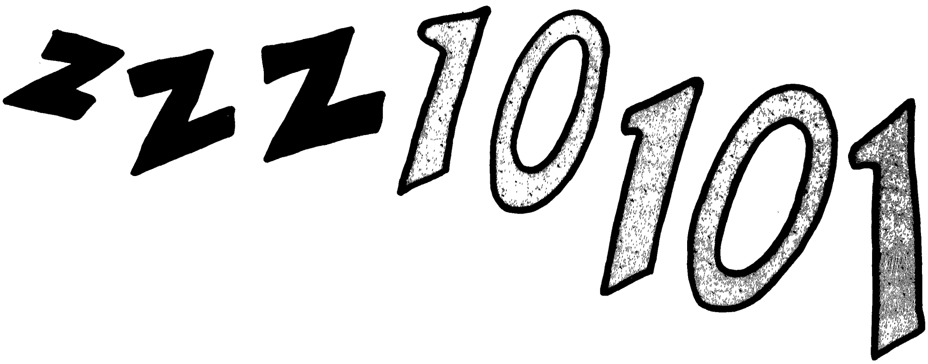
The extra functions provided by maximum-mode operation make system expansion simple. By adding additional 82C88s, separate system and I/O buses can be added. In the system in Fig. 5, two 82C88 C-MOS bus controllers provide all the control signals for a local bus and a shared system bus. In a non-C-MOS system, adding a 8288 bipolar controller would increase power by 2.6 W. The 82C88 draws only 5 mA at 5 MHz and requires less than 0.0085 W, or only about 3% of the power required by the bipolar 8288.

Power dissipation in the system can be further reduced by using the static design attributes of the C-MOS processors in a distributed processing environment. The processors' periods of operation can be closely controlled by the host, permitting entire subsystems to be powered down.

For example, when there is no I/O, that entire subsystem can be put into a standby mode, reducing current to 1 to 2 mA. The I/O subsystem can be reawakened in 20 to 50 milliseconds by an incoming interrupt. In situations where the incoming interrupt requests must be handled faster than 20 to 50 ms, clocking can be reduced below 5 MHz while a low supply current is still maintained The static-design feature of the 80C86 family supports development of multiprocessor distributed systems because power can be reduced by a factor that is inversely proportional to the resulting system's up-time. □



5. Maximum-mode operation. Using the 80C88 in maximum mode optimizes available CPU pins. By increasing the number of bus controllers, it becomes easy to build separate system and I/O buses for multiprocessor applications without increasing system power.



CMOS static clock exerts complete control

When all parts of a CMOS system are static, moment-to-moment demands can be met without performance degradation by slowing or stopping the clock

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The full power-saving potential of static CMOS can be realized only with control over the system clock. The clear advantages of the technology (see *box,* "Why static CMOS?") in low-power systems have not always been achieved, because designers have had to make multichip ad hoc solutions or else forgo flexible use of the most parsimonious modes.

The 82C85 static clock controller/generator (*Electronic Products,* June 17, p. 93) gives simple and complete control of the operating modes of static CMOS systems. Though the 82C85 is directly compatible with the Harris 80C86 and 80C88 CMOS 16-bit static microprocessors, it is designed for general-purpose CMOS system clock control, supporting full-speed, slow, stop-clock, and stop-oscillator operation.

To take the full advantage of static system design, the groundwork for static operation must be laid at the very beginning of the development program and not simply treated as an afterthought to an existing design. This is when decisions must be made regarding all power, performance, and response requirements. The designer can tailor a system to achieve the optimum power/performance tradeoff for the application, thus increasing efficiency and lowering the cost of implementing a static design.

In static-CMOS system design, there are four basic operating modes. In ascending order of power saving, these are: fast, slow, stop-clock, and stop-oscillator. Each has distinct power and performance traits that can be matched to the needs of a particular system at a specific time (see *Table 1*).

A single system may require all of these operating modes at one time or another during normal operation. The power and performance levels of a system are then under the designer's control.

Fast mode: maximum everything

The most common operating mode for a system is the fast mode. In this mode, the 82C85 operates at the maximum frequency determined by the main oscillator. Most systems continually strive for the greatest throughput, and this occurs during full-speed operation. Maximum-frequency operation insures that the CPU, memory, and peripherals are running as fast as possible.

Although the fast mode insures that the system runs at the highest possible rate, it also dissipates the most power. The 82C85 will be running with a crystal frequency of up to 24 MHz; all internal counter logic will also be switching at this rate. Consequently, system power is at its maximum level.

While the system and peripheral clocks are running continuously at the maximum frequency, so are the CPU and peripheral circuits. Because CMOS power dissipation is directly related to frequency of operation, the fast mode has the highest power level of the four modes available (see *Table 2*). There are alternative modes of operation to reduce the average system operating-power dissipation. This does not mean, however, that system speed or throughput will be reduced. When used appropriately, the stop-clock, stop-oscillator, and slow modes can make the design more power-efficient and keep system performance at a maximum.

Table 1. Operating-mode characteristics of 82C85

Operating mode	Description	Power level	Performance	Typical 82C85 power-supply current (mA)
Stop-oscillator	All system clocks and main clock oscillator are stopped	Maximum saving	Slowest response due to oscillator-restart time	0.024
Stop-Clock	System CPU and peripheral clocks stop, but main clock oscillator continues to run at rated frequency	Reduced system power	Fast restart; no oscillator-restart time	14.1
Slow	System CPU clocks are slowed while peripheral clock and main clock oscillator run at rated frequency	Power dissipation slightly higher than stop-clock	Continuous operation at low frequency	16.9
Fast	All clocks and oscillators run at rated frequency	Highest power	Fastest response	24.7

Go slow to reduce power

When continuous operation is critical but power dissipation remains a concern, the 82C85 slow-mode operation divides the CLK and CLK50 outputs by 256 (PCLK frequency is unaffected). The slow mode allows the CPU and the system to operate at a reduced rate, which

Why static CMOS?

A dynamic circuit's clock must be maintained at or above a certain minimum frequency to guarantee proper operation. Internally, the dynamic cells must be refreshed at a certain rate or frequency in order to maintain valid data. Without this minimum clock frequency, the data within the CPU or peripheral device can be lost or altered.

In contrast, a static circuit needs no minimum frequency to guarantee proper operation. Static processors such as the 80C86 and 80C88 maintain valid data over the full frequency range from dc to the maximum frequency rating.

The argument of static versus dynamic NMOS is unimportant since power dissipation for dynamic NMOS is fairly constant over its limited operating frequency range. In CMOS, though, power is directly proportional to speed or frequency. Thus, static system design takes on new meaning. Static CMOS design yields the lowest power available since the frequency of operation can be reduced to dc.

A static system design has several prerequisites. First, it requires static CMOS microprocessors and support circuits, such as the 80C86/80C88 family, which can operate and maintain data from dc to the maximum frequency of operation. Second, it requires circuitry to control starting and stopping of the system clock as well as maintaining proper phase relationships and pulse widths of the system and peripheral clocks.

The main benefit of static system design is its dramatic power saving and the ability to control when and where this power saving will occur. For example, an 80C86 multiprocessor system can be designed to allow the software executive routine to power down the entire system or just portions of the system not in use (i.e., certain I/O sections or file-maintenance areas). This is done by using multiple 82C85s throughout the system. This individual or group clock control is the key to a truly flexible minimum-power system.

Another benefit of static design is the ability to single-step the system clock. This becomes a very important asset when debugging prototype hardware in complex systems. Unlike software single-step debugging routines, commonly used in emulators, direct CPU clock control allows the hardware designer to troubleshoot high-speed signal movements normally hard to obtain as long as transmission line effects are not causing full speed problems.

For example, with the 80C86, one could actually single-step through each phase of the processor timing cycle (T-1, T-2, T-3, etc.) observing what happens on the address, data, and status lines. These signals can then be traced through the entire system because, with the clock stopped, signal levels are maintained indefinitely.

Low power eliminates thermal problems, creating several side benefits. Devices can be positioned closer together on the board, decreasing board size and weight. Sealed enclosures can be used because heat sinks and fans are no longer needed. System reliability increases, a smaller power supply can be used, and shipping weight and size are cut.

in turn reduces system power.

For example, the operating current for the 80C86 or 80C88 CPU is 10 mA per megahertz of clock frequency (50 mA at 5 MHz). In slow mode, CLK and CLK50 run at approximately 20 kHz (5 MHz divided by 256). At this reduced frequency, the average operating current of the CPU drops to 200 μA. Adding the 80C86/88's 500 μA of standby current brings the total current to 700 μA—a sharp contrast to 50 mA.

The 82C85, however, will not see such a major slow-mode reduction. Although the CLK and CLK50 outputs switch at a reduced frequency, the main 82C85 oscillator is still running at 15 MHz (for a 5-MHz system) or 24 MHz (for an 8-MHz system). The 82C85's power-supply current will typically be reduced by only 25% to 35%.

Using the 82C85's slow/fast mode is a simple matter. The chip provides an asynchronous SLO/FST pin, which determines the system clock speed. If the SLO/FST pin recognizes a logic 1 on its input, CLK and CLK50 will run in the fast mode, which is the crystal or oscillator frequency divided by 3. If the 82C85 recognizes a logic 0, on the SLO/FST pin, CLK and CLK50 will run in the slow mode (fast-mode frequency divided by 256).

Internal counters and logic require that the SLO/FST pin be held low for at least 195 oscillator or EFI (external-frequency-input) clock pulses before the slow-mode command is recognized. This eliminates unwanted fast-to-slow-mode frequency changes that could be caused by glitches or noise spikes. To guarantee fast-mode recognition, the SLO/FST pin must be held high for at least three oscillator or EFI pulses.

Because PCLK maintains its high-frequency operation, it can be used by other system devices that need a fixed high-frequency clock. For example, PCLK could be used to clock an 82C54 programmable interval timer to produce a real-time clock for the system or to serve as a baud-rate generator maintaining the serial data communications during slow-mode operation.

High-to-low or low-to-high transitions of the SLO/FST input will be recognized on the next rising or falling edge of PCLK. The transition time for slow to fast mode is calculated by

3 x (EFI or oscillator period) + PCLK high time + SLO/FST to PCLK setup.

Table 2. Typical system power-supply current for 82C85 operating modes

Devices	Stop-oscillator	Stop-clock	Slow	Fast
82C85	24.4 μA	14.1 mA	16.9 mA	24.7 mA
80C88	106.6 μA	106.6 μA	173.0 μA	23.8 mA
82C82	1.0 μA	1.0 μA	6.5 μA	1.7 mA
82C86	1.0 μA	1.0 μA	14.0 μA	1.4 mA
82C88	3.8 μA	3.8 μA	14.3 μA	3.5 mA
82C52	1.0 μA	1.0 μA	72.0 μA	151.2 μA
82C54	1.0 μA	3.5 μA	915.0 μA	943.0 μA
82C55A	1.0 μA	1.0 μA	1.2 μA	3.2 μA
82C59A	509.0 μA	509.0 μA	520.0 μA	580.0 μA
HD-6406	4.97 mA	4.97 mA	5.09 mA	5.12 mA
74HCXX plus other ICs	90.0 μA	90.0 μA	110.0 μA	2.9 mA
HM-6516	1.9 μA	1.9 μA	132.0 μA	820.0 μA
HM-6616	12.0 μA	12.0 μA	52.5 μA	6.3 mA
TOTAL with 6406	5.72 mA	19.8 mA	24.0 mA	71.9 mA
TOTAL without 6406	752.7 μA	—	—	—
CPU FREQUENCY	dc	dc	20 kHz	5 MHz
XTAL FREQUENCY	dc	15 MHz	15 MHz	15 MHz

All measurements taken at room temperature, V_{CC} = +5.0 V

In a 5-MHz 80C86 system (EFI frequency of 15 MHz), slow-to-fast-mode transition will occur within a maximum of 410 ns after the SLO/FST pin is brought high. It is important to remember that the transition time from slow to fast mode will vary with input frequency.

Stop-clock mode

The 82C85 can be used in the stop-clock mode simply by connecting the OSC output to the EFI input and pulling the F/C (frequency/crystal strapping option) input high. This puts the 82C85 into the external fre-

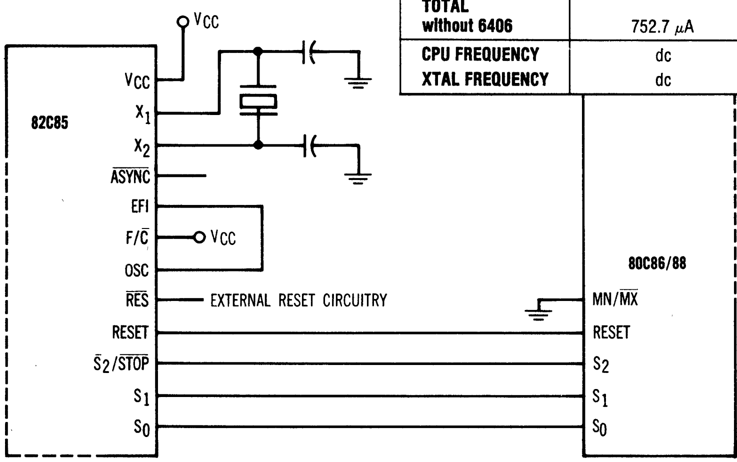


Fig. 1. When the 82C85 is operating in the EFI mode and using its oscillator circuit as the external frequency source, a Stop command will stop only the system clocks, not the 82C85 oscillator.

quency mode using its own oscillator as an external source signal (see *Fig. 1*). When the 82C85 is stopped in the EFI mode, the oscillator continues to run; only the clocks to the CPU and peripherals (CLK, CLK50, and PCLK) are stopped.

Because the oscillator is still running, the power-supply current level is higher than in the stop-oscillator mode. The 82C85 operating current for stop-clock operation is typically 10 to 15 mA, compared with the standby current of 100 μA in the stop-oscillator mode. All other devices in the system that are driven by the 82C85 will go into the lowest power standby mode, reducing system power by up to 75%.

Stop-oscillator mode

In the stop-oscillator mode, system power drops to its lowest level. All processes are stopped, and all devices are in minimum-power standby states. All data, however, are retained in the internal registers of all static circuits. No data is lost, and system operation begins in exactly the same state at which standby was entered.

All devices in the system that are driven by the 82C85 go into the lowest power standby mode. The 82C85 also goes into standby and requires less than 100 μA of supply current.

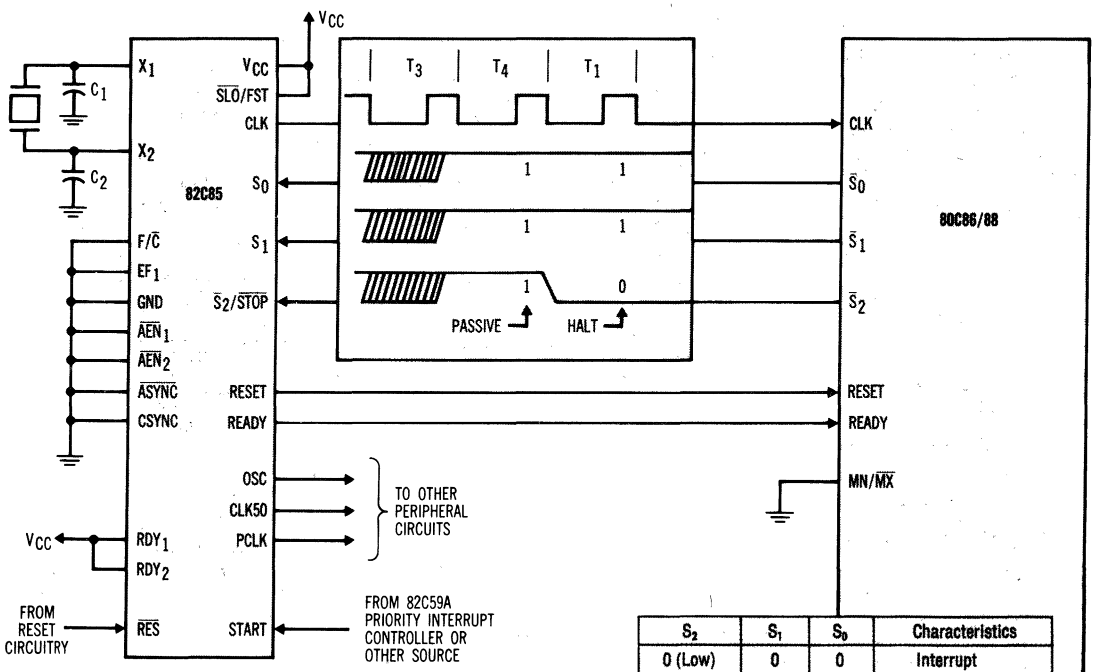
Maximum-mode clock control

Interface for the 82C85 stop and start functions has been optimized for 80C86/88 maximum-mode operation. Three control lines (S_2/STOP, S_1, S_0) are provided on the 82C85 to allow simple software control of the system clock. To allow direct software control of system clocks, these three control lines should be connected directly to the maximum-mode status lines (S_2, S_1, S_0) of the Harris 80C86 and 80C88 microprocessors (see *Fig. 2*).

In the maximum mode, the 80C86/88 status lines identify which type of bus cycle the CPU is starting to execute. These status lines are typically used by the 82C88 bus controller to decode the current bus-cycle status of the CPU. Figure 2 shows the status-line truth table for different operations.

The logic on the 82C85 S_2/STOP, S_1, and S_0 control inputs will recognize a valid software Halt executed by the 80C86 or 80C88 when in the maximum mode. Once this state has been recognized, the 82C85 stops its clock (F/C tied high) or oscillator circuitry (F/C tied low).

The 82C85 control lines (S_2/STOP, S_1, S_0) were designed to detect a passive 111 state followed by a Halt 011 logic state before recog-



S_2	S_1	S_0	Characteristics
0 (Low)	0	0	Interrupt Acknowledge
0	0	1	Read I/O port
0	1	0	Write I/O port
0	1	1	Halt
1 (High)	0	0	Code access
1	0	1	Read memory
1	1	0	Write memory
1	1	1	Passive

Fig. 2. Automatic stop-on-software-halt operation has been designed into the 82C85, for direct interface to the 80C86 and 80C88 in the maximum mode. When the system is connected as shown, the 82C85 detects on the CPU status lines a passive 111 state followed by a Halt 011 state. Once this sequence occurs, the 82C85 stops its clock and/or oscillator circuits (depending on which mode is being used).

nizing the Halt instruction and stopping the system clocks. In the maximum mode, the 80C86/88 status lines go into a passive (no bus cycle) logic 111 state prior to executing a Halt instruction. The qualification of a passive no-bus-cycle logic 111 state insures that random transitions of the status lines into a logic 011 state will not stop the system clock. This is necessary because the status lines of the 80C86/88 pass through an undefined state during T_3 of the bus cycle.

When the Halt instruction is decoded, the CLK and CLK50 outputs will be stopped in a logic 1 state after 1½ additional clock cycles. The Halt instruction is detected in the same manner whether the 82C85 is in the slow or the fast mode.

When the 80C86 and 80C88 microprocessors are configured in minimum mode (MN/MX pin tied high), the status lines S_0, S_1, and S_2 assume alternate functions. The logic states and sequences (passive before a Halt) necessary for automatic Halt detection in the 82C85 do not occur as in the maximum mode. The 82C85 controller cannot use the microprocessor status lines to detect a software Halt instruction when operating in minimum mode.

Independent stop control

However, the negative edge-activated S_2/STOP pin provides a simple means of clock control in non-maximum mode 80C86 and 80C88 systems. S_2/STOP can be used as an independent Stop control when S_1 and S_2 are held in the logical high state.

Keeping the S_1 and S_0 inputs at a logic 1 level and driving S_2/STOP from high to low will meet the requirement for a passive 111 state prior to a Halt 011 state. This feature allows 82C85 operation with both the 80C86 and 80C88 in the minimum mode, provides compatibility with other static CMOS microprocessors, and allows maximum flexibility in a system.

With S_2/STOP being used as a standalone Stop command line, system clocks can be controlled through an 82C55A programmable peripheral interface. This is accomplished

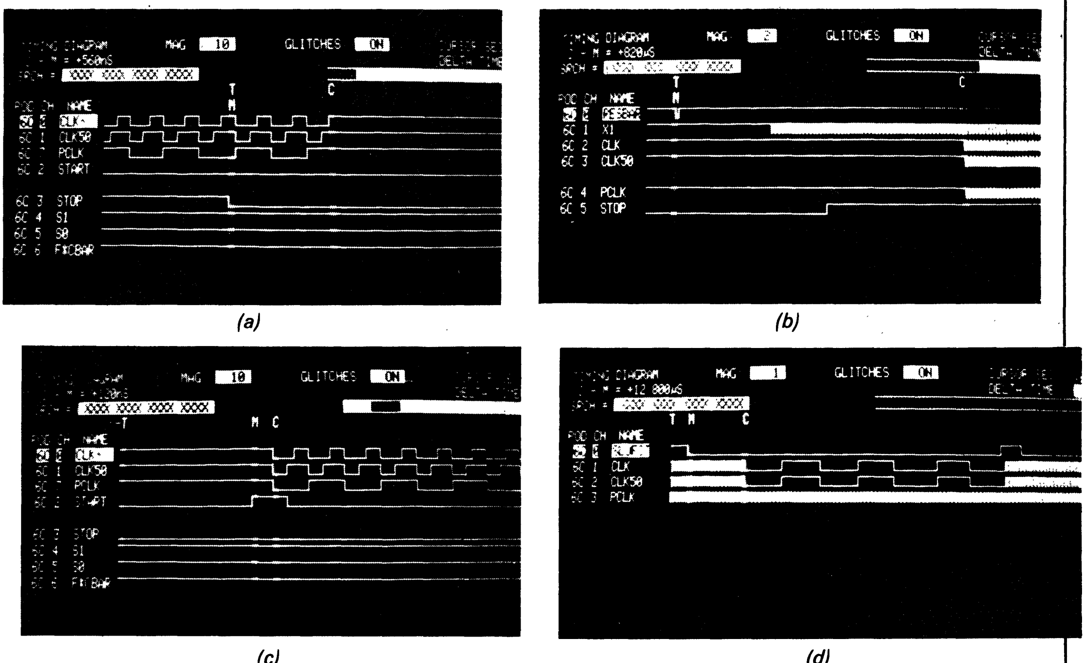


Fig. 3. When issued a Stop command (a), the 82C85 insures that all clocks complete their current cycle and then halt in the high state. In the Stop-oscillator mode (b), the 82C85 oscillator startup circuitry keeps the system clocks in the high state until the oscillator has stabilized. This is true for a reset (shown here) or for a Start command. When given a Start command in the Stop-clock mode (c), clocks start in 400 to 500 ns (at 5 MHz) and are negative-edge synchronized. Transition between fast and slow modes (d) results in clean, synchronized clock pulses in both modes (CLK and CLK50 both appear as 50% duty cycle signals due to the data-acquisition system sampling rate. CLK is actually 33% of the duty cycle).

by tying the pins S_0 and S_1 of the 82C85 to V_{CC} with the S_2/STOP input connected to a port pin on the 82C-55A. The 82C55A port pin should be configured as an output with a logical 1 output to the S_2/STOP pin. This will cause the 82C85 to see a logic 111 passive state before a logic 011 state is detected.

When a logic 0 is written to an 82C55A port pin, the S_2/STOP pin is pulled low, stopping the system clocks (CLK, CLK50, PCLK). In essence, the 82C85 is software controlled through the 82C55A. As with the SLO/FST interface, port C is a logical choice for this job because individual bit Set and Reset commands are available.

Upon receiving a Start command, the 82C85 will begin normal operation. The low state of the negative-edge triggered S_2/STOP input will not prohibit the clocks from restarting. After a Start or Reset command, the 82C85 must see a passive (111) state followed by a Halt 011 state to stop the system clocks. To accomplish this, the 82C55A must be brought high and then returned low again for the 82C85 to recognize the next Stop command.

Restarting the system

To start the 82C85 after it has been stopped, there is an independent Start input. Start is a level-triggered, active-high input and will override any Stop condition.

When F/C is tied low (crystal mode), a logic 1 on the Start input will restart the crystal oscillator. However, the stopped clock outputs (CLK, CLK50, and PCLK) remain stopped until two events occur: The oscillator startup envelope amplitude first reaches the threshold of the Schmitt trigger buffer internal to the X_1 input; then an internal counter must count 8,192 valid oscillator pulses.

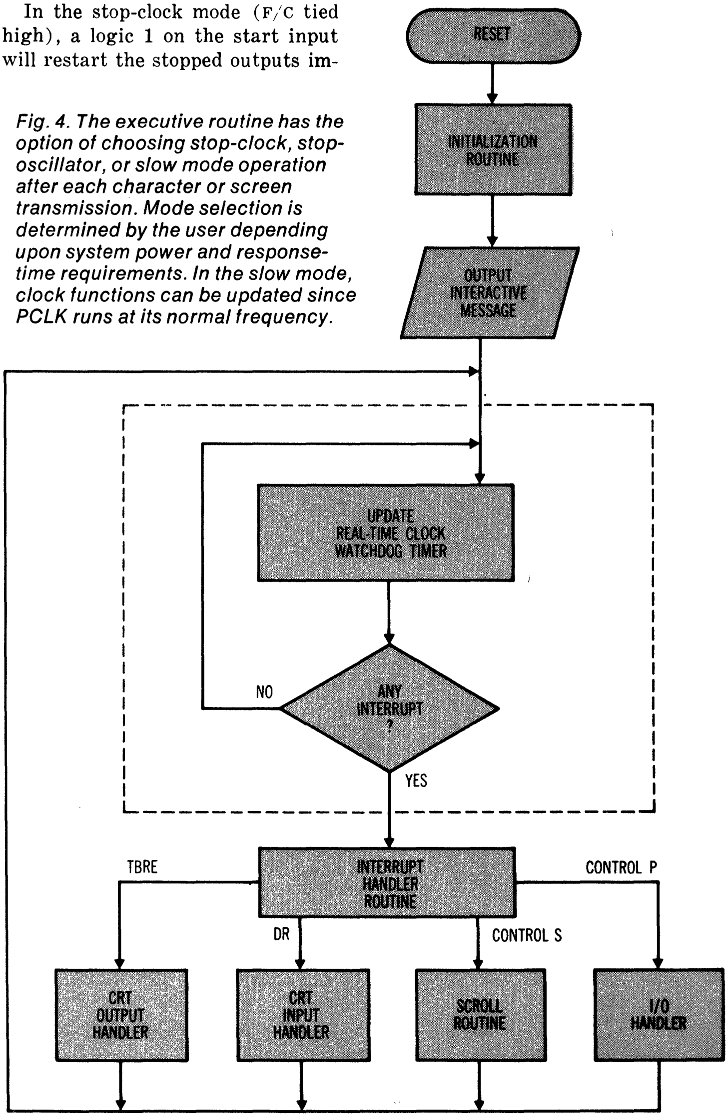
When the count is complete, the stopped clock outputs will start cleanly with the proper phase relationships. The count insures that high-frequency noise and crystal harmonics, which can occur during oscillator startup, are not allowed through to the clock outputs. Otherwise, undesired glitches or unsynchronized signals could appear at the clock outputs, resulting in clock signals that do not meet 80C86/88 clock specifications. This could lead to erratic or erroneous operation.

The total start time will vary depending upon the crystal frequency and manufacturer, the system power supply levels, temperature, and other factors. Typical oscillator start-to-CLK-output delay times are in the range of 500 μs to 2 ms.

In the stop-clock mode (F/C tied high), a logic 1 on the start input will restart the stopped outputs immediately after the start input is synchronized internally. No oscillator startup time is necessary, because the EFI source is either an external clock or the 82C85 OSC output. In either case, the EFI input source will be constantly running.

Control of the start input can be provided through an 82C59A priority interrupt controller or other such asynchronous, clock-independent source. The 82C59A INT output can be connected directly to the 82C85

Fig. 4. The executive routine has the option of choosing stop-clock, stop-oscillator, or slow mode operation after each character or screen transmission. Mode selection is determined by the user depending upon system power and response-time requirements. In the slow mode, clock functions can be updated since PCLK runs at its normal frequency.



Start pin and the INTR pin of the 80C86 or 80C88 microprocessors.

External events, such as a key-pad entry, can be used to produce an interrupt request to the 82C59A, which in turn will produce an interrupt. This high level on the Start input will cause the 82C85 to start the system clocks.

System performance is the key

When choosing between stopping the system clocks or stopping the oscillator, system response time enters the picture. Once stopped, how fast will the system resume operation when given a Start command? The answer could range from nanoseconds to milliseconds depending upon the mode of operation, the specific reason for restart, and the action that needs to be taken. The clock-control mode used must meet the specific restart response requirement of the system at that particular point (see *Fig. 3*).

When in the stop-clock mode, the 82C85 oscillator circuit is running and stabilized. In this case, restarting the clocks to the CPU is a simple matter. When the Start input is set to a logic 1 (high), internal circuitry gates the already running oscillator through to the clock-generation circuit. The internal signals are gated synchronously to ensure glitch-free, negative-edge-synchronized CLK, CLK50, and PCLK outputs.

The clock output will resume operation within 2 EFI cycles (137 ns at 5 MHz) of the Start command input. This will meet the needs of those systems requiring immediate responses to requests.

In the stop-oscillator mode, restarting the 82C85 takes a while longer. In this mode, the oscillator circuit is stopped in order to conserve power. Internal 82C85 circuitry forces the CLK and CLK50 outputs high, while stopping PCLK in its current state.

These outputs do not become active immediately after a restart command. As mentioned earlier, they remain high until internal circuitry detects 8,192 stable oscillator cycles. Once this criterion is met, then the CLK, CLK50, and PCLK outputs are allowed to start operation synchronously.

The oscillator stabilization period will typically last from 500 μs to 3 ms, depending upon the crystal, system voltage, operating temperature, or a multitude of other factors.

Performance analysis is critical

Response time to a Start or SLO/FST speed-change command is different for each operating mode. The key to properly utilizing these alternative modes is to ensure that, wherever possible, power is saved without degrading performance.

In an interrupt-driven system, for example, the executive software routine in the operating system spends

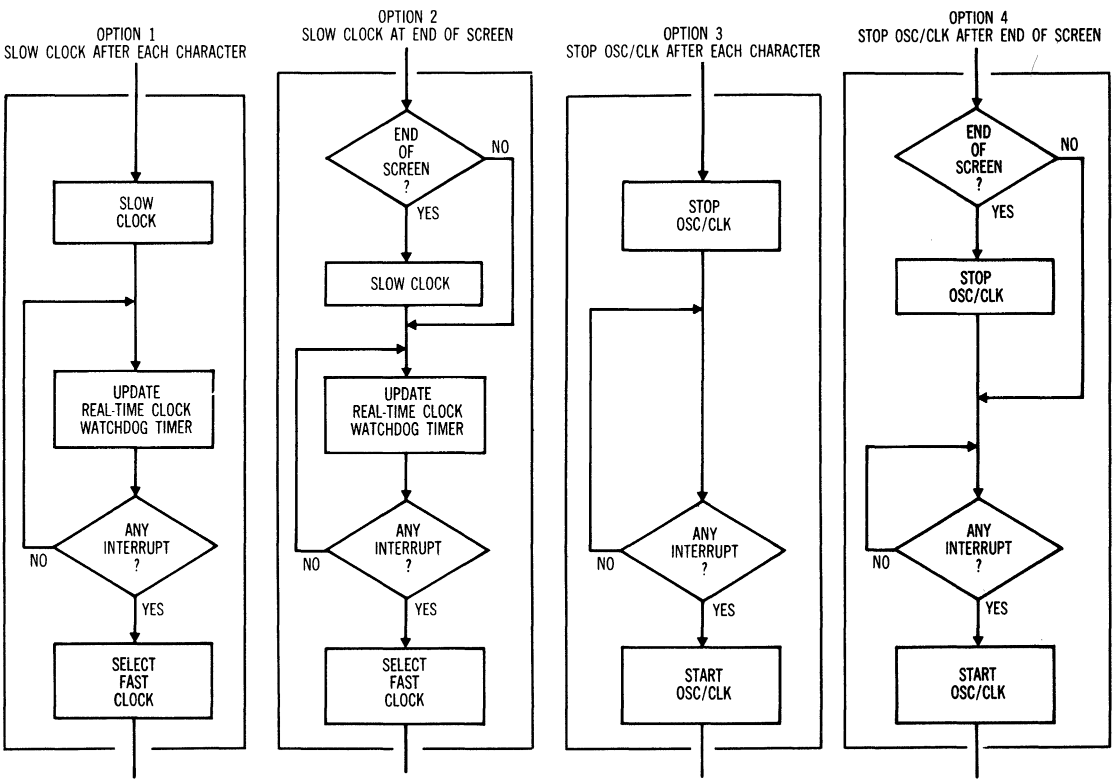


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Table 3. Effect of stop-oscillator mode on data transmission

Baud rate (baud)	Data-transmission time (ms)	Oscillator startup time (ms)	Nominal impact on character transmission time (ms)
19,200	0.52	2	−1.48
9,600	1.04	2	−0.96
4,800	2.08	2	+0.08 (no speed impact)
2,400	4.17	2	+2.17 (no speed impact)
1,200	8.33	2	+6.33 (no speed impact)

the majority of its time in an idle mode waiting for an interrupt from an external hardware source (see *Fig. 4*). When the interrupt is recognized, the necessary task is performed and then the program goes back into its idle mode to await the next interrupt.

Controlling the system clock in software using the 82C85 and Halt instructions positioned in the appropriate places throughout the program can save power without degrading performance. A closer look shows the power/performance tradeoffs that can be considered in a typical CRT-handler routine.

In this system, display data are sent to a remote terminal over a standard serial data link. The CPU loads data into a UART which then completes the data transmission. The system is not required to do any other task during the data-transmission time. The system and CPU can be stopped periodically at intervals based on the data-transmission rate. While the UART is transmitting data to the screen, the rest of the system can power down and wait for the next time data needs to be loaded to the UART from the CPU.

The major concerns in this case are when to stop the system and the impact on performance and power. Two options can significantly affect power and performance: stopping the system after each character is transmitted, or stopping the system after each screen refresh.

If power dissipation is the most important factor, then the best choice would be to use the stop-oscillator mode and stop the system in the main loop of the executive routine. This allows the system to enter a complete standby state after every character sent to the CRT.

An interrupt, signaling that the transmitter buffer register in the UART is empty, will take the 82C85 out of stop-oscillator mode and restart the crystal oscillator. After the oscillator stabilizes and the clock is restored, the interrupt is serviced.

Such a system requires a separate crystal oscillator circuit for the UART so that data can be transmitted when the 82C85 is stopped. This approach provides the lowest power of the two options; with the main system oscillator stopped, current flows only in the UART crystal circuit—typically 1 to 2 mA.

Low power, however, can come at the expense of response time. Because the crystal oscillator must be stabilized before the CPU can restart, data cannot be transmitted between the time the interrupt for more data occurs and the time the oscillator stabilizes. The startup time for crystal circuits can be from 1 to 2 ms, so each application must be evaluated individually. Performance is not affected in this mode as long as the transmission rate is 4,800 baud or less (see *Table 3*).

If faster transmission rates are needed, stopping just the clock and not the oscillator should be considered. Clock startup time is only 136 ns for a 15-MHz crystal. This increases supply current about 20 mA.

The second option, stopping the oscillator after each screen refresh, shows no impact on system response time at any baud rate. With the oscillator and system clock constantly running during a screen update, the CPU is available to respond immediately to the request for more data. This approach does, however, increase power dissipation because the oscillator is running for a much higher percentage of the time. ☐

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Advanced clock controller cuts power needs, size of static CMOS systems

With a one-chip controller-generator running a static CMOS system in any of three minimal-frequency modes, power consumption will drop to a trickle.

The faster a CMOS system runs, the more power it consumes. Consequently a natural way to reduce power consumption is to run the system at a minimal frequency or even stop it whenever full speed is unnecessary. That possibility is open only to static CMOS circuits—those capable of running at anything from dc to their maximum frequency—and not to dynamic ones, which lose data below a certain clock frequency.

The 82C85 clock-signal generator and controller chip ensures that a static CMOS system will dissipate the least power possible (see "Lowering Power Consumption in CMOS Systems," p. 186). The chip can run the system in four modes, which are, in the order of most to least power savings:

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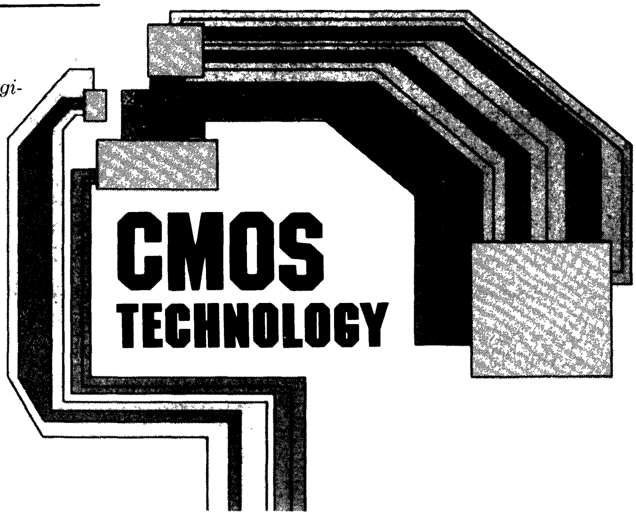
Walt Niewierski, who holds a BSEE from the University of Michigan, is technical marketing engineer for the Harris division. Before joining the company, he designed microprocessor-based test equipment at Ford Motors.

- The stop-oscillator mode, in which both the control chip's oscillator and the system CPU's clock stop.
- The stop-clock mode, in which only the CPU clock stops (to make it faster to restart the system).
- The slow mode, at much less than the system's maximum frequency. Here, power dissipation approaches standby leakage current levels, yet the CPU can still tackle such functions as periodically polling external sources and collecting data from them or sensing low battery conditions.
- The fast mode, at the system's maximum frequency.

The Static Clock Controller-Generator, as the 82C85 is formally called, has separate



CMOS Technology: Clock controller

signals for stopping and starting its oscillator or for blocking and unblocking an external frequency input. It can produce any clock frequency up to its maximum of 8 MHz, plus 1/256 of that frequency for its slow mode. Besides a crystal-controlled oscillator and clock generation logic, the chip contains ready synchronization and reset logic, as well as halt and decode restart logic. It comes in a slim-line DIP with 24 pins on 0.3-in. centers.

To guarantee crystal-controlled operation at 24 MHz, the chip uses a parallel, fundamental-mode crystal and two small-load capacitors. It generates both system and peripheral clock signals and for increased system flexibility, produces edge-synchronized 33% (CLK) and 50% (CLK_{50}) duty-cycle clock signals. Both of the latter are available simultaneously. Moreover the device can synchronize its clocks with 82C84A clock generator-driver ICs and with other 82C85s for use in multiprocessor systems. All of its inputs except three (X_1, X_2, and RES) are TTL-compatible over three temperature ranges—commercial, industrial and military—and the outputs are both CMOS- and TTL-compatible.

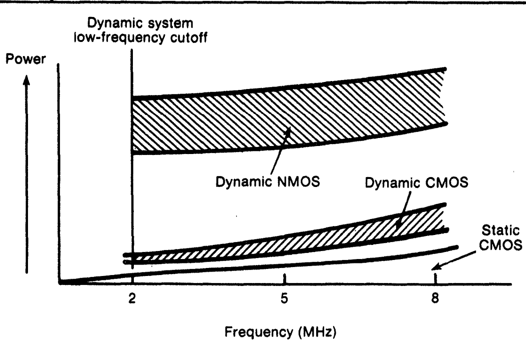
For ease of use with the 80C86/88 CMOS microprocessor family, the new chip is manu-

Lowering power consumption in CMOS systems

Only when static CMOS components are designed into a system can power consumption and package size be truly minimized. Consequently, as CMOS chips take over in architectures formerly built with NMOS devices, the distinction between static and dynamic circuitry takes on new importance.

Dynamic CMOS systems usually dissipate more power than static systems, in both the operating and the standby mode (see the figure). Even when their power dissipation seems the same for such operating conditions as maximum frequency and worst-case voltage, other factors tilt the balance in favor of the static device. A static circuit can run on any frequency from dc to its maximum. In contrast, if the clock frequency of a dynamic circuit falls below a specified minimum, data in the CPU or a peripheral is lost or altered. Therefore true standby operation (with the clock stopped) can occur only with a static CMOS design.

A static microprocessor system, like one based on the 80C86 or 80C88 CMOS devices, can be put in a standby mode by simply stopping the clock signals. The 80C86/80C88 family, for example, has an operating frequency range of dc to 5/8 MHz and retains data even if the external clock is stopped indefinitely. The system restarts when the CPU clock signal resumes.



But a static system design calls for several prerequisites. First, it requires static CMOS microprocessors and support circuits, which can operate and maintain data from standby (dc) to the maximum frequency of operation. Another need is for care in defining power-down situations, in which the processor and system clock frequencies can be controlled. Standby and operating modes should not be considered separate entities. Opportunities to stop the system clock must be evaluated carefully, as should transitions from the operating mode to standby and back again. Standby, low-frequency, and high-frequency operations then become complementary states, and the result is lower system power dissipation.

By anticipating circumstances in which the system can be stopped or run more slowly, the engineer can ensure that the proper standby and low-frequency hardware and software get into the initial system design and are not treated merely as afterthoughts. This increases efficiency and lowers the cost of implementing a static design. The degree to which the system's operating characteristics are altered is based on power, performance, and response requirements.

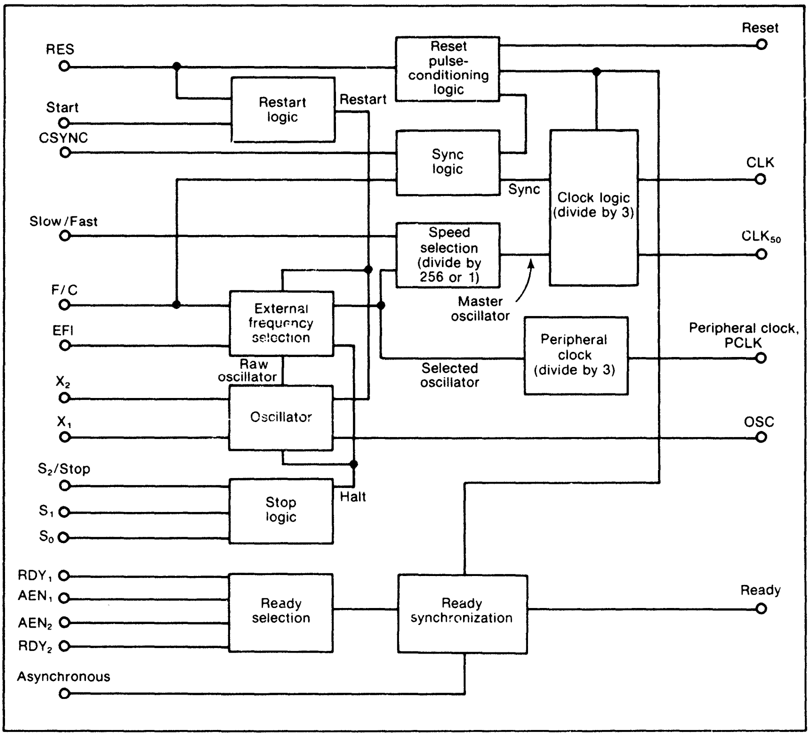
Because a static design results in lower power consumption, the system needs fewer supportive elements. For instance, fans and heat sinks can be eliminated, power-supply requirements reduced, and smaller enclosures used.

factured with the same CMOS process—a self-aligned junction-isolated process called scaled SAJI IV. However, it can be used with any static microprocessor or peripheral device. Its pinout is a superset of that of the 82C84A: pins 1 through 9 and 16 through 24 are compatible with pins 1 through 9 and 10 through 18, respectively. To emulate the 82C84A, pins 11 through 15 are tied high.

If power consumption must be held as low as possible and response times of 1 to 3 ms are acceptable, the device should be operated in the stop-oscillator mode. In this case, the chip gates off the system clock and then stops the crystal oscillator circuit. The External Frequency Input line (EFI) can be used instead of the oscillator by driving the Frequency-Control line (F/$\overline{C}$) line high.

With a 15-MHz crystal, which is needed for the operating frequency of a 5-MHz 80C86/88 system, the total operating current for the oscillator circuit ranges from 15 to 30 mA. Without those 15-MHz transitions in the oscillator circuit, the typical standby current falls to less than 50 μA (100 μA, worst case). A typical 80C86/80C88 system draws from 1 to 2 mA in standby.

Stopping the controller-generator is a simple



1. A single-chip clock controller and generator, the 82C85 generates clock signals for a microprocessor and its peripherals. Designed for static CMOS systems, the device controls system frequency to reduce power consumption.

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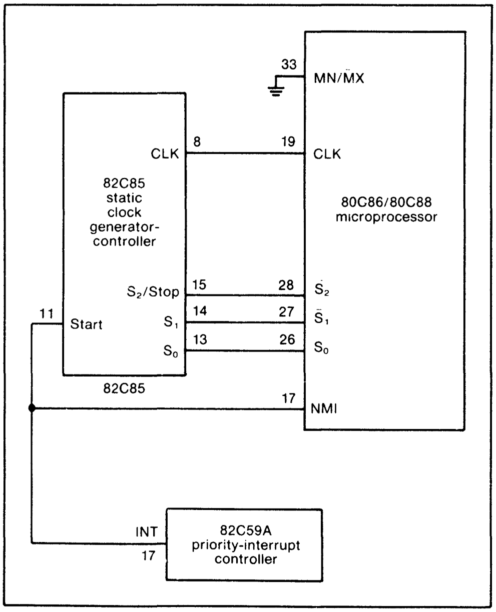
matter. Its three status lines—S_2/Stop, S_1, and S_0—are sampled on the rising edge of the CLK signal (Fig. 1). When these three lines enter the logic 011 state after a 111 state and when the Start line is also low, either the chip's oscillator will be stopped synchronously or its external frequency source will be turned off synchronously. In other words, the CLK and CLK_{50} outputs each stop in a logic 1 state after two additional complete cycles of the clock signal. The operation can occur in either the slow or the fast mode.

The 011 condition after a 111 on the three status pins indicates a software halt in the 80C86/80C88. This condition can be used in conjunction with the CPU's maximum-mode status lines—S_2, S_1, and S_0—to activate a software-controlled power-down that requires no external circuitry (Fig. 2).



2. A simple method for clock control uses the status lines of the 82C85 to detect a software halt. A software-controlled, power-down scheme of this sort requires no additional circuitry. MN/MX stands for Maximum mode.

If a power-down hinges on conditions other than a software halt, the device's S_2/Stop input can be used as a stand-alone command to stop the crystal operation. To do this, the S_0 and S_1 pins are connected to V_{CC}, and the S_2/Stop line is controlled through external logic.

Once the oscillator stops or is committed to stop, its restart sequence begins on either a high level on the Start input or a low level on the Reset input ($\overline{RES}$). A high level applied to the Start input disables the Stop input and overrides a Stop command in all instances. However, the stopped outputs—the peripheral clock (PCLK), CLK, CLK_{50}, and OSC—are held high by the 82C85 until a predetermined number of oscillator cycles have been internally counted. This automatically ensures proper oscillator startup, regardless of temperature, voltage, or the manufacturing source of the crystal. No external components are needed. After the internal count is complete, the high clock outputs restart cleanly with the correct phase relationship.

With an external frequency input (F/C high), the restart operation is slightly different. It occurs immediately after the Start line or the $\overline{RES}$ input has been synchronized internally. In this case, the synchronization ensures that the same four stopped outputs are in the proper phase relationship.

Stopping the clock

The stop-clock mode reduces power consumption but also affords an immediate response to a restart. The master oscillator continues to run while the CPU clock signal is gated off. In this mode the CPU and peripheral circuits are in the standby mode. It is up to the designer, however, to determine which peripherals should go into standby and which must remain active.

The stop-clock mode can be achieved with the 82C85. Here the OSC output connects to the EFI input, and the device is operated in the EFI mode, with F/$\overline{C}$ high. In other words, the chip's own crystal oscillator serves as the "external" frequency source. The S_2/Stop input gates the clock signal in the EFI mode, allowing the oscillator to continue to run. When Start is enabled, system restart begins immediately with the resumption of the CLK output. The clock can also be restarted by a reset or external interrupt.

The mode's primary advantage is that the system clock can be restarted within microseconds after it is enabled, thereby permitting an immediate response to interrupts or other signals that indicate a change in system activity. The clock signal is always active, and there is no waiting for oscillator stabilization.

Of course, the penalty for such instant response is higher power dissipation (Fig. 3). This dissipation comes from current drawn by the crystal oscillator circuit. Clock generator ICs like the 82C84A and 82C85 typically consume 1 to 2 mA/MHz when the crystal is in operation. With a 15-MHz crystal, the total operating current for the oscillator circuit ranges from 15 to 30 mA.

Slow clock cuts power

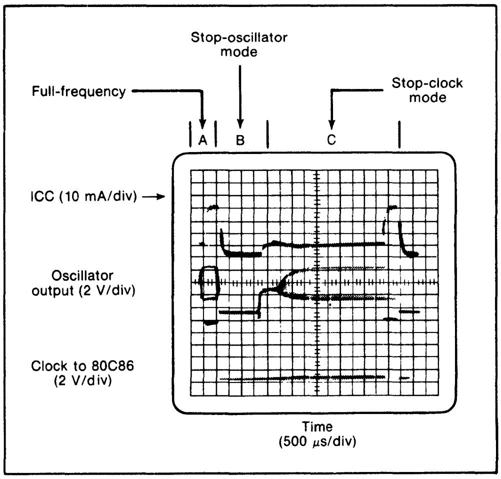
When continuous operation is critical but power consumption remains a concern, the controller-generator can put the system into the slow, low-frequency mode, which retards most operations and thus reduces the total power required. Data continues to flow properly, and the system responds to interrupt requests much faster than it would in the stop-oscillator mode.

The low-frequency divide-by-256 mode offers continual operation and performance of critical functions with a drastic reduction in power. The main oscillator continues to run, but the clock signal is divided by 256. The Slow and Fast input (SLO/FST) controls the frequency of the CLK and CLK_{50} outputs. When the line is high, the two outputs run at full speed—at one-third the crystal or external frequency. When the line is low, the frequencies of the two outputs are divided by 256. The PCLK output, however, remains at a constant frequency of one-sixth the oscillator or external frequency.

To be recognized by the controller-generator, SLO/FST must stay low for at least 195 oscillator or external frequency pulses—13 μs at a 15-MHz oscillator frequency. Otherwise glitches or noise spikes could cause undesirable frequency changes. To eliminate glitches on CLK and CLK_{50}, SLO/FST is synchronized to the high or low transitions of PCLK. To guarantee transition to full frequency, SLO/FST must be held high for at least three oscillator or external frequency pulses.

In the low-frequency mode, a 15-MHz system can be returned to full speed in 1 microsecond—a half PCLK cycle of 800ns plus 200 ns for three OSC or EFI cycles. The total delay in returning to full frequency operation is 50.2 μs. These times depend on the system's operating frequency, and they vary with the main oscillator frequency.

At a 5-MHz system clock—15-MHz crystal—the final CPU clock frequency in the slow mode is approximately 20 kHz. At that reduced speed,



3. System power levels vary significantly, depending on the operating mode of the clock. From full frequency operation (point A), dissipation is lowest in the stop-oscillator mode (point B) and next lowest in the stop-clock mode (point C). Note the differing restart response times. The crystal start-up time is typically 1 to 1.5 ms, and the CPU clock signal is gated on—at point B—after the crystal oscillator restarts, ensuring that the oscillator frequency is stable before it is reapplied to the CPU.

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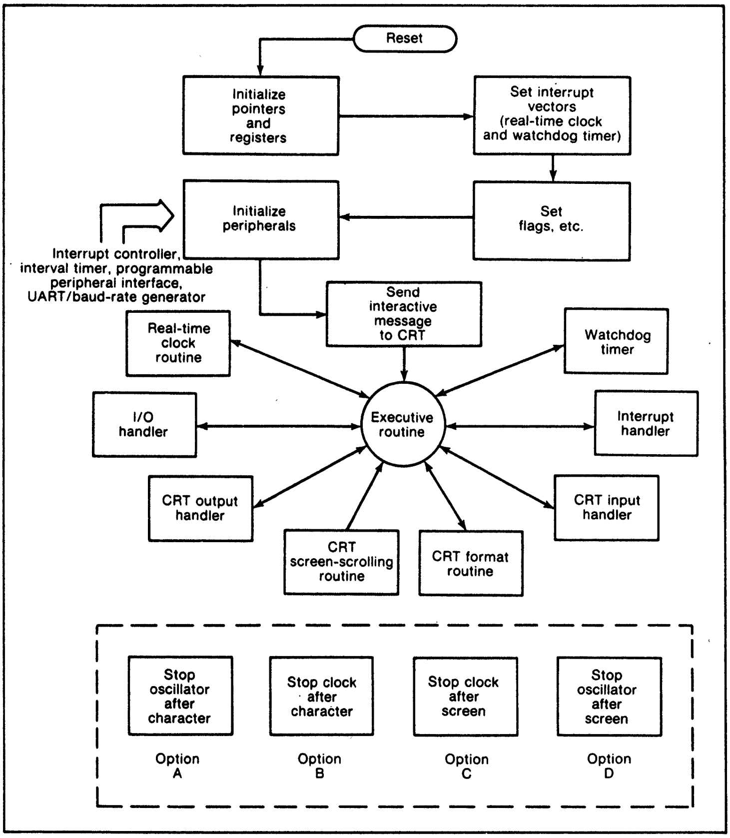
the power dissipation of the CPU and peripheral circuits is very close to that drawn under standby current conditions and results in nearly the same power reduction as in the stop-clock operation.

Since the frequency of PCLK is not reduced when the 82C85 is in the slow mode, a real-time clock can be implemented with an 82C54 programmable interval timer driven by PCLK. Chip count falls, because no need exists for a stand-alone real-time clock circuit. Further, no additional crystal oscillator is needed for a UART, since it can run from PCLK.

CPU dissipation is reduced in the low-frequency mode. The operating power for 80C86/80C88 microprocessors, for example, is 10 mA/MHz of clock frequency. At 20 kHz, the average operating current of these microprocessors drops to 200 μA. Adding 500 μA of standby current brings the total current to 700 μA—a sharp contrast with 50 mA at a 5-MHz operating frequency. However, the controller-generator will still run with a high-frequency crystal that consumes between 15 and 30 mA.

Low-frequency operation is a compromise between the stop-oscillator mode and full-speed operation. It requires a minimum of



4. In a CRT control flowchart, the executive routine can select either the stop-clock or the stop-oscillator mode, depending on the system's power and response requirements. If power consumption is the primary consideration, using the stop-oscillator mode to halt the CPU proves the best choice.

hardware and offers a reasonable tradeoff between power requirements and speed of response.

Power-down through software

In an interrupt-driven system—for example, one for updating information on a CRT—the software executive idles most of the time while waiting for an interrupt from an external source. When it recognizes the interrupt, it allows the task to be completed and then returns to the idle state to await the next sequence. With the controller-generator and the proper software, power in such a system can be regulated. In addition the user gets software and hardware options not previously available.

The system and CPU can be stopped periodically at intervals based on the data transmission rate (Fig. 4). While data travels to the screen over a serial channel, the system can drop into a power-down state until more data can be loaded from the CPU. The major concerns are how often to stop the operation and the impact on power and performance.

Two options significantly affect power and performance: stopping the system after each character is transmitted or stopping the system after each screen refresh. If power consumption is paramount, the choice is to stop the processor on the main loop of the executive routine. This allows the CPU to enter the stop-oscillator mode after a character is sent to the CRT. An interrupt—one indicating that the transmitter buffer register in the UART is empty—takes the system out of the stop mode and restarts the oscillator. After the crystal oscillator stabilizes and the clock is restored to the CPU, the interrupt is serviced.

How the clock oscillator start-up time affects display performance

Baud rate (baud)	Data transmission time (ms)	Oscillator start-up time (ms)	Nominal impact on transmission time per character (ms)
19,200	0.52	3	−2.48
9600	1.04	3	−1.96
4800	2.08	3	−0.92
2400	4.17	3	+1.17 (no speed impact)
1200	8.33	3	+5.33 (no speed impact)

Such a system requires a separate crystal oscillator for the UART and for a hardware real-time clock if periodic scrolling is required. That approach consumes less power than stopping the system after each screen refresh. With the main system oscillator stopped, the only power dissipation is in the UART's crystal circuit—typically 1 to 2 mA.

Nevertheless low power comes at the expense of response time. Since the crystal oscillator must be stabilized before the CPU can restart, data cannot be transmitted between the time the interrupt for more data occurs and the oscillator becomes stable. The start-up time for crystal circuits can be from 1 to 2 ms or longer, but each application should be evaluated individually.

The oscillator start-up time affects the data transmission time. A fixed start-up time of 3 ms is assumed for various baud rates. As the baud rate increases, the start-up time slows the effective transmission rate (see the table). For standard rates above 2400 baud, data transmission is completed well before new data is loaded, resulting in varying degrees of so-called system dead time.

The second option—stopping the oscillator after each screen refreshing—has no effect on the system's response time. With the oscillator and system clock running constantly while the screen is being updated, the CPU can respond immediately to requests for more data. This method, however, dissipates more power because the oscillator runs longer.

If scrolling is called for, a much higher current is needed, since the oscillator must continue to deliver a clock signal to the real-time clock or other circuit used for watchdog timing functions.□

Saving Power in CMOS Systems Design

WALTER J. NIEWIERSKI, Harris Semiconductor, Melbourne, FL

Designed to operate in harsh environments over wide temperature ranges, CMOS reduces system power, size, weight, and cost. Systems can be battery-powered and enclosures can be environmentally sealed. Using static CMOS makes some circuits work even better.

Because CMOS power dissipation is directly proportional to operating frequency in microprocessor-based static CMOS systems, the slower CMOS is switched, the lower the power dissipation. The ability to slow or stop the system clock gives the designer direct control over system operating power. Stopped, power consumption drops to microwatts.

Static microprocessors, such as the Harris 80C86 and 80C88, and static CMOS memories require no active clock signals, consume no active power, and can be in a standby mode indefinitely.

Dynamic CMOS devices require a constant clock or refresh signal to maintain valid data in the chip, and are not discussed in this article.

Clock mode options

Four basic operating modes are used in static CMOS system design:

- FAST—all clocks and oscillators operate at the maximum frequency—highest power dissipation;
- SLOW—system CPU clocks are slowed (to provide a continual operation) while the main clock oscillator continues to run at the rated frequency—reduced power;
- STOP-CLOCK—the system CPU clocks stop while the main clock oscillator continues to run—reduced power; and
- STOP-OSCILLATOR—both the system clocks and the clock oscillator stop—minimum power condition.

Reducing average power

A CMOS system running at full speed uses approximately 10 percent of the power of an equivalent NMOS system. Static CMOS system design techniques can achieve additional power reductions of 35-75 percent.

In STOP-OSCILLATOR, the CPU requires less than 500 μA, the 82C85 static clock controller/generator less than 100 μA, and peripheral and memory circuits less than 10-50 μA. In all, a typical static CMOS system can stand by drawing less than 1 mA.

In STOP-CLOCK, CPU, memory, and peripheral currents are the same as in STOP-OSCILLATOR but the 82C85 current jumps from under 100 μA to 15-40 mA. The significant increase is due entirely to the crystal oscillator switching currents.

In SLOW, the system operates at a very low frequency. CPU, memory, and peripheral power increase slightly due to the 82C85.

Lower power yields longer life

A distributed processor system has three subsystems all running at the maximum frequency and drawing current from a one amp-hour battery. The total current requirement is 198 mA and the battery life is 5 hours.

By analyzing tasks and projecting individual subsystem run-times and modes, decisions can be made about which operating modes can be used and when. Since manipulating operating modes and frequencies reduces system power, hardware and software control to switch the system operating modes can be designed into each.

For example, System A, the host, is the workhorse; it runs full speed 75 percent of the time, consuming 66 mA. In STOP-CLOCK, it consumes 14.8 mA and does most of the data handling and manipulation. The system draws 53.2 mA.

System B runs full speed 40 percent of the time. When it's not doing a specific task, it can be shut down completely. Instead of running at 5 MHz, the maximum frequency was set at 4 MHz. This is significant because the 20 percent lower maximum frequency automatically means a 20 percent power reduction at full speed. System B draws a total of 21.6 mA.

Finally, System C continuously monitors specific conditions in the overall system, i.e., pressure level, low battery indicators, etc. Hence, the need for SLOW operation. When a monitored state requires attention, the system revs to full speed and performs as necessary. System C uses 33.0 mA

Based on the data above, the total current for all three subsystems' operation is 107.8 mA. Compared to the constant full speed operation of the original system, this 45 percent reduction in current consumption increases the estimated lifetime of the battery supply approximately 80 percent.

Examining individual subsystem tasks, their priorities, and how often or how fast each job must be performed allows development of a matrix of maximum subsystem frequencies and operating mode options. Intelligent system design must include the hardware control logic driven by well-defined software, and an established set of algorithms for determining allowable operating mode situations.

Support circuits for static design

Circuits such as the 82C85 static clock controller/generator circuits provide control of static CMOS system operating modes and support full speed, slow, STOP-CLOCK, and STOP-OSCILLATOR operation. The 82C85 can also be used for general purpose clock control.

For static system designs, separate signals are provided on the 82C85 stop (S0, SI, S2/STOP) and start (START) control of the crystal oscillator and system clocks. A single control line (SLO/FST) puts the 82C85 and the rest of the system into the slow mode or lets it run at full speed. Automatic CPU MAXimum mode software HALT instruction decode logic in the 82C85 allows system control via software without additional hardware.

Placing control is critical

The key to optimizing individual subsystem power and performance is to provide local control for each subsystem clock signal. The host system should have a means of controlling the operation of the subsystems under certain conditions (emergency power situation, fault at system level requiring system shutdown, etc.). With an 82C85 in each static subsystem and a logical interface to the host computer, both local and remote control are performed.

Based on current monitored conditions, either the subsystem CPU or the host CPU determines each subsystem's operation in any of the four static modes. Once these decisions are made, the resident 82C85 controls the subsystem's clock.

In this example, how control can exist at both the remote and local levels in a distributed system is discussed. Using a parallel interface, the host can send a command to all subsystems at once. Dedicated decoders in each subsystem decode the command and provide the appropriate interrupt. Upon receipt of the interrupt command, the subsystem CPU determines which mode to enter.

The decoder outputs are dedicated to specific commands. Y1-Y2 control

Subsystem B and Y3-Y5 command Subsystem C. By splitting the command outputs, a single three-line interface controls both subsystems without additional enabling or decoding. Y6 and Y7 are common to all subsystems.

These types of situations must be considered during the initial design phase. Host commands from the 82C59A Interrupt Controller, such as FAST, can be masked individually, allowing a subsystem to override the host in cases where the host tells the subsystem run fast but the subsystem determines slow is preferred. Time is wasted servicing a host SLOW interrupt when the subsystem is already slow. More power can be wasted when a stopped subsystem must be restarted (typically FAST) to service a host STOP.

Hardware control is easy

In the MAXimum mode (typically used in large system design), the CPU's output status signals (MEMORY READ, I/O WRITE, etc.), indicate the operation being executed.

In HALT, the CPU stops operation, gives up the system bus, and waits for a signal to restart—a perfect time to enter into an alternate operating mode.

When the 82C85 status inputs (S0, SI, S2/STOP) are connected to the CPU status output signals, it automatically recognizes the HALT status sequence. Depending upon the previously chosen state of the F/C (EFI/crystal) input, the 82C85 will enter either STOP-CLOCK or STOP-OSCILLATOR.

If the CPU is used in MINimum, the 82C85 S2/STOP input is controlled by a single I/O line from a peripheral device. Connecting S1 and S0 to the +5 V line (VCC) and switching S2/STOP from high to low signals STOP. The 82C85 responds as described in MAXimum.

A third alternate mode is SLOW. In this mode, the system clock frequency is reduced to decrease system power. While the CPU static design allows operation between dc and 5 MHz, a reduced frequency is used for SLOW. The SLOW frequency equals the main oscillator frequency divided by 768.

SLOW is controlled via the SLO/FST input, itself controlled by an I/O port or other control logic. When this line is held low for 195 OSC/EFI cycles, the 82C85 will output system clocks with a reduced frequency. This 195 OSC/EFI clock cycle restriction reduces the chance that system noise will cause a mode change. To return to full speed operation, the SLO/FST pin is held high for at least six OSC/EFI cycles.

To restart a system, START is output to the 82C85. When the START input becomes active, the 82C85 will restart its crystal oscillator or the system clocks. Once the clock signals are stabilized and synchronized, they're output to the CPU and system operation begins.

The START input is connected to the system's interrupt scheme or gated by a flag signal. When a significant external event occurs, a START command is issued, and the system restarts.

Response time is important

Operating mode decisions are based upon two key criteria: power requirements and system performance. Each mode has its own power dissipation characteristic. Typically, power is the reason to choose an operating mode. Restart time and its impact on system performance must be considered.

In SLOW or STOP-CLOCK, response will be faster than in STOP-OSCILLATOR mode. The main 82C85 oscillator continues to run, providing instant or constant response to a system command.

The slow response when returning from the STOP-OSCILLATOR mode is due to the time necessary for the main oscillator to restart. In the STOP-OSCILLATOR mode, the 82C85 must wait for it to stabilize before allowing a clock signal to be sent to the CPU. This restart time typically runs from 0.5-3 msecs, compared to 100-400 nsecs for the STOP-CLOCK and SLOW modes. This extra time, along with 82C85 synchronization circuitry, ensures clock signals meet system and device specifications.

From STOP-OSCILLATOR, the 82C85 insures a valid CPU clock restart sequence in three ways. First, the hysteresis of a Schmitt trigger input is used at the crystal input to prevent the oscillator's signal from proceeding past that point until its amplitude has reached a predetermined level.

When the oscillator signal enters the 82C85, the clock outputs remain inactive while an 8K counter is incremented through the entire count sequence. During this sequence, harmonic and irregular cycles in the crystal oscillator's start-up can't be used to form the CPU clock signal. When the count is complete, internally developed system clock signals are negative-edge synchronized and released to the system.

Trade-off: power vs speed

In designing a system, each mode should be evaluated not only for power but whether the mode's response time allows completion of the task in the given time period. (Examples: STOP-CLOCK or SLOW require 20-40 times the current of STOP-OSCILLATOR and response time to a restart request is two orders of magnitude faster.)

If an input requiring service is received by a subsystem at a rate of 1 KHz, the system responds in 10 msec intervals. Since the oscillator restart time is in the 1-3 msec range, (allowing 7-9 msecs for servicing the interrupt request), in this case the STOP-OSCILLATOR mode is a valid option.

If the frequency of the interrupting input increases to 10 KHz, then interrupts would require service at 1 msec intervals. This isn't enough time to guarantee oscillator restart and STOP-OSCILLATOR operation would be ruled out. In this case, STOP-CLOCK or SLOW mode operation should be considered. Their response time of 100-400 nsecs allows system restart and servicing of interrupts within the 1 msec intervals.

Another area where a conscious decision to stop the system can be made is during A/D data conversions. When a command is given to an ADC to begin the conversion process, data may not be available for a length of time (20-70 μsecs). This time period depends on the converter's speed, the sample-and-hold structure, and the accuracy.

If the system is doing only this task, it can be stopped or slowed during the conversion delay time. A "conversion complete" signal from the ADC status output generates an interrupt request to restart the system. The main concern becomes which mode to use? This decision is based on the conversion time of the ADC and the response time of the system. If it's determined that a system shouldn't stop, then choose SLOW. Its response time is similar to STOP-CLOCK with only slightly higher power requirements.

Keep your system quiet

CMOS can be a source of system noise. Since current flows only when a CMOS circuit switches, these switching transients result in noise on power supply and signal lines. The faster CMOS switches, the more noise.

Static system operating modes reduce system noise. With the system running at full speed, the +5 V line (VCC) is subject to significant noise.

In SLOW the VCC noise level goes down. Since the high frequency crystal oscillator is running, the average noise level remains relatively consistent. The frequency of the large noise transients is reduced since the main system clock frequency is lower and most system components switch at a lower rate.

The large current spikes occur with less frequency. In STOP-CLOCK, a similar situation seen in SLOW exists. The system isn't running but the oscillator continues and the general noise level remains high.

When the system goes into STOP-OSCILLATOR, all clocks and oscillators stop switching and the VCC noise drops to zero. □

Microprocessor Family Turns to Low-Power CMOS

The 80C86 microprocessor adds a proven design and low power to high performance defense systems.

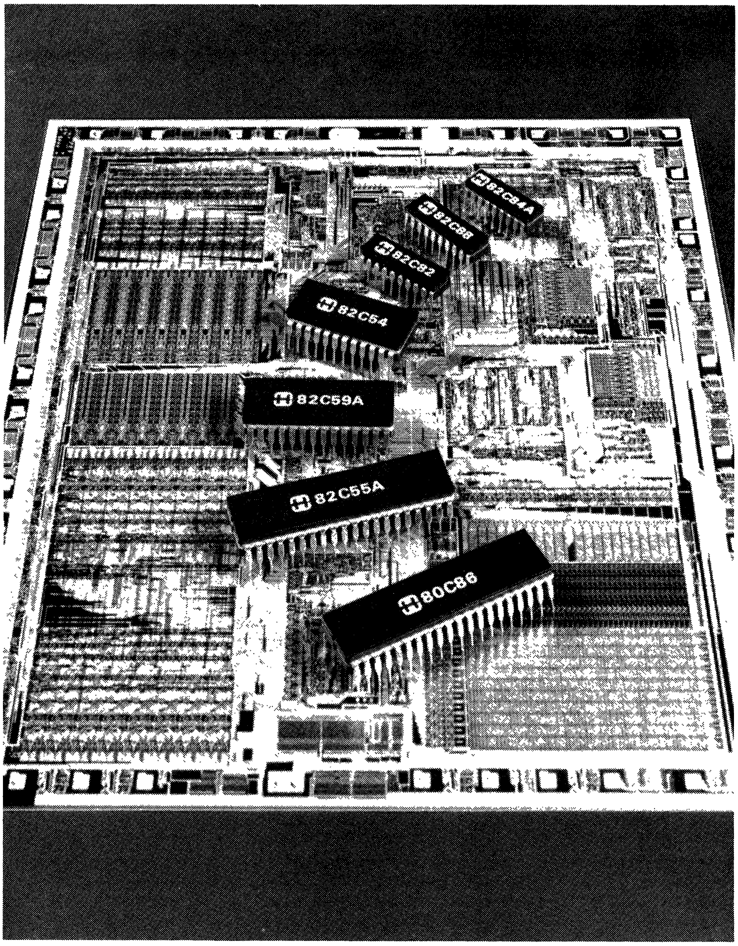
By Walter J. Niewierski

Next Month, Part II in this two-part series on microprocessors will examine the transition of the low-power 80C86 family to industry standard leadless chip carrier packages.

Walter Niewierski is a technical marketing engineer with Harris Corporation's Semiconductor Group, CMOS Digital Products Division, P.O. Box 883, MS 54-130, Melbourne, FL 32901.

CMOS equivalents of existing high performance circuits offer obvious advantages to the military system designer—allowing immediate reductions in critical system operating power, reduced power supply requirements, sealable enclosures, and lighter, higher density packaging. System reliability is improved due to lower ambient and junction temperatures and the high radiation tolerance of the CMOS process. In the past, however, this power reduction usually came at the expense of lower system performance.

The new 80C86 products from Harris Semiconductor have been designed especially for high performance military systems. Initial device specifications for the product line include 5 MHz operation over the full −55°C to +125°C temperature range, with selected products available in 8 MHz versions. Upgrades of all circuits to 8 MHz compatibility are planned. MIL-STD-883B processing allows full implementation of CMOS products in military designs.



Harris Semiconductor will begin delivering *the 80C86 mil-spec CMOS microprocessor and the six support chips by August. Additional parts will follow into fourth quarter 1983 to complete the family. The 80C86 is an exact replica of the NMOS 8086 processor, and takes advantage of existing software and support tools.*

80C86 Functional Compatibility

Full functional compatibility with existing 8086 NMOS/bipolar equivalents is provided in the 80C86 family. Programs that test original source devices are being used to verify functionality and compatibility. In-system testing has been done by both the Harris Semiconductor CMOS Applications Group and selected external customer sites to verify functionality in a real system, real time environment—providing an additional level of compatibility assurance.

Product compatibility with existing industry standard devices and development systems can immediately improve system performance with respect to power and reliability. Life spans of existing hardware and software designs can be extended by providing direct low-power, high performance upgrades for existing 8086-based systems.

The unit's hardware interface and instruction set are compatible with proven design and development tools. Software developed for projects using the 8086 can be used directly with the 80C86 family, reducing the manpower investment and resulting in decreased development time and cost. With standard software (Ada, Jovial, etc.) for military, defense, and aerospace applications, this software compatibility can result in significant savings in new and existing projects.

CMOS 80C86 Microprocessor Family

Part Type	Description	Scheduled Availability
80C86	CMOS 16-Bit CPU	Aug '83
82C54	CMOS Programmable Interval Timer	Now
82C55A	CMOS Programmable Peripheral Interface	Now
82C59A	CMOS Priority Interrupt Controller	Now
82C82	CMOS Octal Latch	Now
82C84A	CMOS Clock Generator/Driver	Now
82C88	CMOS Bus Controller	Now
HD-6406	CMOS PACI (UART/BRG)	Q3CY83
82C89	CMOS Bus Arbiter	Q4CY83
82C83 82C86 82C87	CMOS Inverting Octal Latch CMOS Bus Transceiver CMOS Inverting Bus Transceiver	Q4CY83

Worst Case Design for Defense Applications

As with all system components, CMOS devices best perform within their specified operating conditions. The problem facing the designer is one of insuring these system operating conditions will not degrade device performance beyond the limits imposed by the design. Devices guaranteed to operate to specifications over "worst case ranges" make this task easier (for example, parameter limits guaranteed over the full temperature range and propagation delays guaranteed at realistic 100 to 300 pF capacitive loads as opposed to 15 to 45 pF). All AC parameters are tested and guaranteed with worst case specified loads on the appropriate outputs.

The 80C86 product line has been designed for military applications; specific operation goals over the military temperature range were established and maintained throughout the design process. Performance is also guaranteed at worst case conditions, including operation over the power supply voltage range and at the maximum rated loads. These worst case specifications insure reliable operation under adverse conditions such as extreme temperature variations, fluctuating power supply level, and heavy output load.

Limits specified for the 80C86 family AC and DC parameters reflect maximums and minimums over the entire military (−55°C to +125°C) temperature range. Capacitive loads are 100 to 150 pF for standard peripherals and 300 pF for the 82C82 and 82C88 bus interface devices, which interface directly with the system bus. These guarantees insure a system is designed to worst case specifications; no performance degradation calculations for guaranteed parameters will be needed during initial design; and, the system will operate properly over the full specified operating ranges.

Low-Power System Application

The 80C86 CPU, operating in the maximum mode, is the focal point in the control module for flight navigation. Non-inverting octal latches (82C82) and transceivers (82C86) provide the address/data latching and buffering for the local bus. The 82C88 CMOS bus controller provides the control signals for the on-board memory, both CMOS RAM and non-volatile CMOS PROM, and for the peripheral circuits.

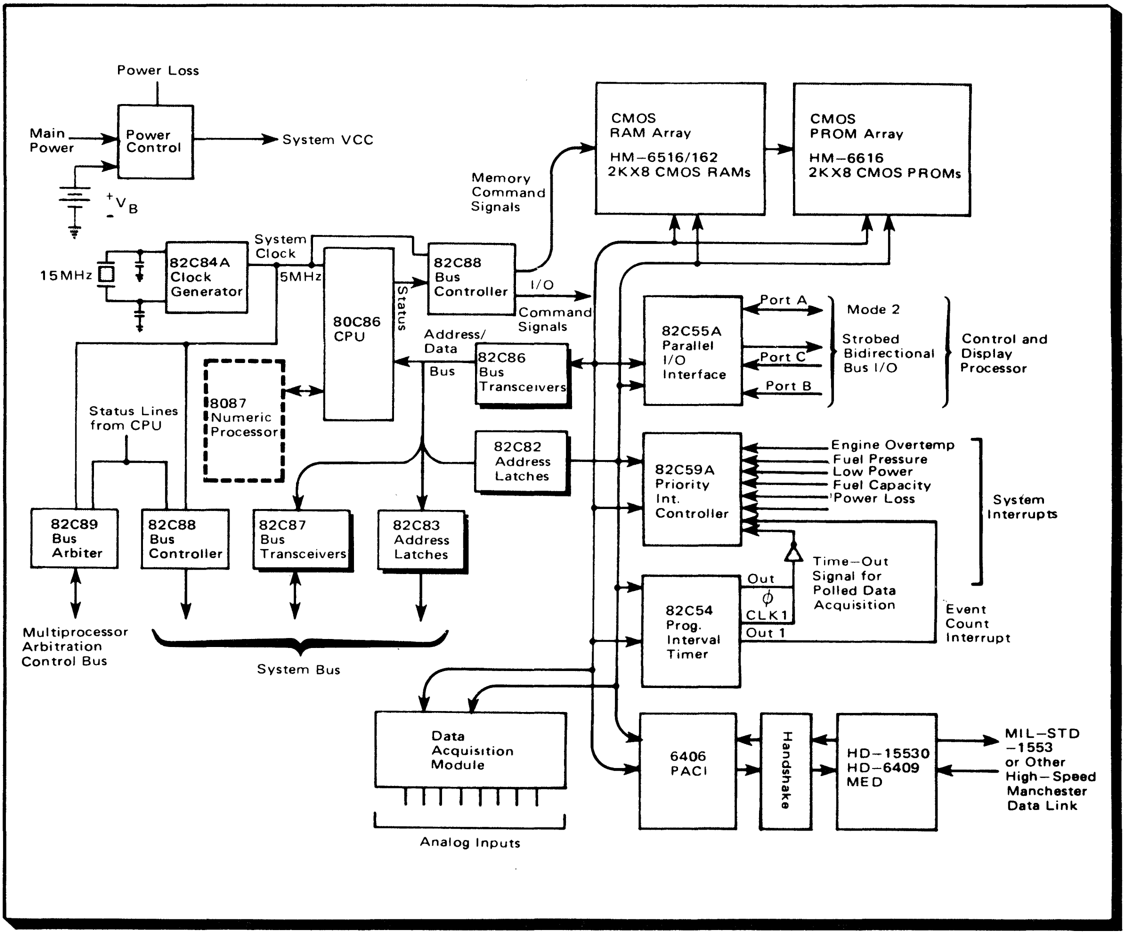
CMOS Memory Options

CMOS memory circuits offer the designer several options. The HM-6516, a 2K x 8 CMOS static RAM, offers a low operating power of 10 mA/MHz, maximum, for military applications. Access times as low as 120 ns make this device compatible with many high-speed applications. Where increased performance is necessary, the HM-65162 asynchronous 16K CMOS RAM can be used with an access time of 70 ns, maximum.

CMOS fuse link PROMS are used in this application because of the high reliability requirements of military systems. The long-term data retention characteristics of polysilicon fuses insure reliable operation in extreme environments. The low power (13 mA/MHz for the 16K density CMOS PROM) and 150 ns access time provide the performance needed for this generation of CMOS systems.

Multiple CPUs

Expanding system capabilities beyond the level available with a single



A typical flight control computer configuration *based on the 80C86 microprocessor family is a full 5 MHz design. The device can also operate at lower speeds to provide even greater power savings. The 80C86 can directly replace the NMOS 8086 in existing designs.*

processor can be accomplished in several ways. The addition of another CPU subsystem, along with the appropriate interface to allow common access to data, significantly improves system throughput. To accommodate this multiprocessing scheme, the 82C88 bus controller and the 82C89 bus arbiter provide the control and arbitration for the system bus. Inverting latches (82C83) and transceivers (82C87) meet the necessary functional compatibility for existing industry standard multiprocessor bus systems.

If there is no need to expand beyond a single board or enlarge to a multiprocessor system, the 80C86 can run in the Minimum mode, where decoded memory and I/O signals are available from the processor. This type of configuration eliminates the need for the 82C88 bus controllers and the additional multiprocessor interface circuitry.

Mixing Technologies

Another way to increase system throughput, especially in cases where arithmetic functions and numeric data manipulation are critical, is to add an 8087 numeric coprocessor to the system. Although not available in CMOS, the device can be used in a CMOS 80C86 system, providing the increase in power dissipation is acceptable.

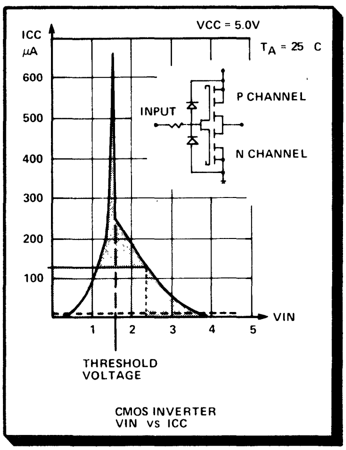
The addition of the NMOS 8087 to the otherwise all-CMOS 80C86 system and the subsequent mixing of technologies is possible with the full TTL compatibility present on the 80C86 products. This compatibility on both inputs and outputs eases interfacing to NMOS and bipolar circuits. CMOS output drivers, along with the dual VOH specification, guarantee operation at CMOS and TTL logic levels.

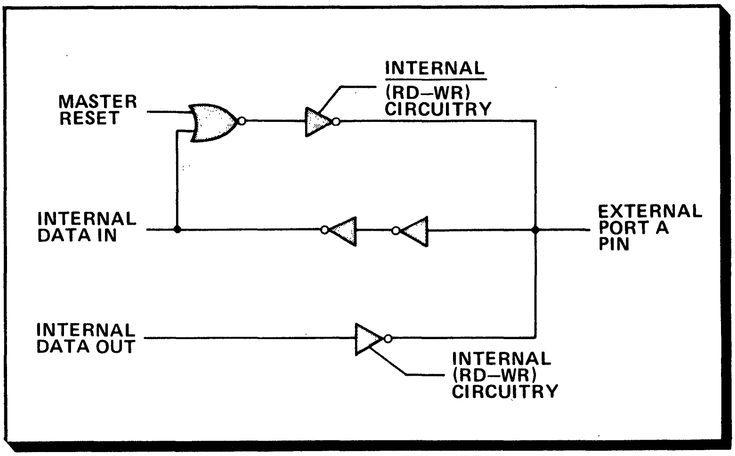
Mil-Std Bus

When data communication between subsystems is desired, but not necessarily at parallel bus speeds, a MIL-STD-1553 or alternate protocol Manchester-based serial bus can be used. The addition of an HD-6406 programmable asynchronous communication interface (PACI) and an HD-15530 Manchester encoder-decoder

(MED) form a high-speed serial link between several remote systems. Standard eight-bit data transfers can be accomplished in the non-1553 bus applications by using the military version of the HD-6409 Manchester encoder-decoder—which allows more freedom than the MIL-STD-1553 bus for formatting the serial data.

The HD-6406 provides the UART parallel-to-serial/serial-to-parallel conversion function and bit rate generator in a single 40-pin package. A 28-pin version (82C52) will also be available for higher packing density applications. The HD-6406 functions are fully programmable through a microprocessor-compatible bidirectional bus, which has a maximum serial data rate of one megabaud (asynchronous transmission with a 16X clock). The HD-15530 (1.25 M-bit/sec) and the HD-6409's (1 M-bit/sec) maximum data rates can fully support a one M-bit serial bus interface for military applications.





***Both the 80C86 and the 82C55A** use this on-chip "bus-hold" circuitry to provide valid input voltages to specific inputs without using external resistors.*

Peripheral Monitor and Control Functions

Several peripheral functions monitor system I/O and timing control. The 82C55A programmable peripheral interface can be used for display control or for information passing between subsystems, using the bidirectional handshaking mode. Upon RESET, the 82C55A port pins become defined as inputs. If these inputs are not used or will eventually become outputs, they have no driving source and are in an undefined, or "float," condition.

Undefined input voltage levels are forbidden in CMOS system design. Undefined input states allow the input circuitry to "float" within the devices' active regions. Unfortunately, floating CMOS inputs tend to migrate toward the threshold voltage and increase ICC substantially. All CMOS inputs, if unused, must be tied to VCC or GND to avoid oscillation and high ICC conditions.

Pull-up/pull-down resistors are the most common method for defining CMOS inputs when no driving source is present. But, this technique has several disadvantages. Additional components (resistors) are necessary, which increase production costs and reduce overall reliability. Higher power operation can actually occur when using pull-up/down resistors. Since the driving circuit must supply the current needed when switched to the opposite state of the pull-up/down resistor, the result can be a significant increase over normal CMOS input leakage current levels of 1 μA.

Bus-Hold Circuitry

To avoid the need for external resistors and eliminate the high power effects of floating inputs, the 82C55A, along with the 80C86 CPU, uses on-chip "bus-hold" circuitry to provide valid input voltages to specific inputs; this is important when there is no driving source (i.e., a no-connect or a driving input that goes to a high impedance state). The bus-hold circuits maintain these pins at a Logic One level internally and externally until they are defined as outputs or are overdriven by an external source.

An external driver must be capable of supplying 300 μA minimum sink or source current at valid input voltage levels in order to overdrive the bus-hold circuits. Since this circuitry is active and not a passive pull-up resistive-type element, the 82C55A, standby current is kept to 10 μA, maximum.

System needs and overall compatibility dictated the placing of bus-hold circuits on specific devices. The 80C86 CPU has bus-hold devices on selected pins (AD0-AD15, etc.), which are common to the local bus—This eliminates the compounding of the overdrive current necessary if all 80C86 family members had bus-hold circuitry, and keeps all current requirements within TTL/LSTTL capabilities.

Gated Inputs

The 82C82 octal latch also has specialized input circuitry to minimize power dissipation and help eliminate the need for external resistors. Gated inputs minimize the effects on the ICC from switching and undefined inputs. This gating function, initiated by the falling edge of the strobe (STB) input, disconnects the input inverter from the VCC by turning off the upper P-channel (Q1) and lower N-channel (Q2). Thus, there is no current path, other than leakage, between VCC and

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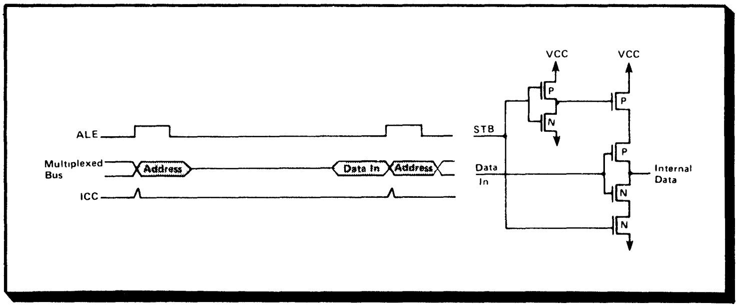
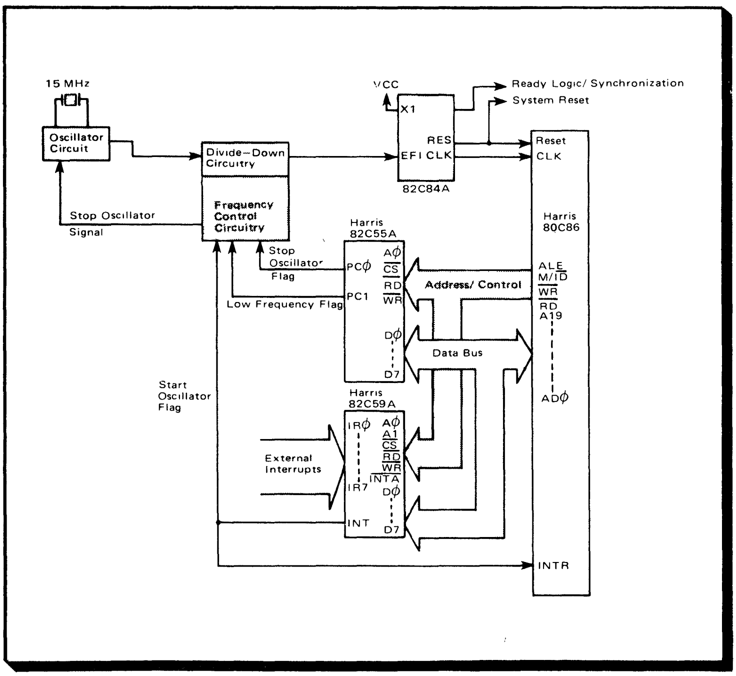
ARTICLE REPRINTS



Gated inputs on the 82C82 octal latch *eliminate extraneous current spikes due to input conditions unrelated to latch operation. While data is latched, floating inputs can be directly connected to the 82C82 inputs without using pull-up resistors.*



For power critical applications *where power is reduced to the point that even full-time operation at reduced frequency is not desirable, the 80C86's static circuitry allows the clock to be stopped.*

GND during input transitions when data is latched in the 82C82. Internally, logic states are held valid by the feedback logic signal in the circuit's latch section.

Input gating also isolates the driving source from the internal circuitry. Invalid logic states from floating inputs cannot be transmitted to succeeding stages when the inputs are turned off, eliminating the need for pull-up resistors when data is latched.

In an 80C86 system, the STB input is driven by an ALE (address latch enable). At 5 MHz, the high pulse width of the ALE is 98 ns or approximately 15 to 20 percent of the bus cycle period. Therefore, 82C82 inputs are disabled 80 percent of the time. During this time, ICC transients from input switching are eliminated, resulting in a lower operating current.

Polled or On-Demand Data Sensing

The 82C59A priority interrupt controller and the 82C54 programmable interval timer manage system interrupt and polling control functions. Two methods, used either separately or concurrently, are available for controlling the system sequencing of data acquisition. Polled acquisition or interrupt-driven data taking can be accomplished with the circuit described.

The 82C54 timer can be programmed, using single or multiple 16-bit timers (three per package), to provide an input to the 82C59A interrupt controller and cause execution of a data acquisition software routine. This procedure can be repeated by using the 82C54 in the rate generator mode (Mode 2), inverting the signal, and inputting it to the 82C59A programmed for edge-triggered inputs.

If certain functions must be executed only every Nth cycle, the 82C54 Timer 0 output (OUT 0) can be fed into the clock of Timer 1 (CLK 1). Timer 1 can be programmed to operate as an event counter (Mode 0—interrupt on terminal count) and interrupt the 82C59A every Nth count.

The 82C59A is also used for control of other external interrupts such as emergency conditions like engine over-temperature, pressure high, low, and other on-demand situations. If desirable, the repeated interrupt for polling purposes can be disabled by using the 82C59A's interrupt masking ability, which only allows generation of critical situation interrupts.

The 82C59A interrupt inputs can be prioritized. When both polled and on-demand sequences are used concurrently, the on-demand emergency situations would be considered highest priority.

Tailoring Low-Power System Operation

Several circuit design techniques can be valuable in examining low-power operation at the system level. CMOS is only a first step. Significant reductions in system-level power consumption can be realized if proper design approaches are taken.

In an aircraft situation, power is not normally a problem. If, however, the microsystem power fails independent of the main aircraft power, full

CMOS/NMOS/Bipolar Parametric Comparison

	CMOS 80C86	NMOS 8086	CMOS 82C54	NMOS 8254	CMOS 82C55A	NMOS 8255A	CMOS 82C59A	NMOS 8259A	CMOS 82C82	Bipolar 8282	CMOS 82C84A	Bipolar 8284A	CMOS 82C88	Bipolar 8288
VIH	2.2V	2.0V	2.2V	2.0V	2.2V	2.0V	2.2V	2.0V	2.2V	2.0V	2.2V	2.0V	2.2V	2.0V
VIL	0.8V	0.8V	0.8V	0.8V	0.8V	0.8V	0.8V	0.8V	0.8V	0.8V	0.8V	0.8V	0.8V	0.8V
VOH	3.0V/ VCC 0.4V	2.4V	3.0V/ VCC 0.4V	2.4V	3.0V/ VCC 0.4V	2.4V	3.0V/ VCC 0.4V	2.4V	2.9V	2.4V	VCC 0.4V	2.4V	3.0V/ VCC 0.4V	2.4V
IOH	-2.5mA/ -100μA	-400μA	-2.5MA/ -100μA	-400μA	-2.5mA/ -100μA	-400μA	-2.5mA/ -100μA	-400μA	-8mA	-5mA	-2.5mA	-1mA	-8mA/ -2.5mA	-5mA
VOL	0.4V	0.45V	0.4V	0.45V	0.4V	0.45V	0.4V	0.45V	0.4V	0.45V	0.4V	0.45V	0.5V/ 0.4V	0.5V
IOL	+2.5mA	+2.5mA	+2.5mA	+2mA	+2.5mA	+2.5mA	+2.5mA	+2.2mA	+8mA	+32mA	+2.5mA	+5mA	+20mA/ +8mA	+32mA/ +16mA
ICCSB	500μA Typical	Not Appli-cable	10μA	140mA	10μA	120mA	10μA	85mA	10μA	160mA	10 μA Typical	162mA	10μA	230mA
ICCOP	40mA @ 5 MHz Typical	340mA	1mA/ MHz Typical	140mA	1mA/ MHz Typical	120mA	1mA/ MHz Typical	85mA	1mA/ MHz Typical	160mA	40mA @ 25 MHz	162mA @ 25 MHz	1mA/ MHz	230mA
C_L	100 pF	100 pF	150 pF	150 pF	150 pF	150 pF	100 pF	100 pF	300 pF	300 pF	100 pF/ 30 pF	100 pF/ 30 pF	300 pF/ 80 pF	300 pF/ 80 pF

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navigation controls can remain intact and operational with the 80C86 CMOS control system. With a backup battery power supply, the power sensing unit can transfer the system from main power operation to battery supply. With system power levels approximately 10 percent of equivalent NMOS/bipolar circuits, full 5 MHz operation can be maintained.

As primary power is diminished (battery discharging) or removed (power interruption—battery backup operation) in portable or remote battery-powered applications, running at a lower frequency to conserve power becomes important. Operating power is critical in low-power applications, and CMOS operating power is directly related to frequency.

With the 80C86 family's static design, power requirements can be user controlled; lowering the frequency reduces power. Static design (i.e., no internal dynamic registers needing constant clocking or refresh) allows operation from DC to the individual device's maximum rated frequencies.

The CMOS 80C86 static design allows the system clock to drop to a lower frequency (100 kHz, for example), making full computational and data manipulation powers available while significantly reducing system power consumption. This low frequency operation is not available with most NMOS processors, including the NMOS 8086 where 2 MHz is the minimum allowed clock frequency. Dynamic register designs in the NMOS CPUs need to be refreshed at a minimum rate and do not allow low operating frequencies.

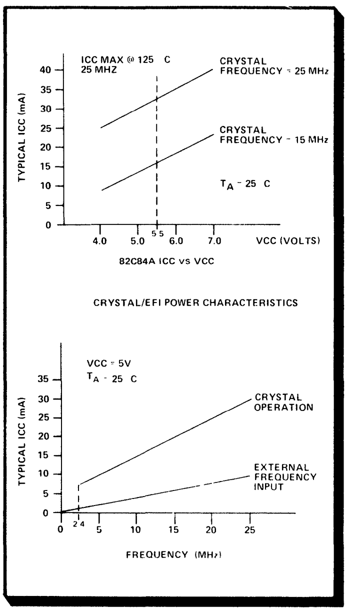
Typical operating power for the 80C86 CPU at 5 MHz is 40 mA, derated linearly as frequency drops (approximately 2 mA at 100 kHz). Similar deratings are also valid for the power dissipations of the peripheral, support, and memory circuits.

Finally, given a power critical situation where power is diminished to the point that even low frequency, full-time operation is undesirable, the 80C86's static internal circuitry allows clocks to be stopped. This capability eliminates the power dissipation associated with switching, and reduces device currents to standby levels. With static DC operation, individual peripheral device standby currents are guaranteed to be less than 10 μA, with the 80C86 CPU typically less than 500 μA.

Static design can also stop and single-step the system clock during system prototyping. This debug method allows the designer to inspect the system bus and examine specific operations. The real time complications of 5 MHz bus transfers are eliminated and system debug is simplified.

Stopped Clock Power Savings

Although the 82C84A clock generator's 40 mA ICC limit is significantly lower than the bipolar 8284A's 162 mA limit, it is still the largest, single power user in a CMOS 80C86 system; this is due to the high frequency of



Power curves *for the 82C84A show the effects of both frequency and voltage decreases on the ICC.*

operation (15 24 MHz crystal frequency for 5/8 MHz system frequency) and the non-ideal waveform of the crystal signal.

When using the 82C84A in a stop-clock application, the external frequency input (EFI) mode of operation must be used. The 82C84A clock generator has a minimum crystal frequency of 2.4 MHz (corresponding to 800 kHz system frequency) for internal oscillator operation. The EFI input allows use of an external clock to provide the main timing. This external clock is processed through the same internal 82C84A circuitry as the crystal oscillator input, so timing within the system remains the same.

An additional benefit, critical to the successful design of a stop-clock circuit, is the 82C84A's reduced operating power when using an external frequency source to drive the EFI input.

With X1 and X2 crystal operation, the input transistors spend a greater percentage of time in the active region due to the sinusoidal nature of the crystal circuit. Driving the EFI input to VCC and GND levels with an external source more effectively turns internal circuitry on and off, resulting in decreased operating power.

The clock frequency reduction must be properly timed to meet minimum 80C86 clock high- and low-time requirements. Therefore, along with the appropriate divide-down circuitry needed to provide the proper lower frequency, synchronization between the low frequency signal line and the control circuitry is necessary. Care must be taken to avoid cases of asynchronous timing errors caused by irregular clocks that are outside the CPU specification limits.

The 82C55A PPI provides the parallel CPU interface to the control circuitry. An interrupt from the 82C59A priority interrupt controller can provide the start-up signal for the system clock control circuitry. The 82C59A allows prioritizing and masking of interrupting sources so that, during the time the system is stopped, only the most critical signals may restart the processor.

High Density Leadless Chip Carrier Packages Increase Reliability, Save Weight

A military CMOS 16-bit microprocessor packaged in LCCs reduces operating temperatures, size, and weight, adding to that family's low-power advantages.

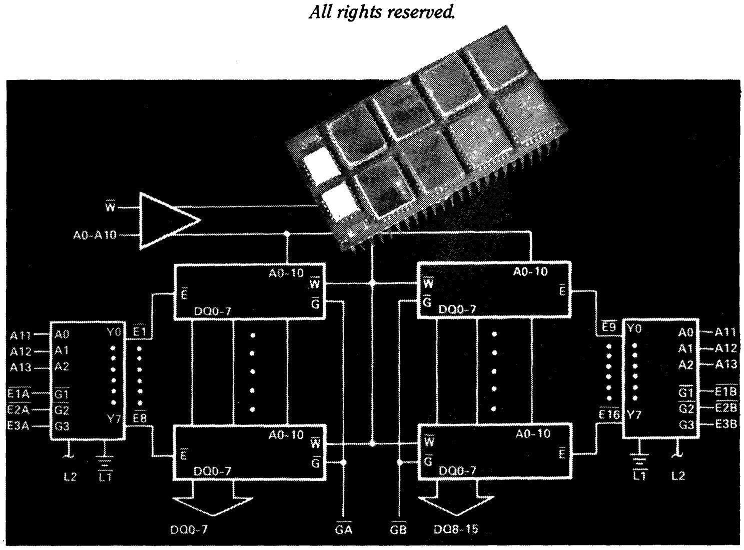
By Walter J. Niewierski and Jeffrey M. Wilkinson

Last month, DE *looked at the 80C86 family, which adds low-power CMOS to a proven design for high performance defense systems. This month, Part II in this two-part series on microprocessors will examine that family's transition to industry standard leadless chip carrier packages.*

Just as critical as power consumption is packaging technique. The low-power operation of the CMOS 80C86 family, along with memory and support chips, allows for design of sealed, portable system enclosures. In turn, this type of packaging reduces operating temperatures and minimizes hostile external environment effects, increasing system reliability.

System Level Reductions

Replacing higher power devices with their CMOS equivalents can reduce system "hot spots" caused by localized high dissipation circuits. A direct replacement with low-power CMOS components will significantly reduce system ambient temperatures. Using the power supply current requirements of the CMOS 82C88 and bipolar 8288 bus controller, along with a typical θjA (junction to ambient temperature rise with respect to power dissipation) of 50°C/W, the following device temperature comparison can be made:



Leadless chip carriers *attached to a ceramic dual-in-line substrate allow Harris Semiconductor to package the complete 16-bit CMOS microprocessor as a single unit. Harris has already used this packaging concept to produce 64K- and 256K-bit RAM arrays based on 16K and 64K chips. All these LCC packaged products are military qualified.*

$$T = \theta jA \times \text{power dissipation} + T_A$$

For bipolar
$= 50°C/W \times (230\ mA) \times 5.5V + 125°C$

$= 50°C/W \times 1.265W + 125°C$

$= 63.25°C + 125°C$

$= 188.25°C$, typical

For CMOS
$= 50°C/W \times (5\ mA) \times 5.5V + 125°C$

$= 50°C/W \times .0275\ mW + 125°C$

$= 1.375°C + 125°C$

$= 126.375°C$, typical

The rise in the die surface temperature of CMOS is approximately two percent of the increase seen in NMOS products. This lower CMOS die temperature results in a significant in-

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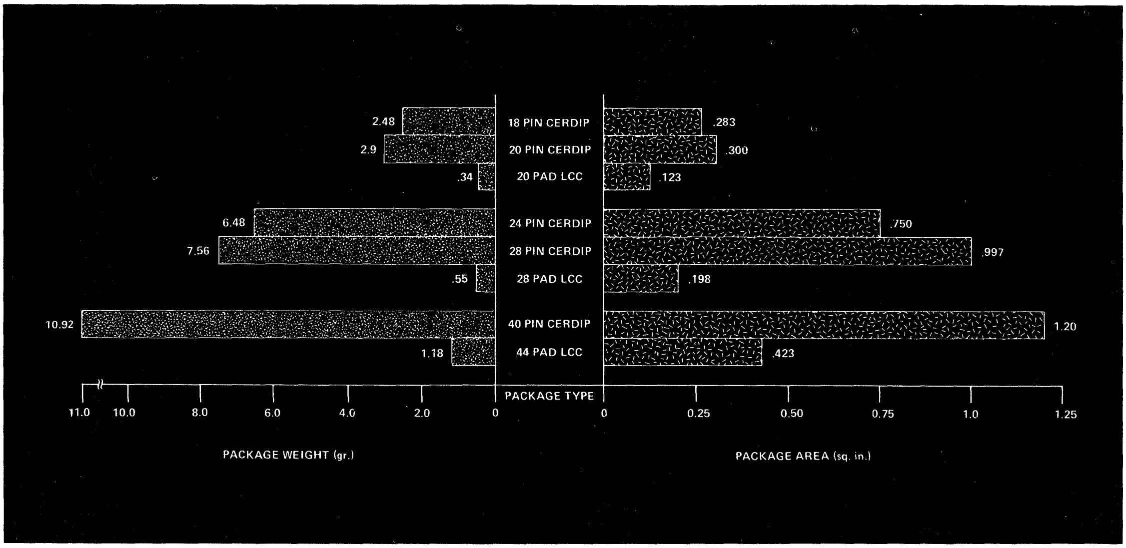


Package weights and area *for LCCs are compared to equivalent ceramic dual-in-line packages.*

crease in the mean time between failure (MTBF). The MTBF equation shows the direct relationship of the failure rate and temperature:

$$MTBF_T = e^{EA/KT}$$

where $MTBF_T$ = MTBF at temperature T

EA = activation energy (ev)

K = Boltzman's constant

T = absolute temperature (°K)

Similar increased MTBF numbers can be estimated for system operation when system ambient temperatures are reduced by CMOS circuits.

With decreased system temperatures, the need for special cooling equipment and enclosure openings can be eliminated or reduced. The use of cooling techniques such as heat pipes, liquid coolants, heat sinks, and louver assemblies can add weight and volume to systems. Besides these physical disadvantages, the lower reliability of electromechanical operation and the system's exposure to hostile environments adds an additional risk factor to system reliability. CMOS systems can keep the system operating temperature to lower levels, enabling the use of sealed enclosures with a minimum of cooling.

Temperature also affects circuit and system performance. CMOS leakage currents and, therefore, standby power dissipation increase at the high end of the temperature range. Performance also degrades because of increased channel resistances on the P- and N-channel transistors. Keeping the system ambient temperature low results in an improved overall performance.

Replacing existing circuits with low-power CMOS offers many benefits. However, the system environment remains constant—that is, compatible with NMOS/bipolar operation. Power supplies, cooling equipment, and enclosure size and weight all remain the same.

In order to optimize the reductions possible in weight and cost and increase reliability, the system must be designed with low power in mind. Smaller system power supply requirements and lower temperatures eliminate the need for cooling components.

Device Level Miniaturization

Decreasing an individual device's package can lead to miniaturization and portability. Flatpacks and DIPs are the main packages used in military system designs. However, leadless chip carriers (LCC) have recently become popular because of their small size and light weight.

The trend toward using dual-in-line packages has proven sufficient in most applications. But, where very light and small, complex electrical functions are required, LCCs offer space and flexibility. DIPs occupy approximately three times the space an LCC package uses for the same pin count. And unlike an LCC package, the DIP has leads that can bend or break, adding a parasitic resistance and capacitance.

The introduction of flatpacks to military applications proved an alternative to the DIP package in reducing board space requirements. But, flatpack costs are high because of the large amounts of gold used in the package plating. Long lead length and narrow spacing also require special carriers for handling. And, when soldering to printed circuit boards, the long lead length permits package vibration, which could affect the reliability of the leads or their solder connections.

Leadless chip carriers offer small package sizes, no leads to bend or break, and premium electrical performance due to full parametric testing allowed at the package level. For critical military applications, MIL-STD-883B, group A, B, C, and D can be applied to leadless chip carriers in a method similar to those applied to dice packaged in a size-brazed DIP.

Many devices cannot be manufactured in LCCs or must be placed in larger pad count carriers because of bipolar and NMOS technologies' excessive power dissipations. But with CMOS, power dissipation is reduced—optimizing package size and pin count.

The leadless chip carrier pinout definitions for the CMOS 80C86 family follows, for the most part, predefined pinout and package assignments as established by the original NMOS source. With certain device types, specifically the original source products, larger than necessary packages were used. For example, the 8282 octal latch, 8284A clock generator, and 8288 bus controller are packaged in 28-pad LCCs, while 20-pad LCC packages are standard for the 82CXX CMOS equivalents. One of the main reasons for using this enlarged package for bipolar devices is its higher-than-CMOS power dissipation. With CMOS' lower power characteristics, however, minimum package sizes can be achieved. Using 20-pad LCCs for the CMOS versions of the above devices allows for maximum system packing density.

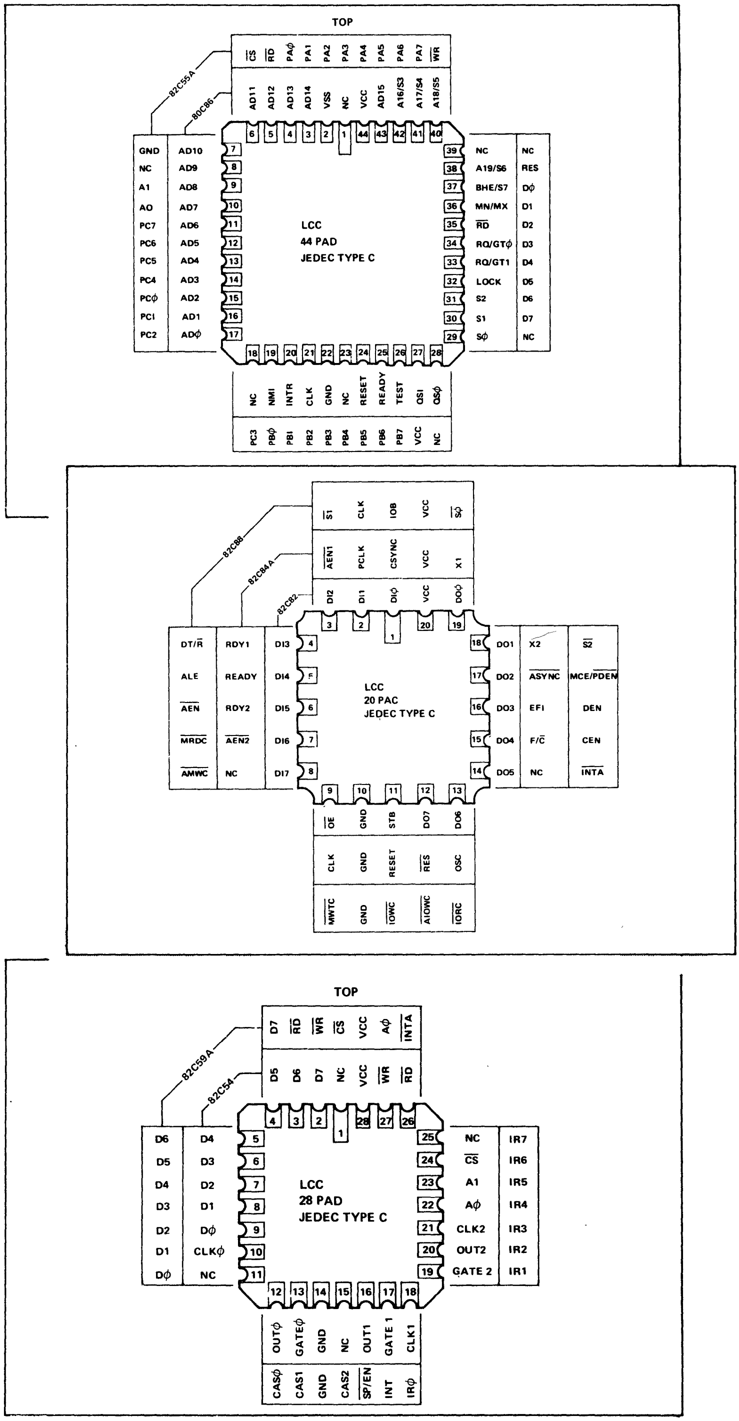
Leadless chip carriers for high density packaging and minimized pad counts further reduce board space and weight in high density systems. In addition, LCC packages' reduced package lead lengths and interconnect lower the parasitic inductance of the circuitry. Parasitic inductance is a major contributing factor to noise in high-speed CMOS system designs (See sidebar, "System Noise Reduction in High-Speed CMOS Design").

LCC Assembly Techniques

The relatively recent revival of the LCC package, along with the advantages of implementing these packages on printed circuit boards and substrates, allows designers a high-density packaging option. To ease the transition from conventional DIP/PCB assemblies to the LCC/PCB packaging option, the designer must understand the differences between the two packaging technologies.

Substrate Material Selection

The basic concern for selection of the substrate material is matching the



Pinouts *for the 80C86 CMOS microprocessor family are similar to the more familiar pinouts used for conventional flatpacks.*

8 ARTICLE REPRINTS

CMOS vs NMOS Power Requirements

Part Type	Description	CMOS Operating Power Supply Current	NMOS/Bipolar Equiv. Power Supply Current
80C86	CMOS 16-Bit CPU	40 mA	340 mA
82C54	CMOS Interval Timer	5 mA	140 mA
82C55A	CMOS Parallel Interface	1 mA	120 mA
82C59A	CMOS Interrupt Controller	1 mA	85 mA
HD-6406	CMOS UART/BRG	3 mA	100 mA
82C82	CMOS Octal Latch	1 mA	160 mA
82C83	CMOS Octal Latch (Inv)	1 mA	160 mA
82C84A	CMOS Clock Generator	25 mA	162 mA
82C86	CMOS Bus Transceiver	1 mA	160 mA
82C87	CMOS Bus Transceiver (Inv)	1 mA	130 mA
82C88	CMOS Bus Controller	5 mA	230 mA
82C89	CMOS Bus Arbiter	5 mA	165 mA
Approx. System Power Supply Current		**89 mA**	**1,952 mA**

80C86 Family Package Comparisons

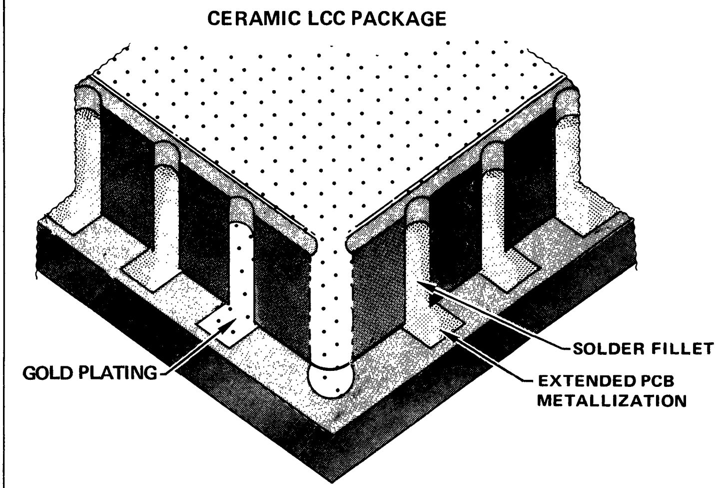
Part Type	DIP Pin Count	LCC Pad Count	DIP Area (Sq. In.)	LCC Area (Sq. In.)	DIP Weight (Gr.)	LCC Weight (Gr.)
80C86	40	44	1.2	0.423	10.92	1.18
82C54	24	28	0.75	0.198	6.48	0.55
82C55A	40	44	1.2	0.423	10.92	1.18
82C59A	28	28	0.997	0.198	7.56	0.55
HD-6406	40	44	1.2	0.423	10.92	1.18
82C82	20	20	0.3	0.123	2.9	0.34
82C83	20	20	0.3	0.123	2.9	0.34
82C84A	18	20	0.283	0.123	2.48	0.34
82C86	20	20	0.3	0.123	2.9	0.34
82C87	20	20	0.3	0.123	2.9	0.34
82C88	20	20	0.3	0.123	2.9	0.34
82C89	20	20	0.3	0.123	2.9	0.34
System Area/Weight Summary			**7.43 Sq. In.**	**2.526 Sq. In.**	**66.68 Gr.**	**7.02 Gr.**

Material Thermal Properties

Substrate Material	TCE (in./in./°C x 10^{-6})	Comments
Alloy 42	5.3	42% Ni, Balance Fe
96% Alumina	6.3	Industry Standard
94% Alumina	6.4	Industry Standard
92% Alumina	6.4	
Copper Clad Invar	6.4	
99.5% Be0	6.4	Expensive
Low Carbon Steel	12.0	Porcelanized
Polyimide G30	14.3	Industry Standard
Epoxy/Glass G10	15.8	Industry Standard
Triazine G40	16.0	Industry Standard
CDA 101 Copper	17.3	Very High TCE
6061 Aluminum	23.6	Very High TCE

linear thermal coefficient of expansion (TCE). Matching the TCEs is critical to attaching an LCC to a substrate when the assembly must be able to survive the number of thermal cycles typical of military applications and testing. When the LCC is soldered on a board, the solder interface is not only the electrical contact but the mechanical connection as well.

When the TCEs of both the package and mounting substrate are not properly matched, thermostatic deflection (warp) can occur during temperature cycles. When these two materials warp, torque is directed to the solder joints, which results in a fatigued mechanical/electrical connection. This problem becomes even more apparent as the LCC pin count increases. Larger package and substrate sizes result in higher stress levels. The selection and use of board material should follow this general rule: The larger the difference between the TCEs of the two materials used (the LCC and the substrate material), the smaller the substrate surface area should be. Available materials range widely in cost and TCE characteristics.



Printed circuit board metallization *should extend beyond the LCCs outer edge. This extension permits molten solder to flow up the castellated regions, and to form a fillet of solder to complete the electrical connection while strengthening the mechanical bond.*

Printed Circuit Considerations

After selecting the substrate material, the printed circuit trace geometries should be investigated. The circuit traces for LCC foot pads should be the same size as the metallization on the bottom of the LCC and slightly longer to the outer edge of the package. This metallization allows the solder, when heated to the reflow temperature, to wet both the base contacts and the LCC package's castellations.

The outer surface of the solder deposit forms a fillet where it extends over the metallization pad on the substrate's surface, strengthening the mechanical bond. This type of bond raises the LCC away from the board's mounting surface to facilitate cleaning the residual flux and debris under the package.

To optimize packaging density, relatively tight geometries in layout are of concern. Leadless package layouts often require .010-in. lines, 010-in. spaces between lines, and .020-in. or smaller feed-through holes. The pads that connect to the LCCs are typically .020-in. wide, and are .050-in. center to center. This spacing allows one .010-in. line at .010-in. spacing to be run between the LCC mounting pads.

If lines are run close to other metallization, a solder mask should be used on the board to prevent solder bridging during the reflow process. When using multilayer boards or substrates, a clean layout can be made by allocating the surface layer metallization exclusively to LCC mounting pads—eliminating the need for a solder mask and reducing the concern for solder bridging. Electrical noise problems can be diminished by power gridding the supply buses on a unique layer while routing signal lines on other layers of the substrate.

LCC Mounting Techniques

Socketing and soldering directly to the board are the two methods possible for mounting LCCs on circuit boards. In military applications, socketing becomes a disappointing compromise for LCC mounting because of the socket's bulky size. An LCC socket has its place in less critical applications, but can severely sacrifice packing density, and falls short of the stringent environmental testing required by most military applications. Direct LCC to substrate mounting is the most reliable method for assembly.

The basic principle for attaching LCCs to boards and substrates is reflow soldering. Both the leadless package I/O metallization and the interconnecting substrate metallization are pre-tinned with solder; the two are then mated and heated by one of a number of means. Surface tension and the cohesive properties of the molten solder align the package over the substrate metallization. The assembly is then cooled, making complete the electrical/mechanical bond.

The best results are usually obtained from reflow soldering, and when both the LCC and the metallization on the substrate it is to be attached to are pre-tinned. The LCC package pads can be pre-tinned by fluxing and dipping. The substrate pads are usually tinned by wave soldering or screening on a solder paste.

When using a wave solder tinning approach, and after the substrate has been tinned, an adhesive must be applied temporarily to hold the LCC in place over the substrate metallization during the reflow process.

In implementing the screened on solder paste technique, the paste is

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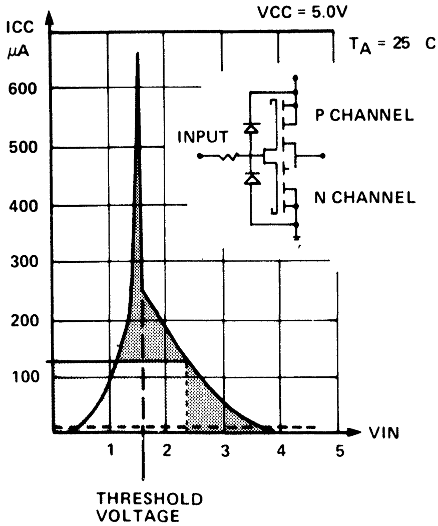

CMOS INVERTER
VIN vs ICC

System Noise Reduction in High-Speed CMOS

The majority of current flow in an all CMOS system is transient by nature, occurring on the waveform edges or transitions where instantaneous demand for current occurs. These current transients result from:

- charging and discharging of output load capacitance
- simultaneous P-channel and N-channel switching

The currents generated by these switching conditions can be large and cause noise on the power supply lines. However, the current's magnitude is not the only factor in determining the size of VCC/GND variations—The time period over which this current is switched is also critical. If this time period is relatively long, the current can be categorized as steady or bulk current, and the transient effect on the power supply voltage is minimal.

However, as the time period decreases, these inductance effects begin to play a more important role. The relationship of time and inductance are given by:

$$V = L\, {}^{di}/_{dt}$$

Switching the same amount of current more quickly will have as great an effect on the VCC as an increase in the magnitude of the current change in the same time period. As propagation delays and output rise/fall times decrease, the effect of the related inductance becomes more significant.

The parasitic inductance is a result of system interconnect, socket, decoupling capacitor, and device package contributions. The inductance must be minimized to reduce this transient effect. The main sources of inductance are lead lengths (both IC and decoupling capacitor), PC board interconnect (VCC to capacitor to GND), and the capacitor, itself.

Although the designer can do little about standard IC packaging and lead length, manufacturers can employ several techniques for controlling the IC's parasitic inductance. Matching device size to package cavity area allows minimum bond wire lengths in assembly. Doubling the VCC and GND bond wire interconnect also reduces parasitic inductance effects within the package.

Printed circuit board runs should be kept to minimum lengths with VCC and GND lines 3/16-in. to 5/16-in. wide to reduce power line inductance. In prototype circuits, extra care should be taken in limiting wire length and including sufficient decoupling since the wire and socket lead length add inductance beyond that normally found in PC boards. Low inductance capacitors and socket elimination will help control system related inductance. —*W.J.N. & J.M.W.* ■

applied to the substrate contacts using a screen printing technique. Normally, a layer of "wet" paste, eight to nine mils thick, is deposited on the substrate contacts. Then the contact area, covered with paste, is air dried until tacky before the LCC is attached. The LCC is then mounted to the corresponding contacts manually or by automatic placement.

One important step in the LCC assembly process is baking the populated substrates dry before soldering, which allows the air and flux pockets in the paste to evacuate, minimizing the volatility effects in a vapor phase soldering operation. This process is vital because unevacuated flux pockets will cause the package to float during the reflow operation. Floating affects the package's positioning properties, and an unacceptable package alignment can occur. Also, the liquid vehicle of the solder paste is evaporated and the LCC is temporarily held to the substrate by the paste, which is now dry.

LCC placement on the substrate is not as critical as it might appear. During the reflow process, the dried solder paste holds the LCC in place while the paste reaches the reflow temperature. During this process, the surface tension of the solder will pull the LCC into alignment over the substrate contacts. The placement must be accurate enough to insure the LCC solder pads do not overlap the adjacent interconnect on the metallization below.

Heat must be applied to melt the solder and connect the LCC and the substrate. Methods such as belt furnaces, heated air chambers, and infrared radiated heat techniques can be used, but are not finding widespread acceptance. The most popular heating method for high-volume production is the vapor phase reflow technique.

In vapor phase reflow, the populated substrate to be soldered is lowered into a saturated vapor above a pool of high boiling point, flourinated hydrocarbons. Usually, vapor phase soldering systems have two operation zones. The primary zone is used for heating; the secondary zone is used as an intermediate cooling and cleansing zone before the assembly is removed from the soldering operation.

As the board is lowered into the primary zone, the solder joints are reflowed uniformly by the vapor, condensing over the surface of the substrate, which gives up its latent heat from vaporization. This thermal exchange heats the board quickly and evenly. When the substrate is raised into the secondary zone, the now condensed fluid from the primary zone drips off the board into the boiling liquid below. The substrate assembly exits from the process, uniformly oldered, dry, and relatively clean.

Cleaning the soldered assembly should be performed immediately after the vapor phase reflow process while the boards are still hot. Uncongealed residue can be easily removed at this time, resulting in thorough cleaning.

Another reflow technique employs hot solder oil. The substrate with positioned LCCs are fully immersed in a hot oil bath to bring the solder and parts up to the reflow temperature quickly. The assembly is then removed from the oil and allowed to cool. Rinsing the assembly afterwards removes residual oil and excess flux. This technique is useful for experimentation and low-volume production because of its relatively small capital investment.

LCC Assembly Rework

The repair and replacement of a failed device packaged in an LCC is important in chip carrier assembly processes. The advantages in rework stem from the ease of reflow soldering. Since there are no leads on LCCs and usually no holes in the substrate to deform, many rework cycles are allowed. Of course, rework is dependent on the reflow technique, type of solder, reflow temperature, and the thickness of the metallization used in a particular application. During a rework situation, LCC removal can be accomplished using several techniques.

One method is to use the same hot solder oil immersion technique for applying the LCCs to a board. After the immersion and subsequent reflow of the solder, a pair of tweezers, or a similar tool, can be used to remove the defective LCC from the board. Other removal methods are possible, such as using a soldering iron with a specially shaped tip to heat the contacts or by heating the defective package and its surrounding area with a forced hot air gun.

The heat gun method is usually the most convenient, inexpensive, and practical for rework. When the LCC is heated by the gun, the package should be removed with tweezers—the now exposed substrate contacts can be tinned, if necessary, as could the LCC contacts on the replacement device. The LCC is manually replaced in close proximity to its final position. The repair area or entire board is then heated to the solder reflow temperature to complete the operation.

System on a Substrate Concept

When the appropriate LCC system components are assembled on a ceramic substrate with dual-in-line pins, the space, weight, and reliability advantages of LCCs are made more accessible. This "system on a substrate" technique allows LCCs to be used in more traditional system configurations such as those using standard DIP packaging.

One of the first movements in this concept direction has been the development of memory arrays on ceramic substrates. The HM-6564, a 64K CMOS RAM module, was first introduced in 1979, and uses sixteen 4K x 1 CMOS RAMs mounted on both the substrate's top and bottom. This packaging technique further increases an LCC's functional density on the RAM module. Other products available in module form include the Texas Instruments TMS4164, a 64K dynamic RAM assembly, and a 64K EEPROM assembly from National Semiconductor, the NMH2864.

With the introduction of the 16K CMOS RAM, a step-up in module density is also seen. The HM-92560 uses sixteen HM-6516 RAMs, and has a total capacity of 256K bits of static CMOS memory. The HM-92560 can be configured as a 16K x 16 or 32K x 8 static RAM array.

The HM-6564 and HM-92560, along with the other such modules, provide only the memory circuitry—This approach increases the system packing density when large amounts of memory are necessary. Maximum reduction, however, is not accomplished because bus drivers and decoders must be added externally to the module assembly. To achieve a greater reduction in size, as many functions as possible must be placed on high density assemblies.

The Harris HM-92570 is a beginning to the "system on a substrate" development. By providing LCC-packaged CMOS bus drivers and decoders on the substrate, all the functions of a 256K-bit memory board are contained in one high density assembly. The HM-92570 address inputs are buffered and have an input current leakage limit of 10μA so direct connection to the CPU address bus is possible without additional buffering. The HD-6440 CMOS decoders on the substrate meet the memory array decoding needs.

The Digital Equipment Corporation Micro/J-11, a CMOS module assembly, which is a two-chip set equivalent of the PDP-11 minicomputer, has adapted this concept to the microprocessor area. Two CMOS devices manufactured by Harris, the control chip and the data chip, are packaged in 64-pad LCCs and are mounted on a 60-pin ceramic DIP substrate, compatible with the PDP-11's full instruction set. Compared to the original PDP-11 assembly, which consisted of several boards, this transition to a 60-pin substrate offers significant size and power reduction advantages.

The next step will be the combination of CPU, I/O, and a significant amount of memory onto a single substrate assembly. The development of more highly integrated processor, such as the 80C186, that include I/O and control functions on-chip will make the logistics of providing all capabilities in a single high-density unit easier to handle. With all functions available in one unit, systems can be implemented with one assembly connected to the outside world, or additional assemblies added to provide greater amounts of memory or high-density multiprocessing capabilities. ■

Solving System Design Problems Via The Semicustom Route

By Jack W. Scherer

Director, Semicustom Marketing Semiconductor Digital Products Division, Harris Corp.

Integrated-circuit definition at the system-design level can make use of time, manpower and silicon far more effectively today than at any other time in the past. An important ingredient contributing to the improved efficiency is semicustom technology. While not new to the design scene, semicustom's potential and importance here are growing, largely the result of its increased flexibility.

While circuits such as microprocessors allow system designers to customize circuit operation, their basic capabilities are, for the most part, predefined by the semiconductor manufacturer. With semicustom, by contrast, the designer can define specific system design solutions at the circuit-function implementation level.

Three major factors are driving semicustom: CMOS technology, standard-cell libraries and design automation.

When the goal is to integrate as many functions as possible onto a single chip, power and design flexibility are key. The low-power and circuit-design options available with the complementary p- and n-channel structure of CMOS give this technology the edge here.

The technology used to design highly integrated semicustom circuits must offset the power increase normally seen when transistor counts jump by an order of magnitude. CMOS does just that.

In addition, semicustom integration reduces system power. The power for driving external capacitive loads drops significantly, since much of the circuit interface is done internally to the device package. This also reduces the number of packages and, in turn, board and system size.

Reducing power-supply and board-size requirements and eliminating fans and heat sinks allows use of smaller, sealed enclosures, with no need for vents or cooling ports. Overall, reliability is increased and costs are lowered.

Standard-Cell Edge

The main argument for the move to semicustom has been the rigid, inflexible function definition of standard products. The desire to define and customize function also gives standard-cell designs an advantage over the gate-array approach.

Gate arrays are easy to define because of their fixed-gate structure, which needs only a customized metallization layer. This rigid structure is also their limiting factor, with users being bound not by imagination or by photolithography limits but simply by the number of gates in the array.

Standard cells have a functional density capability much above that attainable with gate arrays. These predefined functional blocks make application-specific design possible at density levels equal to or greater than standard LSI or gate-array-based circuits. For a typical comparison, see Chart A.

And, when compared to gate arrays, standard-cell design parts can cost 30 percent less on a volume basis. There is little premium in design turn-around time or prototype cost. In fact, as double-level metal and other design changes are introduced to increase gate-array density, their greater fabrication complexity tends to equalize their prototype design time with that for standard-cell circuits.

Ease of use is critical to any type of semicustom design. As regards this, the 80C86 LSI Macro peripheral family, which is available from Harris' standard-cell library, provides the same function and reliable design found in standard industry products built in DIP or surface-mount packages. Available functions range from peripheral support (82C59A Interrupt Controller, 82C54 Interval Timer) to data communication (82C52 UART/BRG) to bus support (82C82/3/

6/7 bus drivers). Several of these functions can be combined onto a single chip.

Standard-cell libraries containing these types of industry standards do away with the need to "reinvent the wheel" each time a new product must be designed. Turnaround time is reduced; functional design and checkout times are significantly lowered; and circuits become more reliable, since these standard functions have already been tested and used in many different system applications.

Design Automation

Today, thousands of engineers are designing board-level systems using standard ICs. But, only a fraction of that number are trained to design integrated circuits, even though the tools needed to tap the vast system-level design base using semicustom IC technology already exist.

Essentially, semicustom manufacturers must minimize the amount of additional knowledge needed to work in silicon. They can do this by coupling the system designer to the IC-design process through hardware and software, with design automation being of critical importance here.

Standard-cell libraries with predefined LSI functions, MSI/SSI cells and automated software support tools allow logic designers to use existing system-level design experience. To tap standard cells' design potential for adding value to their systems, designers must look for manufacturers who can offer a sound CMOS technology base, combined with plans to move forward to the submicron level; who can supply a total system solution for CMOS design; and who can provide complete service and support in both design and manufacturing. **EET**

Chart A.

Gate Array	**Gross Gates 6000**	**Usable Gates 4400**	**Die Size sq mils 160k**
Standard Cell	**Open-ended**	**4400 (for comparison only)**	**80k**

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A Design Approach Using Large-Scale Macros

Michael A. Bohm, Harris Semiconductor, Melbourne, FL

The capabilities of semicustom vendors have made significant advances in recent years. However, the designer generally still has to design at the SSI/MSI level. Complex systems still require a great deal of design time. The Harris HSC cell library was developed to increase the productivity of the designer and thus reduce the development cycle. The family includes 23 LSI macros, which can be combined with an extensive SSI/MSI library to customize a complete system on a chip. The LSI macros represent years of work converting the standard product area to standard cells.

The MSI and LSI logic macros in this library vary in complexity from 150 to 3,000 gate equivalents. These macros are 100% functionally compatible with the corresponding standard ICs available in discrete packages (see Table 1). AC performance is equal to or better than the standard product. These elements are usable from −55 to 125 degrees Celsius, with an operating voltage of 5 V ± 10%. The present versions are manufactured in a 2.5-micron CMOS process. Each design uses 100% static circuitry, with a stand-by current of less than 10 μA.

The designer uses these LSI macros as if he were designing at the system level. Many of the macros have complexities in the 2,000–2,500-gate range. A demonstration of the reduction in I/O count achieved using LSI macros is shown in Figure 1.

Hardware Design

The development of the LSI macros is an ongoing task. The first 23 macros are members of the 80C86 peripheral family, plus some general communications circuits. Two types of macros exist in the library. The first type is the soft macro. These macros are laid out with standard cells every time they are used, in order to minimize die area. These macros include the timers, interrupt controllers, UARTs, and I/O controllers. These circuits have a large AC margin to specification and conform very well to the standard-cell approach. (Harris standard products that are now on the market were implemented with standard cells.)

The second type of macros are the hard macros. These macros are a fixed layout and are placed in the circuit as a block. They also mix very well into the standard-cell approach as subchip modules.

While the LSI macro approach is an efficient method of design, a complement of simpler elements that will "glue" the design together is needed. Besides a full family of 110 primitive standard cells, approximately 90 MSI macros were developed. These MSI functions are 100% functional replacements for the standard 74XX components and are implemented as soft design modules.

Cell	Description	Gates
82C37A	DMA Controller	2332
82C52	UART/Baud Rate Generator (BRG)	1840
82C54	Programmable Interval Timer	2540
82C55A	Parallel I/O	566
82C56A	Multifunction UART	2600
82C59A	Priority Interrupt Controller	542
82C82	Octal Latch	100
82C83	Inverting Octal Latch	100
82C84A	Clock Generator	50
82C85	Static Clock Controller	150
82C86	Octal Bus Transceiver	100
82C87	Inverting Octal Bus Transceiver	100
82C88	Bus Controller	60
82C89	Bus Arbiter	70
HD4702	BRG	450
HD6402	UART	555
HD6406	UART/BRG/Modem Control	1840
HD6408	Asynchronous Manchester Adapter	600
HD6409	Manchester Encoder-Decoder (MED)	500
HD15530	MED (MIL-STD-1553 compatible)	600
HD15531	Programmable MED	600
1K RAM	Reconfigurable RAM	2600
1K ROM	Reconfigurable ROM	1200

TABLE 1. LSI macro functions.

All macros go through a thorough verification to prove out functionality and performance. Logic simulations are performed using the same test vectors used for final test of outgoing product. Estimated routing capacitance and loading are used in the simulation to verify AC specifications. Feedback from the field is also used to improve the existing designs. Finally, a data sheet is published that reflects all specifications.

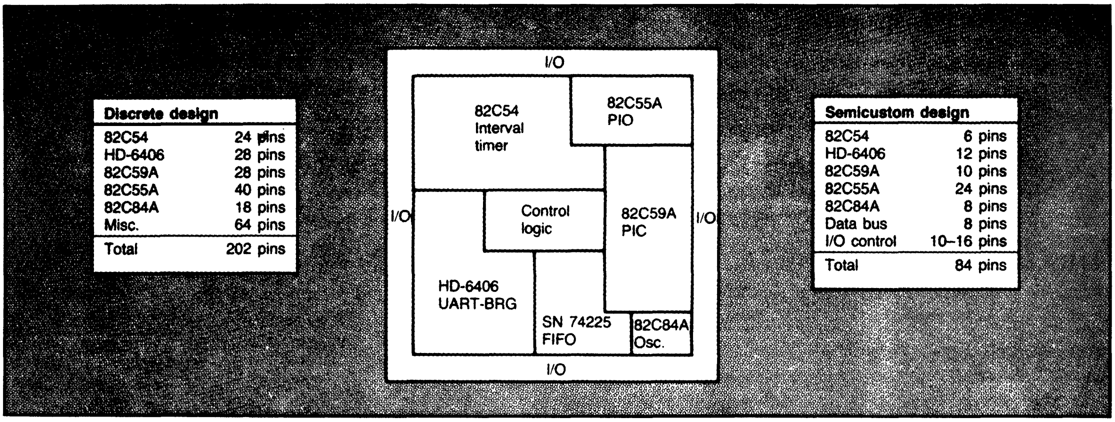


FIGURE 1. External I/O interface reduction.

The entry point into the Harris Teledesign system is through an engineering workstation. At present, the Daisy system is the major interface with the design system. Valid will be the next workstation to be brought online.

Design and related layout needs have been considered in constructing the system. Critical paths inside the module have been given special weighting to indicate approximate AC delays per node. The placement and routing routines will use this information to minimize propagation delays on these critical paths.

In order to ensure that the soft MSI and LSI macros meet their performance specifications, a technique called partitioning is used. A partition is a logical cluster of cells that have been given a specific domain, that is, associated with a specific area of the chip. These partitions are used to give the software an indication of the floor plan of the chip and its initial placement.

All circuit design is set up to allow the customer to move on to other technologies with a minimum of redesign. When the LSI macros were designed, the logic function was captured independent of technology. Simulations were first completed to prove out functionality by using a generic standard-cell family. As new cell families are developed, the naming convention they use will match previous families. This allows a design to migrate up to new technologies. This task is transparent to the designer, since none of the databases change except the "calls" to a different library.

This technique also gives the designer the ability to use previously designed semicustom circuits as LSI macros. This ability will then allow a system with multiple semicustom ICs to merge into a single circuit when the process technology matures, without the need for redesign.

To help guarantee technology independency, a few special cells have been developed. Digitally programmable one-shot and pulse-delay cells have been designed to aid in the use of asynchronous logic in some of the LSI macros. Bus hold devices and precharge cells have been used when designing three-state data buses internal to the macros, and they will also be used when wiring macros together.

Both TTL and CMOS input levels are available. The I/O cell outputs have a 6-mA drive capability with a 10-ns delay into 100 pF over the military temperature range. I/O cells have been laid out in various aspect ratios to allow for optimal layouts regardless of gate count or number of pins. These I/O cells will supply the AC and DC characteristics that are needed for a microprocessor-based system.

Software Support

To allow the use of LSI macros within the Harris Teledesign system, a change in basic design philosophy had to occur. Numerous software routines had to be written to handle this new approach. When a schematic is captured on the workstation, not all the data needed to perform simulation and layout is available at that point. What is captured is the heirarchical connectivity of the design; i.e., LSI82C55 is connected to an SN74165, etc. (see Figure 2).

All models needed to perform the design are stored on the mainframe, and only when the database is compiled for logic simulation are all levels of the data brought together. This approach allows the design system to talk to any workstation, and it also sets up a minimal storage area for the database.

An engineer can capture a design at a workstation and then create a Harris HDL (hardware description language) file. This file is then uploaded to the mainframe, where it is linked with the proper library. All simulation, layout, and test-generation tools then use this HDL file as input.

A major objective that was kept in mind when designing the LSI macros was to protect the proprietary design information. A security system was put in place to prevent unauthorized access to certain levels of the hierarchy. Since the Teledesign system is a "true" hierarchial system, the entire design, starting from the block diagram down to any single transistor, can be viewed.

Since the designer needs to see only the pin information of the macro, design access level will be limited to only the information displayed on the workstation, and nothing lower in the hierarchy. Those individuals who perform LSI macro design will have access to the entire design structure. With this approach to database control, accidental corruption of data cannot occur from outside users. Designers may look on this security as a disadvantage, because they cannot "customize" the LSI macros. On the other hand, the security is a guarantee that the macro circuit used will be a proven and reliable design.

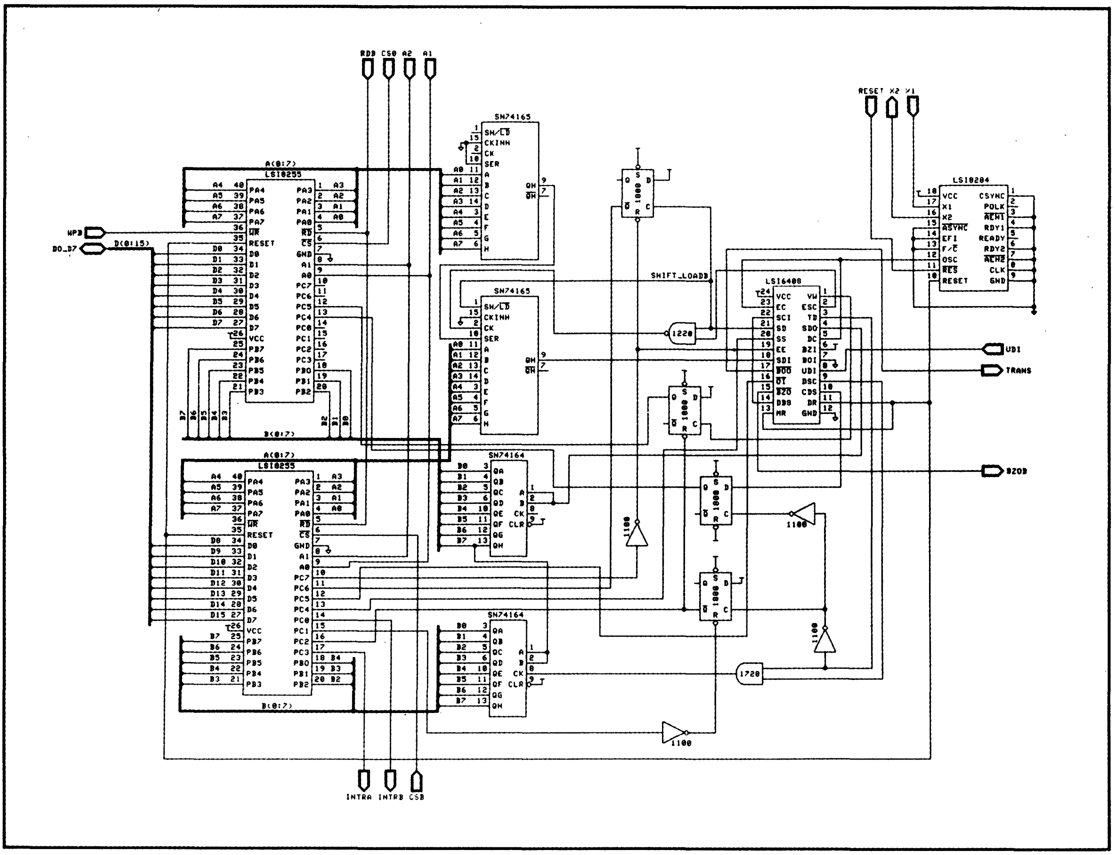


FIGURE 2. Example of a system-level schematic captured on an engineering workstation.

The initial simulation tool allowed any node in the circuit to be interrogated. It was deemed desirable that only the information available at the pins of the components be accessed. This restriction not only improved simulation time, but it also made the initial debugging of circuits much simpler.

Another feature added was the ability to evaluate timing equations. Each standard-cell model contains a t_{pHL} and t_{pLH} equation with variables for fanout and capacitive load. When a circuit is compiled for simulation, a file containing the load information is back-annotated into the database.

This pre-layout file contains exact fanout data with an estimated routing load. After layout, it contains all actual loads. Work now in progress will include global variables for process, voltage, and temperature coefficients. This will allow the designer to specify at the beginning of a simulation exactly what conditions he wishes to simulate.

Layout was the final area in which modifications were made. Since most of the LSI marcos are soft designs, the number of basic cells given to the router exceeded 1,500 elements. When utilizing commercially available placement and routing software, we found there was a major dependence on initial placement of cells. Our method for predictable and optimal layouts was to use the logically clustered data available from the engineering workstation. The result was a predictable layout and a 10% reduction in die size. At the current time, we are developing a placement optimizer routine. By using simulated annealing techniques, this program will reduce chip area by 6% to 15% by reducing the total number of feedthroughs, vias, and routing.

Summary

The Harris HSC library including the LSI macros offers an advantage to the system designer by providing the ability to create a semicustom IC design with proven components. With the aid of a workstation, design can be done using system-level design techniques in a software atmosphere. By using these macros, a reduction in development time, cost, chip size, and power consumption will be seen. □

About the Author

Michael A. Bohm is currently Harris Corp.'s section head in charge of semicustom development for the Semiconductor Division's semicustom product line. His concentration is now on CAD hardware and software support for the LSI macro family of standard cells. He has been with Harris since receiving the B.S.E.E. from Florida Institute of Technology in 1978.

A Comparison Of CMOS Static Random-Access-Memory Cells

By Ken Lyons

Not all CMOS static RAMs are the same. The biggest difference is in the number of transistors used to construct the SRAM's cells. Today, that can be either four or six. The impact on system performance that each has differs considerably—in fact, a switch from one to the other can have a greater impact on performance than the system design itself.

The four-transistor (4-T) cell is commonly used in commercial-temperature-range RAMs because it is smaller and easier to build than the six-transistor (6-T) cell. It is also found in some military-temperature-range RAMs.

However, the 6-T cell requires less standby supply current than the 4-T when operated over the military temperature range (−55°C to +125°C). Its stability is inherently greater than that of the 4-T cell, giving greater immunity to soft errors due to electrical noise and alpha particles. Tolerance to gamma radiation is also improved.

Why then do so many CMOS RAM manufacturers use the 4-T cell? Many consider the 6-T cell more difficult to design because the cell uses two types (n- and p-channel) of transistors, whereas the 4-T cell uses only n-channel transistors.

The 6-T cell also requires tighter lithography to obtain the same cell size.

Another reason not to use 6-T cells is that RAMs contain additional circuitry to increase speed. Some techniques used to accomplish this result in circuits that consume far more current than the memory array itself. In this case, manufacturers opt for the easier-to-process 4-T cells, as the 6-T's lower power consumption is offset by the speed circuit's high power requirements. However, newer techniques give low-power-consuming speed circuits, and, in these instances, 6-T cells are gaining favor.

Despite the apparent popularity of the 4-T cell, the number of full-CMOS, 6-T-cell RAMs in the market is growing. This is especially true for military-temperature-range parts.

RAM Cell Optimization

It might appear at first that the RAM cell is too small a circuit to have a significant impact on RAM performance. Because the RAM cell must be duplicated as many as 256k times in a single CMOS static RAM, taking up more than 80 percent of the chip's area, a small change in the performance or structure of the cell has a large cumulative effect on device characteristics. Because of this, RAM-cell optimization for specific applications is extremely important.

Although 4-T and 6-T RAMs both operate similarly, they differ greatly in construction (see diagram). This is particularly true regarding the inverters that make up the data-storage latch. The 4-T cell uses one n-channel transistor and one polysilicon load resistor for each of the two inverters in the latch. This is actually an NMOS circuit.

CMOS RAMs that use this type of cell are frequently referred to as mix-MOS RAMs because they combine NMOS and CMOS circuitry on the same chip.

On the other hand, the 6-T cell uses one n-channel and a complementary p-channel transistor for each of the two inverters. This is a true CMOS circuit—CMOS RAMs that use this type of cell are sometimes called full-CMOS RAMs.

Load Resistor Resistance

One of the most important measures of cell performance is the supply current required to retain data in the cell. The latch in a RAM cell has two stable states, each of which occurs when the output of one inverter is high and the other is low.

In the 4-T cell, the transistor of the inverter that is low is turned on and a direct current flows from V_{CC} to ground through the load resistor and transistor of that inverter. In either state, therefore, the current required to retain data in the cell is determined by the resistance of the load resistor. This current is multiplied by the RAM's density (in bits) to determine the total current for the entire array of cells.

Selection of this resistance value is critical: if the resistance is too low, the standby supply current of the RAM will be unacceptably high; if too high, the cell will be marginally stable and data may be lost.

This is further complicated by the inverse relation between temperature and the polysilicon resistor's resistance. The resistance of the intrinsic polysilicon pull-up resistor can decrease by several orders of magnitude as the temperature rises from room temperature to the high end of the military-temperature range.

As in the 4-T cell, the output of one inverter in the 6-T cell is always low. There is, however, no direct current path from V_{CC} to ground, because the complementary p-channel pull-up transistor in the CMOS inverter is turned off whenever the n-channel pull-down transistor is turned on. There is only the small leakage current through the channels of the transistors in the full CMOS latch.

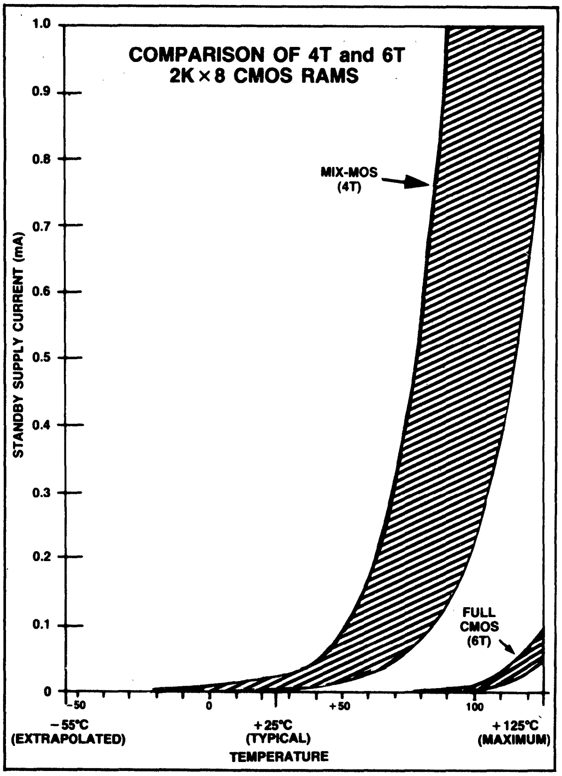
This current is due to thermally generated carriers and increases as temperature increases. In both the 4-T and 6-T cells, the standby current is greatest at high temperature, but that is where the similarity ends.

The 6-T cell invariably operates at lower current than 4-T cells. For example, military-temperature, mix-MOS, 2k × 8 RAMs are commonly specified at 900 to 10,000 µA maximum standby supply current. By contrast, similar full-CMOS 6-T-cell RAMs are commonly specified at 50 to 100 µA. At room temperature, the mix-MOS part has a typical supply current of 4 to 20 µA, while the 6T RAM typically operates at 0.01 µA or less (see graph).

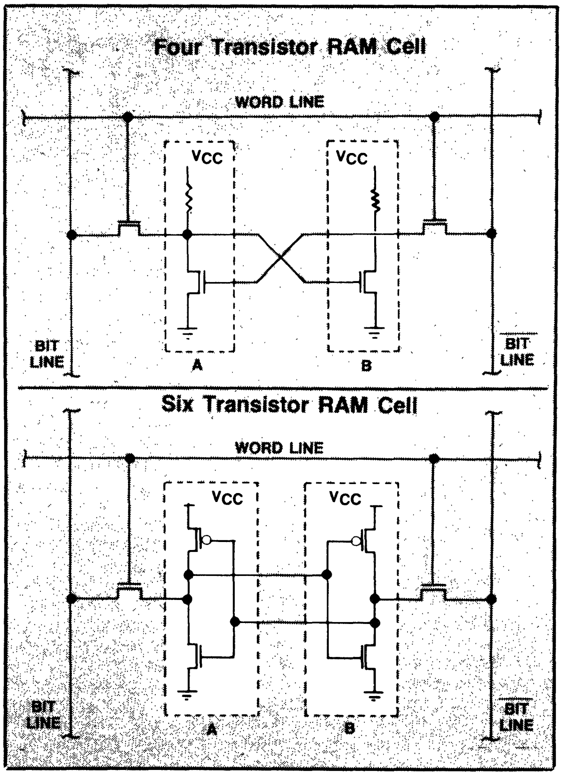
Cell Stability

Another important factor in CMOS RAM performance is cell stability. If the resistance of the internal pull-up resistors in a 4-T cell is too high, the cell can behave like a dynamic RAM cell and data could be lost because there are no refresh cycles. It is also possible for the data to change when reading a marginally stable cell, especially if the bit lines are not properly precharged or equalized before reading the cell. This limitation can reduce the speed or operating-temperature range of mix-MOS RAMs.

Finally, cell stability is essential to



While standby current requirements increase with temperature for both 4-T and 6-T cells, the rate of increase is far greater for 4-T cells. The data is for 2k × 8 CMOS RAMs.



Although 4-T and 6-T RAMs operate similarly, they differ in the load devices making up the data-storage latch. It results in 6-T RAM cells operating at lower current than 4-T cells.

prevent soft errors due to alpha particles given off by trace radioactive elements contained in IC-packaging materials. When a high-energy alpha particle strikes a device, a large number of electron-hole pairs are generated. If this occurs in the vicinity of a reverse-biased junction, the electron-hole pairs give rise to a transient current pulse. In the high-impedance 4-T cell, this transient, and the resultant changes in the internal voltage levels, may cause the cell to change state, resulting in data loss.

6-T cells are inherently more stable than 4-T cells. Even under worst-case conditions, the p-channel pull-up transistors have a lower impedance when turned on than that of the load resistors of the 4-T cell. Therefore, it is more difficult to pull the high side of the latch in a 6T cell low if, for example, the bit lines are not precharged and equalized prior to reading the cell.

Also, the p-channel pull-up transistors are able to source sufficient current to ensure that data are not lost when the cell is struck by an alpha particle. This has been verified in tests where an alpha-particle source was placed on the exposed surface of a 2k × 8 full CMOS RAM for 24 hours without data loss.

Finally, there is evidence which strongly suggests that cell stability may be important in determining the tolerance of the RAM to gamma radiation. During extensive radiation testing done throughout the industry, several types of full-CMOS 6-T RAMs have shown tolerance to total doses of radiation in excess of 10k rads (silicon), with some parts remaining functional after exposures greater than 40k rads. This is significant when compared to the performance of mix-MOS RAMs, which failed at total doses of less than 6k rads. **EET**

Ken Lyons is an applications engineer in Harris Corp.'s Semiconductor Digital Products Division, Melbourne, Fla.

CMOS

Harris Quality and Reliability

9

PAGE

Harris Quality and Reliability

Introduction

The Product Assurance Department at Harris Semiconductor Products Group is responsible for assuring that the quality and reliability of all products shipped to customers meet their requirements. During all phases of product fabrication, there are many independent visual and electrical checks performed by Product Assurance personnel.

Prior to shipment, a final inspection is performed at Quality Assurance Plant Clearance to insure that all requirements of the purchase order and customer specifications are met.

The following military documents provide the foundation for HARRIS Product Assurance Program.

MIL-M-38510D	"General Specifications of Microcircuits"
MIL-STD-883	"Test Methods and Procedures for Microelectronics"
NASA Publication 200-3	"Inspection System Provisions"
MIL-C-45662	"Calibration System Requirements"
MIL-I-45208	"Inspection System Requirements"

The Harris Semiconductor Reliability and Quality Manual, which is available upon request, describes the total function and policies of the organization to assure product reliability and quality. All customers are encouraged to visit the Harris Semiconductor facilities and survey the deployment of the Product Assurance function.

Quality Control

The Quality Control Department consists of Process Control with Chemical Mix as an available supporting service.

Process Quality Control is responsible for quality engineering and controls in the wafer processing modules, assembly, mask and materials production areas, and electrical wafer probe.

The primary responsibilities of Process Quality Control are:

a. To establish and maintain effective controls for monitoring manufacturing processes and equipment

b. to provide rapid feedback of information concerning the state of control

c. to initiate, design, and develop statistically controlled experiments to further improve product reliability and quality levels.

Statistical control charts on processes and operating procedures are used in the manufacturing areas and in the evaluation of process and product parameters utilized to qualify new processes.

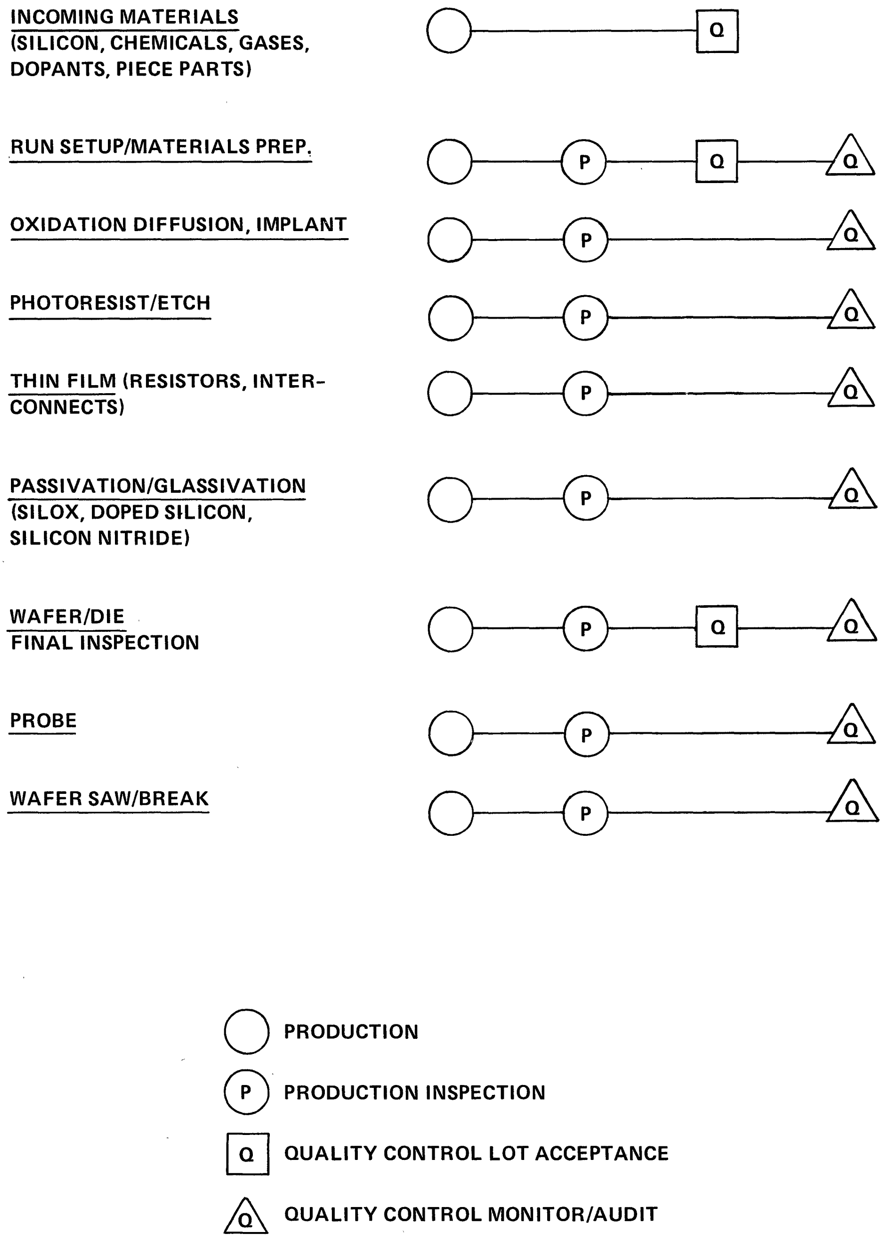
When necessary, fixed gate inspections are permanently employed to assure specified quality levels.

On a regular basis, process audits are performed to verify conformance to operating procedures.

Statistical control charts are maintained on processes and workmanship for all phases of assembly and environmental testing.

PROCESS CONTROL

WAFER FABRICATION - GENERAL PROCESS FLOW



Quality Assurance

The primary responsibility of the Quality Assurance Department is to assure that all delivered products meet the rigid standard of reliability and quality of Harris Semiconductor Products Group. The Quality Assurance department is responsible for process control and product quality from product assembly to shipment. Random sampling of products at specified points and intervals is used to ensure quality. This includes performance and analysis of sample electrical testing (Group A) and environmental and life testing (Groups B, C and D). In addition, mechanical and visual inspections specified by the Quality Assurance Test Plans, as well as customer and military specifications are performed. The random selection and distribution of samples, the routing of devices through specified testing and adherence to inspection programs are controlled and implemented by Quality Assurance.

All packaged microcircuits are marked by a code indicating the date the lot was sealed. This code provides product traceability and meets customer date coding requirements. Traceability is maintained through lot acceptance, testing and shipment to the customer.

Reliability

RELIABILITY PROCEDURES

Harris Semiconductor Products Group employs a comprehensive approach to reliability evaluation to ensure that reliability is designed and built into all products. This approach is referred to as the Reliability Evaluation Procedures and outlines the basic guidelines for evaluation of the total inherent reliability capability of all products types. The Reliability Evaluation Procedures are applied as an overlay during the early product development phase, subsequent prove-in via preproduction and final maturity in the manufacturing of all new product types. They also provide guidelines for evaluation of new process technologies deployed in all applicable products. The Reliablity Evaluation Procedures also encompass a package qualification procedure, and the "Add-on" program which is a quarterly reliability monitor of all process groups. These documents are available upon request.

The HARRIS CMOS Product line has had a continual evolution of new and enhanced processes. From SAJI I (Self Aligned Junction Isolated) to the most recent SAJI V process. There has been an ongoing effort to increase performance, density and reliability. The current RAM products (4K and up) along with the microprocessors and peripheral families utilize the SAJI IV, scaled SAJI IV, and SAJI V processes. Table 1 is a summary of recent reliability data taken on the various SAJI processes. Table 2 lists the activation energies of the most common defects associated with the CMOS products. Table 3 gives a breakdown of field returns by failure mechanism.

At Harris, accelerated life Tests are utilized to estimate the filed failure rate of our product. A typical life test consists of 200 devices tested at +125°C to +150°C ambient, dynamic operation, 5.5V to 6.5V, for 1000 hours. All failures are carefully analyzed to determine derating factors back to +55°C ambient, 5.5 volts operation are determined.-

Derating factor = D. F. = $e - \left(\frac{E_A}{K}\right)\left(\frac{1}{T_2} - \frac{1}{T_1}\right)$ where

EA = Activation Energy
K = Boltzman's Constant
T2 = Life Test Junction Temp.
T1 = Junction Temp. at +55°C Ambient

Projected field failure rates are calculated at 60% and 95% confidence levels. This means that either 60% or 95% of the product will meet or exceed the reliability demonstrated in the test. We also ensure that the failure rate is decreasing with time to prevent any wear-out mechanism from reaching our customers.

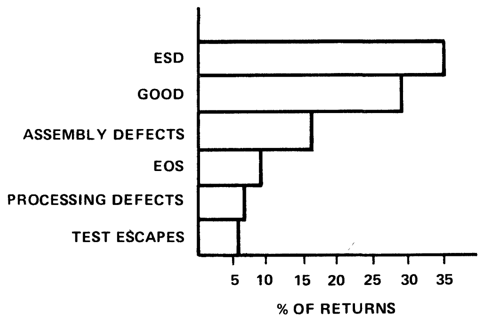
TABLE I. SUMMARY OF RELIABILITY DATA

SAJI Process Type	No. Of Devices	Device Hours (+125°C)	No. Of Failures	E_A (eV)	Failure Rate (%/K Hours) @ T_A = +55°C Observed	60% Confidence	95% Confidence
I	2,046	4,019,046	1 4 6	1.0 0.6 0.5	0.0007	0.001	0.002
II	1,515	1,791,668	2 1 2 2	1.0 0.7 0.6 0.5	0.004	0.013	0.028
III	440	938,844	0	—	0.002	0.005	0.015
IV	687	740,464	1 2	0.6 0.5	0.020	0.025	0.044
Scaled IV	1740	3,387,860	21 2 3 6	1.0 0.7 0.6 0.5	0.012	0.015	0.025

TABLE II. CMOS PRODUCTS - ACTIVATION ENERGY

Failure Mechanism	Activation Energy (E_A)
Oxide Defects	0.5ev
Defective Apertures	0.6ev
Photoresist Flaws	0.7ev
Assembly Defects	0.8ev
Ionic Contamination	1.0ev

TABLE III. FIELD RETURNS BY FAILURE MECHANISM



NOTE: Returned units are approximately 1% of the total shipped.

Harris Takes the Total Approach to Quality

Quality and reliability do not occur by accident in microcircuit manufacturing. They can be achieved only as a result of precise design, capable manufacturing methods, carefully controlled production processes and accurate screening and testing. Quality and reliability must be totally designed and built into the product. They are not characteristics that can be added after manufacture. They must be part and parcel of the flow from the original design through final assembly and test.

The major steps affecting microcircuit reliability and quality are:

- Initial circuit selection and design.
- Selection of package materials and design.
- Die layout and geometry.
- Raw material inspection and QC.
- Wafer/die production process and controls.
- Die/package assembly and controls.
- Screening and test procedures.

Harris Standard Flows

Harris Semiconductor offers a variety of standard product flows which cover the myriad of application environments our customers experience. These flows run the gambet of low cost commercial parts to fully qualified JAN microcircuits. All of these grades have one thing in common. They result from meticulous attention to quality, starting with design decisions made during product development and ending with the labeling of shipping containers for delivery to our customers. The standard flows offered are:

Dash 5 : Electrical performance guaranteed from 0°C to +70°C.

Dash 9 : Electrical performance guaranteed from -40°C to +85°C.

Dash 9+ : Dash 9 plus burn-in.

Dash 2* : Electrical performance guaranteed from -55°C to +125°C.

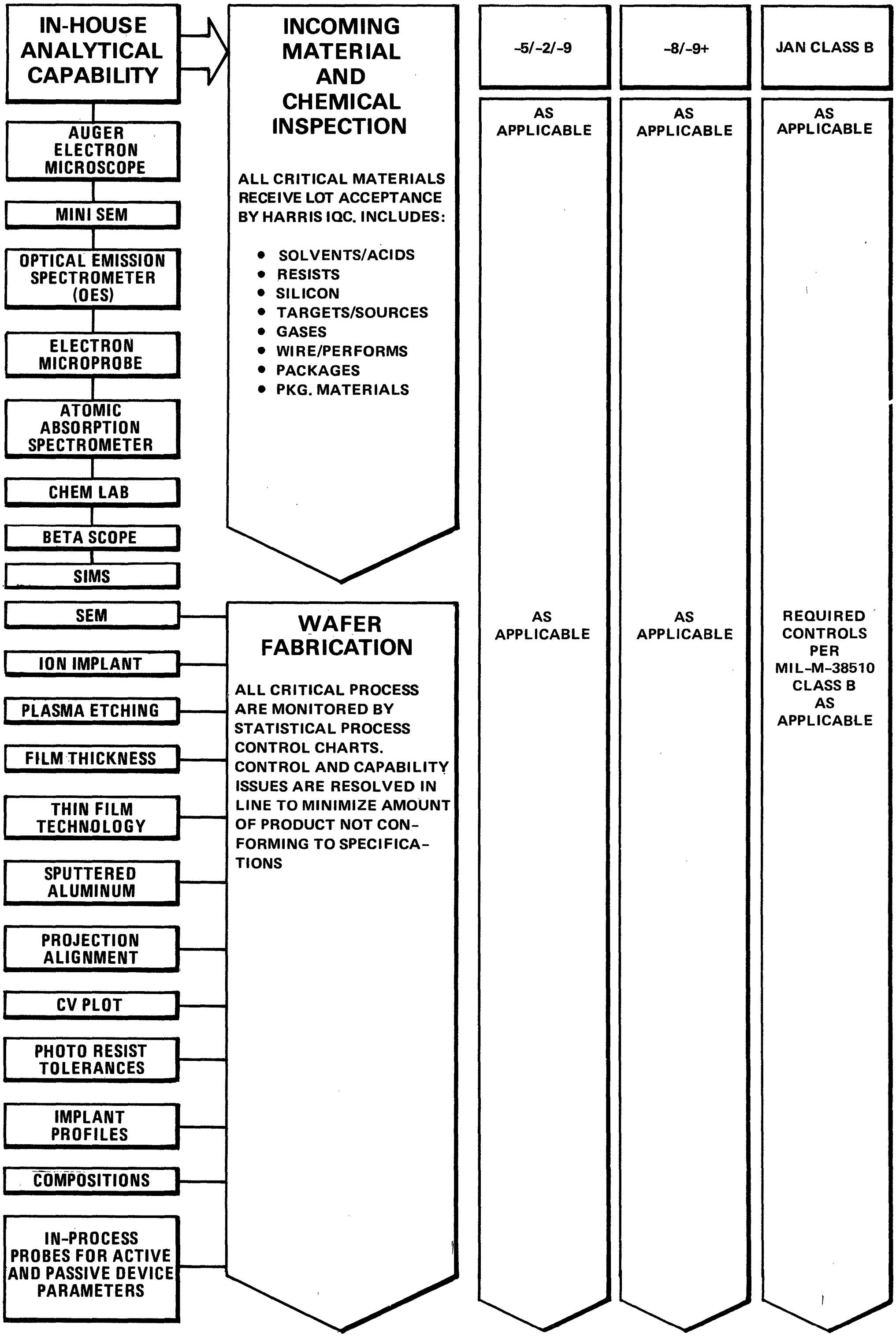
Dash 8* : Electrical performance guaranteed from -55°C to +125°C with burn-in and PDA testing.

JAN Class B : Fully qualified and certified microcircuit manufactured per Mil-M-38510 requirements.

Details of the individual process requirements are contained in the flow charts which follow.

*Harris reserves the option to perform alternate screening in accordance with MIL-STD-883 method 5004 paragraph 3.3 on DASH 2 and DASH 8 products.

Harris Semiconductor Standard Processing Flows



(1) T_A = -55°C to +125°C for all grades

Harris Semiconductor Standard Processing Flows

LASER TRIMMING AT BOTH PACKAGE AND WAFER LEVELS

HIGH/ROOM TEMP PROBE TEST

Step	-5/-2/-9	-8/-9+	JAN Class B
PROBE/DICE PREPARATION	VISUAL INSPECTION WITH QC MONITOR	VISUAL INSPECTION WITH QC MONITOR	VISUAL INSPECTION PER MIL-STD-883. METHOD 2010. CONDITION B, WITH QC MONITOR

ASSEMBLY (1)

◆ = Operation
★ = QA Monitor

PRE-SEAL WASH IN LAMINAR FLOW

DIE ATTACH CONTROL

WIRE BOND CONTROL

PRE-SEAL VISUAL INSPECTION IN CLASS 100 LAMINAR FLOW

PARTICLE IMPACT NOISE DETECTION (PIND) AS REQUIRED

Step	-5/-2/-9	-8/-9+	JAN Class B
◆ Lead Frame Clean	YES	YES	YES
◆ Pre-Seal Clean	AS REQUIRED	AS REQUIRED	YES
◆ Die and Frame Attach Control	YES	YES	YES
◆ Wire Bond	YES	YES	YES
★ QA Wire Bond Control	4-HOUR	4-HOUR	4-HOUR
◆ Pre-Seal Inspect	YES	YES	PER MIL-STD-883 METHOD 2010, CONDITION B
★ QA Pre-Seal Inspect	YES	YES	YES
(GSI) GSI Inspect	NO	NO	YES
◆ Cerdip Sealing	YES	YES	YES
★ QA Seal Control	YES	YES	YES
◆ Stabilization Bake	NO	AS APPLICABLE	YES
◆ Temperature Cycle	YES	YES	YES
◆ Centrifuge	YES	YES	YES
◆ Tin-Plating	YES	YES	YES
★ QA Tin-Plating Inspect	YES	YES	YES
◆ Fine Leak Test	YES	AS APPLICABLE	YES
◆ Gross Leak Test	YES	AS APPLICABLE	YES
◆ PIND Test 100%	AS APPLICABLE	AS APPLICABLE	AS APPLICABLE
◆ Frame Removal	YES	YES	YES
◆ Load Shipping Tubes	YES	YES	YES
★ QA Final Inspect	YES	YES	YES
★ QA Documentation Inspect	NO	NO	YES

(1) Example for a Cerdip package part.

AC/DC SINGLE INSERTION TEST CAPABILITY; HIGH/LOW TEMP

BURN-IN

QUALITY CONFORMANCE GROUPS A, B, C, AND D AS REQUIRED

DELTAS PER SLASH SHEET REQUIREMENT IF APPLICABLE

IN-HOUSE PACKAGE MOISTURE MONITOR CAPABILITY

COMPUTERIZED LOT TRACEABILITY MONITORING SYSTEM

TEST (2)

◆ = Operation
★ = QA Monitor

TEST (2)	-5/-2/-9	-8/-9+	JAN Class B
◆ Electrical Test Sorting Operation	YES	YES	YES
★ QA Monitor	YES	YES	NO
◆ Serialize	NO	NO	Group A and C Samples Only
◆ Pre Burn-In Electrical Test	NO	YES	YES
◆ Burn-In	NO	YES	160 HR @ +125°C, OR PER SLASH SHEET
◆ Post Burn-In Test	NO	YES	YES
◆ Apply Burn-In PDA (as applicable)	NO	NO for -9+ YES for -8	PER SLASH SHEET
◆ Brand	YES	YES	YES
◆ External Visual	YES	YES	YES
★ Quality Conformance Inspection	GROUP A	GROUP A	GROUP A, B, C, D
◆ Final Data Review	NO	NO	YES

Package & Ship or Stock

(2) -5: 0°C to +70°C
-2/-8/JAN: -55°C to +125°C
-9/-9+: -40°C to +85°C

Advantages of Standard Flows

Wherever feasible, and in accordance with good value engineering practice, the IC user should specify device grades based on one of the five standard Harris manufacturing flows. These are more than adequate for the overwhelming majority of applications and may be utilized quite effectively if the user engineer bases his designs on the standard data book or slash sheet (as applicable) electrical limits.

Some of the more important advantages gained by using standard as opposed to custom flows are as follows:

- Lower cost than the same or an equivalent flow executed on a custom basis. This results from the higher efficiency achieved with a constant product flow and the elimination of such extra cost items as special fixturing, test programs, additional handling, and added documentation.
- Faster delivery. The manufacturer often can supply many items from inventory and, in any case, can establish and maintain a better product flow when there is no need to restructure process and/or test procedures.
- Increased confidence in the devices. A continuing flow of a given product permits the manufacturer to monitor trends which may bear on end-product performance or reliability and to implement corrective action, if necessary.
- Reduction of risk. Since each product is processed independent of specific customer orders, the manufacturer absorbs production variability within its scheduling framework without major impact on deliveries. In a custom flow, a lot failure late in the production cycle can result in significant delays in delivery due to the required recycling time.

Despite the advantages of using standard flows, there are cases where a special or custom flow is mandatory to meet design or other requirements. In such cases, the Harris Marketing groups stand ready to discuss individual customer needs and, where indicated, to accomodate appropriate custom flows.

Quality Beginning to End

There are several significant elements which comprise Harris Semiconductor's approach to quality that don't show on a process flow chart. Some of these are as follows:

INITIAL CIRCUIT SELECTION AND DESIGN

Once operational characteristics and parameter limits have been defined there are many different circuit configurations capable of conforming to them. Harris designers are tasked to choose those which are capable of meeting the required performance specifications with maximum reliability.

Powerful computer aided design (CAD) techniques are applied in developing the original concepts and detailed schematics, with computer modeled circuit simulation used to corroborate projected product performance. Monte Carlo methods, and other simulation techniques are also used, as appropriate to achieve specific objectives.

Regardless of the circuit approach selected, high reliability, top performance, and maximum potential yield to the required specifications are the governing criteria.

Individual active device types and component values are selected to provide optimum circuit performance and to minimize sensitivity to parametric changes which may occur with aging or as a result of environmental conditions.

Since most Harris products are sold into military, industrial and commercial end use applications most circuits are designed to meet military temperature range requirements at the outset. This results in more capable products introduced to all segments of the marketplace.

Die Layout and Geometry

Conformance with good layout practice is a must, for consistently reliable devices cannot be assembled from poorly designed chips. Therefore, the IC layout phase at Harris is controlled by ground rules which establish the "do's" and "don'ts" for each manufacturing process. These rules define dimensions and toleranced to insure product immunity to process variations, while maximizing product reliability under worst-case stress conditions. Computerized ground rule software packages are used by the chip designers to assure dimensional adherence of diffusion windows as well as interconnect width and spacing. Automatic checkout procedures confirm that the product conforms to the established ground rules.

Raw Material Inspection and QC

Acknowledging that Hi-Rel, high performance devices can be manufactured only by using top quality materials, Harris subjects incoming materials, piece parts and supplies to documented tests and inspections. The techniques used are selected for optimum evaluation of the materials checked to ensure full compliance with Harris internal specifications. Close coordination with the suppliers is maintained to assure a reliable supply of quality materials.

Wafer Die Production Process and Controls

Harris has a wide range of state-of-the-art wafer and die processing capabilities, permitting the circuit designer to choose the optimum production technique for each type of device.

Statistical process control charts are employed to maximize the visibility of wafer lot variability during production. These charts take the form of $\overline{X}/R$ charts for variables data and $\overline{C}/\overline{p}$ charts for attributes data. Typical process control points include diffusion, thin film, photo resist steps as well as inspection points or electrical device measurements. The goal of the control charts is three fold:

- Isolate and eliminate special causes of variability to preclude the production of wafers with a process which is not operating correctly.
- Define the natural limits of variability in a process to determine its capability in light of engineering expectation.
- Provide a reference baseline for process enhancements or changes to improve capability or reduce cost.

With high reliability an integral part of its manufacturing philosphy, Harris Semiconductor does not have separate production lines for standard and JAN devices. Rather, all Harris devices of a given type are manufactured on the same line. Product grades are selected by the application of screening tests and inspection from the same generic process flows in wafer fab.

Die/Package Assembly and Controls

Each major process operation (mount, bond, seal, trim) is carefully monitored by in-process quality control steps. In addition, many mechanical and environmental tests are implemented during the die/package assembly stage. The specific controls and tests utilized at each step are in strict compliance with the applicable standards for the device reliability class designation.

Burn-In

100% burn-in is a screening procedure used when applicable to detect devices subject to infant mortality failure modes. Biases are applied to simulate worst-case operational conditions, permitting the identification and elimination of marginal units.

The applied voltage levels, operational state, temperature and test period vary with the type of device and reliability class, as governed by the applicable standards. Electrical test of the device is performed both prior to and after the burn-in period.

Electrical Screening and Test Procedures

While many factors are critical in the production of I. C. devices, the electrical screening and test procedures, are critical to matching product performance to customer need. All products receive 100% electrical test per the data sheet requirements for each product type. In addition product lots received a battery of QA inspections and tests to assure compliance with Harris production standards.

Reliability Assessment and Enhancement

At Harris, reliability assurance is a dynamic program with the primary and ultimate goal of securing full product performance throughout its usage life. Each manufacturing phase from original design to final packaging is subject to continuous review, analysis, and evaluation, with modifications introduced as needed to improve product performance and reliability. There are three important sources of reliability data:

1. Initial qualification
2. Add on life
3. Field failure history

New Products/Processes/Packages

Two requirements are imposed on the product development phase of new circuits and processes. First is the use of proper process methodology, design techniques, and layout practices. New designs are reviewed throughout the course of their development for conformance to the constraints defined by process ground rules. These rules document the results of years of experimentation and experience and reflect a relatively conservative approach to process capability and technology. Second is demonstration of reliability performance of a new product or process through a series of stress tests designed to accelerate typical failure mechanisms in integrated circuits. Qualification requirements are illustrated in Table I for a variety of product/process/package maturity conditions. These tests are executed by the Harris Reliability organization for each new product/package/process before circuits are committed to the marketplace. Failure rate predictions are made based on test results. More importantly, failure analysis results are fed back into design and process engineering organizations to generate corrective action (if applicable) and enhance product performance. Each new product entry must meet minimum failure rate standards to qualify for sale to customers.

"Add On"

An important source of reliability information is performance of established products through extended life testing under worst-case operating conditions. Failure rate predictions for specific products or product types are available on request via Harris Semiconductor Reliability bulletins;

Accelerated life test are utilized to estimate the expected field failure rate of our products. Life tests are conducted periodically on regular production samples. Sample sizes are typically 200 units which are operated at 125^{o}C at nominal supply voltages and with forcing and loading conditions simulating typical application environments. Where possible, operating conditions are structured to provide maximum thermal and electrical acceleration of the natural failure mechanisms found in I. C. devices.

All rejected devices are carefully analyzed and activation energies are assigned based on the observed failure mechanisms. There rates are then computed based on thermal derating factors per the Arrhenius equation. The results are reported in the Harris Reliability bulletins based on derating to +55°C operations and nominal supply conditions. Failure rates are reported at the 60% confidence level and the 95% confidence level.

Finally, life tests are monitored at mid-point intervals to assure that failure rates are decreasing and that no wearout mechanisms are at work.

TABLE IV. TEST MATRIX

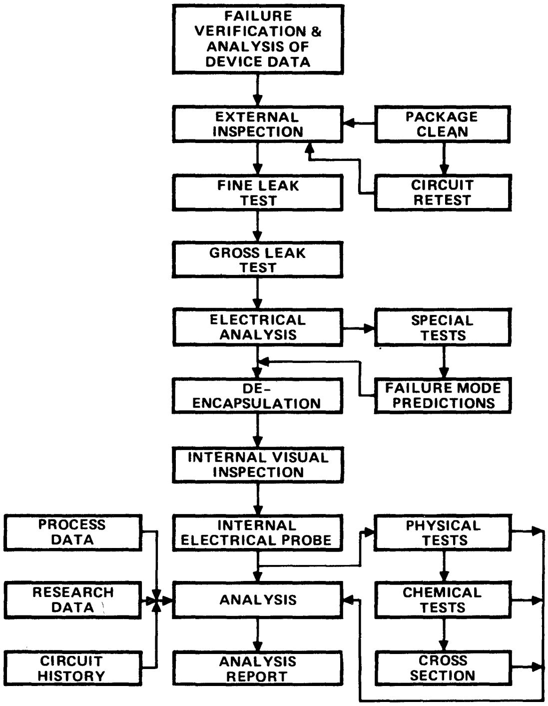
Design Package Process	New New New	New New Est.	New Exist New	New Exist Est.	Exist New New	Exist New Est.	Exist Exist New	Exist Exist Est.
Abuse Tests 20 Units	X	X	X	X	X		X	X
Max. Ratings 20 Units: No Failures	X		X	X	X		X	X
86/86 or Autoclave 50 Units: No Failures	X	X	X		X	X	X	
Constr. Analysis 5 Units: No Failures	X	X	X	X	X	X	X	X
Centrifuge 50 Units: No Failures	X	X			X	X		
Ele. Charac. 20 Units: No Failures	X	X	X	X	X		X	X
ESD Immunity 20 Units: No Failures	X	X	X	X	X		X	X
Fig. Test 20 Units: No Failures	X	X	X	X	X		X	
HTOL Sample Groups	200 (min)	200 (min)	200 (min)	200 (min)	200 (min)	200 (min)	200 (min)	200 (min)
Latch-up 20 Units: No Failures	X	X	X	X	X			
Lead Integrity 20 Units: No Failures	X	X			X	X	X	X
Mech. Charac. 20 Units: No Failures	X	X			X	X		
Mech. Schock 50 Units: No Failures	X	X			X	X		
Moisture Resist 50 Units: No Failures	X	X			X	X		
θja/θjc 20 Units	X	X			X	X		
Solvent Resistance 4 Units: No Failures	X	X			X	X		
Solderability 20 Units: No Failures	X	X			X	X		
Temperature Cycling 50 Units: No Failures	X	X			X	X		
Thermal Shock 50 Units: No Failures	X	X			X	X		
Vibration 50 Units: No Failures	X	X			X	X		

Field Failures

The final source of continued reliability assessment and enhancements is the analysis of defects on products returned by our customer.

An exhaustive analysis of device failures is a requirement of the Harris reliability program. After failure confirmation by electrical test, the device is processed through the standard failure analysis procedure outlined below.

FAILURE ANALYSIS FLOW



ESD (ELECTROSTATIC DISCHARGE)

Since the introduction of MOS, manufacturers have searched for effective and safe ways of handling this voltage sensitive device. High input impedance of CMOS, coupled with gate-oxide breakdown characteristics, result in susceptibility to electrostatic charge damage.

Figure 1 shows a cross-section of a silicon gate MOS structure. Note the very thin oxide layer (≈500-1000Å) present under the gate material. Actual breakdown voltage for this insulating layer ranges from 70V to 100V.

Handling equipment and personnel, by simply moving, can generate in excess of 10kV of static potential in a low humidity environment. Thus, static voltages, in magnitudes sufficient to damage delicate MOS input gate structures, are generated in most handling environments.

A failure occurs when a voltage of sufficient magnitude is applied across the gate oxide causing it to breakdown and destruct. Molten material then flows into the void creating a short from the gate to the underlying silicon. Such shorts occur either at a discontinuity in doping concentration, or at a defect site in the thin oxide. If no problems appear in the oxide, breakdown would most likely occur at gate/source, or gate/drain intersection coincidence due to the doping concentration gradient.

Noncatastrophic degradation may result due to overstressing a CMOS input. Sometimes an input may be damaged, but not shorted. Most of these failures relate to damage of the protection network, not the gate, and show up as increased input leakage.

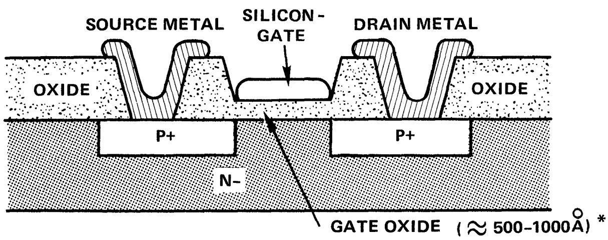


Figure 1 — Silicon-gate PFET structure cross-section shows the heavily doped source and drain region. They are separated by a narrow gap over which lies a thin-gate oxide and gate material.

*NOTE: 1Å (Angstrom = 10^{-8} cm)

Voltage Limiting Input Protection

During the evolution of monolithic MOS, manufacturers developed various protection mechanisms that are an integral part of the circuit. However, several of these earlier techniques have been replaced by improved methods now in use. The object of most of these schemes is to prevent damage to input-gate structures by limiting applied voltages.

Recent CMOS designs employ a dual-diode concept in their input protection networks. Figure 2 illustrates such a protection circuit.

One characteristic of junction-isolated CMOS protection circuits is the ≈ 200Ω current limiting resistor. Cross sectional area of the metallization leading to the resistor, and the area of the resistor are, therefore, designed to absorb discharge energy without sustaining permanent damage. This dual-diode protection has proved very effective and is the most commonly used method in production today.

HARRIS INPUT GATE PROTECTION

To protect input device gates against destructive overstress by static electricity accumulating during handling and insertion of CMOS products, Harris provides a protection circuit on all inputs. The general configuration of this protection circuit is shown in Figure 2.

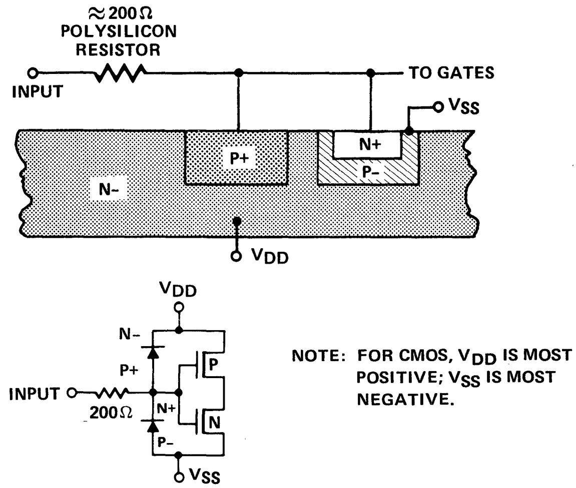


Figure 2 — Junction isolated dual-diode protection networks are most commonly used in today's CMOS circuits.

Both diodes to the V_{DD} and V_{SS} lines have breakdown voltages averaging between 35 and 40 volts. Excessive static charge accumulated on the input pin is thus effectively discharged through these diodes which limit the voltage applied from gate to drain and source. The 200 ohm resistor provides current limiting during discharge. Depending on the polarity of the input static charge and on which of the supply pins are grounded, the protective diodes may either conduct in the forward direction or breakdown in the reverse direction.

In order to test this concept, step stress tests have been performed at Harris using an approximate equivalent circuit to simulate the static charge encountered in handling operations. The equivalent circuit consists of a 100pF capacitor in series with a 1.5K ohm resistor and is considered the rough equivalent of a human body. Step stressing takes the form of charging the capacitor to a given voltage and then discharging it into an input pin of the CMOS device under test according to the sequence given in MIL-M-38510.

Stress Voltage	Cumulative Failures
500	0
700	0
1000	0
1400	1
1600	3
1800	4

These results indicate that the input protection used for Harris CMOS products provides adequate protection against static electricity based on the limits specified in MIL-M-38510.

There are two trade-offs to consider when fabricating an input protection scheme, namely effectiveness of the overvoltage protection and performance of the overall circuit. It is obvious that increasing the series resistance and capacitance at an input limits current and this, in turn, increases the input protection's ability to absorb the shock of a static discharge. However, such an approach to protection can have a significant effect on circuit speed and input leakage. The input protection selected must therefore provide a useful performance level and adequate static-charge protection.

Commonly used MOS-input protection circuits all have basic characteristics that limit their effectiveness. The zener diodes, or forward-biased pn-junctions, employed have finite turn-on times too long to be effective for fast rise-time conditions. A static discharge of 1.5kV into a MOS input may bring the gate past its breakdown level before the protection diodes or zener becomes conductive.

Actual turn-on times of zeners and pn-diodes are difficult to determine. It is estimated that they are a few nanoseconds and a few tens of picoseconds, respectively. A low-impedance static source can easily produce rise times equal to or faster than these turn-on times. Obviously the input time constant required to delay buildup of voltage at the gate must be much higher for zener diodes or other schemes having longer turn-on times.

Consider an example. Figure 3 shows a test circuit that simulates the discharge of a 1.5kV static charge into a CMOS input. Body capacitance and resistance of the average person is represented by a 100pF capacitor through 1.5kΩ. Switch A is initially closed, charging 100pF to 1.5kV with switch B open. Switch A is opened, then B is closed, starting the discharge. With the 1.5KΩ x 5pF time constant to limit the charge rate at the DUT input, it would take approximately 350psec to charge to 70V above V_{DD}. Diode turn-on time is much shorter than 350psec, hence the gate node would be clamped before any damage could be sustained.

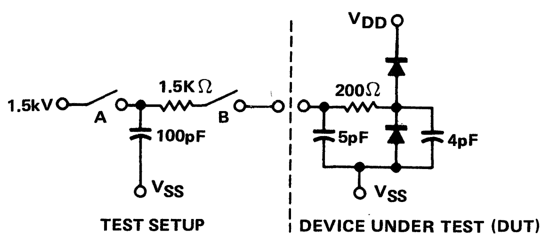


Figure 3 — Input protection network test setup illustrates how diode clamping prevents excessive voltages from damaging the CMOS device.

HANDLING RULES

There is no completely foolproof system of chip-input protection presently in production. If static discharge is of high enough magnitude, or of sufficiently short rise-time, some damage or degradation may occur. It is evident, therefore, that proper handling procedures should be adopted at all times.

Elimination or reduction of static charge can be accomplished as follows:

- Use conductive work stations. Metallic or conductive plastic tops on work benches connected to ground help eliminate static build-up.
- Ground all handling equipment.
- Ground all handling personnel with a conductive bracelet through 1MΩ to ground.
- The 1MΩ resistor will prevent injury.
- Smocks, clothing, and especially shoes of certain insulating materials (notably nylon) should not be worn in areas where devices are handled. These materials, highly dielectric in nature, will hold or aid in the generation of a static charge.
- Control relative humidity to as high a level as practical. A higher level of humidity helps bleed away any static charge as it collects.
- Ionized air blowers reduce charge build-up in areas where grounding is not possible or desirable.
- Devices should be in antistatic conductive carriers during all phases of transport. If antistatic carriers are used the devices and carriers should be in a static shielding bag.
- In automated handling equipment, the belts, chutes or other surfaces the leads contact should be of a conducting nature. If this is not possible, ionized air blowers may be a good alternative.

Harris currently ships all CMOS products in Benstat ™ tubes placed inside static shielding bags. Packing materials are all antistatic.

THE FORWARD-BIAS PHENOMENON

Monolithic CMOS integrated circuits employ a single-crystal silicon wafer into which FET sources and drains are implanted. For complex functions many thousands of transistors may be required and each must be electrically isolated for proper operation.

Junction techniques are commonly used to provide the required isolation – each switching node operating reverse-biased to its respective substrate material. Additionally, as previously mentioned, protection diodes are provided to prevent static-charge related damage where inputs interface to package pins. Forward-biasing any of these junctions with or without power applied may result in malfunction, parametric degradation, or damage to the circuit.

High currents resulting from an excessive forward-bias can cause severe overheating localized to the area of a junction. Damage to the silicon, overlying oxide and metallization can result.

BIPOLAR PARASITICS

Care must always be exercised not to forward-bias junctions from input or output pads.

A complex and potential defect phenomenon is the interaction of a npn/pnp combination a la SCR (Figure 5). Forward-biasing the base-emitter junction of either bipolar component can cause the pair to latch up if $\beta npn \times \beta pnp \geq 1$. The resultant low impedance between supply pins can cause fusing of metallization or over-dissipation of the chip.

Figure 5 shows how an SCR might be formed. The p+ diffusion labeled INPUT is connected to aluminum metallization and bonded to a package pin. Biasing this point positive with respect to V_{DD} supplies base drive to the pnp through R2. Although gain of these lateral devices is normally very low, sufficient collector current may be generated to forward-bias and supply substantial base current to the vertical npn parasitic. Once the pair has been activated, each member provides the base current required to sustain the other. A latched condition will be maintained until power is removed or circuit damage disables further operation.

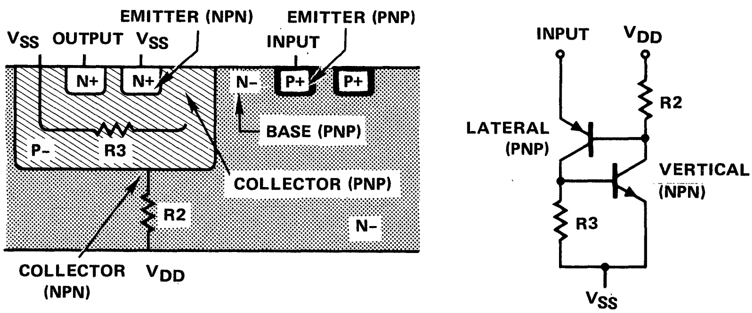


Figure 5 — Improper biasing can latch-up this SCR configuration. A p+ guard ring is commonly used to kill lateral pnp action. This ring is diffused into the surface at the junction of p- and n- silicon.

DESIGN RULES EQUALLY IMPORTANT AS HANDLING RULES

A system using CMOS devices must have reliability designed in. No amount of testing can guarantee long term reliability when poor design practices are evident.

- Never apply signals which exceed maximum ratings to a CMOS circuit before or after power has been turned on (to prevent latch-up)
- Supply filter capacitance should be distributed such that some filtering is in close proximity to the supply pins of each package. Testing has shown 0.01 μF/package to be effective in filtering noise generated by most CMOS functions.
- CMOS signal lines are terminated at the driving end by a relatively high impedance when operating at the low end of the supply voltage range. This high-impedance termination results in vulnerability to high-energy or high-frequency noise generated by bipolar or other non-CMOS components. Such noise must be held down to manageable levels on both CMOS power and signal lines.
- Where CMOS must interface between logic frames or between different equipments, ground differences must be controlled in order to maintain operation within absolute maximum ratings.

- Capacitance on a CMOS input or output will result in a forward-bias condition when power is turned off. This capacitance must discharge through forward-biased input or output to substrate junctions as the bus voltage collapses. Excessive capacitance (thousands of pF) should be avoided as discharging the stored energy may generate excessive current densities during power-down.
- Where forward-biasing is inevitable, current limiting should be provided. Current should not be permitted to exceed 1mA on any package pin excluding supply pins.

All CMOS is susceptible to damage due to electrical overstress. It is the user's responsibility to follow a few simple rules in order to minimize device losses.

First, select a source for the CMOS device that employs an effective input protection scheme. This will allow a greater margin of safety at all levels of device handling since the devices will not be quite so prone to static charge damage. Next, he should apply a sound set of handling and design rules. At minimum, this will eliminate electrical stressing or hold it to manageable levels.

With an effective on-chip protection scheme, good handling procedures and sound design, users should not lose any CMOS devices to electrical overstress.

CMOS

Hi-Reliability Products

10

PAGE

Harris Hi-Rel Products

Harris has developed standard flows which should satisfy most Hi-Rel requirements. Produced in accordance with established manufacturing flows, the standard Harris Hi-Rel grades and their indicated areas of application are as follows:

Dash 5: Electrical performance guaranteed from 0°C to +70°C.

Dash 9: Electrical performance guaranteed from -40°C to +85°C.

Dash 9+: Dash 9 plus 96 hours of burn-in.

Dash 2: Electrical performance guaranteed from -55°C to +125°C.

Dash 8: Electrical performance guaranteed from -55°C to +125°C plus 160 hours of burn-in with PDA of 5%. 100% preseal visual per Mil-Std-883C, Method 2010.

/883: Mil-Std-883C — compliant product: contact the factory or local Harris sales office for details on availability and specifications

JAN Class B: Fully qualified and certified microcircuit manufactured per Mil-M-38510 requirements.

Details of the individual process requirements are contained in the flow charts on pages 9-8, 9-9 and 9-10 of this data book.

CMOS Microprocessor and Support Circuits

HI-REL PART NUMBER	FUNCTION	PIN COUNT	PAGE REF.
8/16-BIT MICROPROCESSORS			
MD80C86/B	16-Bit CMOS Microprocessor (5MHz)	40	3-2
MD80C86-2/B	16-Bit CMOS Microprocessor (8MHz)	40	3-2
MD80C88/B	8-Bit CMOS Microprocessor (5MHz)	40	3-25
80C86/88 PERIPHERAL CIRCUITS			
MD82C50A/B	CMOS Asynchronous Communication Element	40	3-68
MD82C52/B	CMOS Serial Communication Interface	28	3-88
MD82C54/B	CMOS Programmable Interval Timer	24	3-98
MD82C55A/B	CMOS Programmable Peripheral Interface	40	3-113
MD82C59A/B	CMOS Priority Interrupt Controller	28	3-133
MD82C37A/B	CMOS DMA Controller	40	3-50
80C86/88 BUS SUPPORT CIRCUITS			
MD82C82/B	CMOS Octal Latching Bus Driver	20	3-147
MD82C83H/B	CMOS Octal Latching Inverting Bus Driver	20	3-152
MD82C84A/B	CMOS Clock Generator/Driver	18	3-157
MD82C85/B	CMOS Static Clock Controller/Generator	24	3-164
MD82C86H/B	CMOS Octal Bus Transceiver	20	3-181
MD82C87H/B	CMOS Octal Inverting Bus Transceiver	20	3-181
MD82C88/B	CMOS Bus Controller	20	3-186
MD82C89/B	CMOS Bus Arbiter	20	3-193
SERIAL COMMUNICATION CIRCUITS			
HD-4702-8	CMOS Bit Rate Generator	16	4-3
HD-6402-8	CMOS UART	40	4-8
HD-6406-8	CMOS Programmable Asynchronous Communication Interface	40	4-14
HD-6409-8	CMOS Manchester Encoder-Decoder	20	4-30
HD-15530-8	CMOS Manchester Encoder-Decoder	24	4-40
HS-15530RH	CMOS Manchester Encoder-Decoder (Radiation Resistant)	24	
HD-15531-8	CMOS Manchester Encoder-Decoder	40	4-47
HS-3182	CMOS ARINC 429 Bus Interface Line Driver Circuit	16	
HS-3282	CMOS ARINC 429 Bus Interface Circuit	40	
CMOS PROGRAMMABLE LOGIC			
HPL-16LC8-8	Programmable Logic	20	6-3
HPL-16RC4-8	Programmable Logic	20	6-10
HPL-16RC6-8	Programmable Logic	20	6-10
HPL-16RC8-8	Programmable Logic	20	6-10
HPL-82C339-8	Programmable Chip Select Decoder (PCSD)	24	6-20
HPL-82C338-8	Programmable Chip Select Decoder (PCSD)	20	6-25
HPL-82C139-8	Programmable Chip Select Decoder (PCSD)	16	6-30
HPL-82C138-8	Programmable Chip Select Decoder (PCSD)	16	6-35

CMOS Static RAMs

HI-REL PART NUMBER	CONFIGURATION	PIN COUNT	ACCESS TIME	STANDBY CURRENT-ICCSB	DATA RET. CURRENT-ICCDR	OPERATING CURRENT-ICCOP	PAGE REF.
1K — SYNCHRONOUS							
HM-6508-8	1K x 1	16	250ns	10μA	10μA	4mA/MHz	2-4
HM-6508B-8	1K x 1	16	180ns	10μA	5μA	4mA/MHz	2-4
HM-6518-8	1K x 1	18	250ns	10μA	10μA	4mA/MHz	2-10
HM-6518B-8	1K x 1	18	180ns	10μA	5μA	4mA/MHz	2-10
HM-6551-8	256 x 4	22	300ns	10μA	10μA	4mA/MHz	2-16
HM-6551B-8	256 x 4	22	220ns	10μA	10μA	4mA/MHz	2-16
HM-6561-8	256 x 4	18	300ns	10μA	10μA	4mA/MHz	2-22
HM-6561B-8	256 x 4	18	220ns	10μA	10μA	4mA/MHz	2-22
4K — SYNCHRONOUS							
HM-6504-8	4K x 1	18	300ns	50μA	25μA	7mA/MHz	2-28
HM-6504B-8	4K x 1	18	200ns	50μA	25μA	7mA/MHz	2-28
HM-6504S-8	4K x 1	18	120ns	50μA	25μA	7mA/MHz	2-28
HM-6514-8	1K x 4	18	300ns	50μA	25μA	7mA/MHz	2-39
HM-6514B-8	1K x 4	18	200ns	50μA	25μA	7mA/MHz	2-39
HM-6514S-8	1K x 4	18	120ns	50μA	25μA	7mA/MHz	2-39
16K — SYNCHRONOUS							
HM-6516-8	2K x 8	24	200ns	100μA	50μA	10mA/MHz	2-50
HM-6516B-8	2K x 8	24	120ns	50μA	25μA	10mA/MHz	2-50
16K — ASYNCHRONOUS							
HM-65162-8	2K x 8	24	90ns	100μA	40μA	70mA	2-55
HM-65162B-8	2K x 8	24	70ns	50μA	20μA	70mA	2-55
HM-65262-8	16K x 1	20	85ns	100μA	40μA	50mA	2-62
HM-65262B-8	16K x 1	20	70ns	50μA	40μA	50mA	2-62
HM-65262S-8	16K x 1	20	55ns	50μA	40μA	50mA	2-62
64K — ASYNCHRONOUS							
HM-65642-8	8K x 8	28	150ns	250μA	100μA	80mA	2-71
CMOS RAM MODULES							
HM-6564-8	64K	40	350ns	800μA	400μA	28/56mA/MHz	2-76
HM-92560-8	256K	48	150ns	500μA	350μA	15/30mA/MHz	2-99
HM-92570-8	Buffered 256K	48	250ns	600μA	450μA	15/30mA/MHz	2-106
HM-8808A-8	8K x 8	28	150ns	900μA	400μA	70mA	2-85
HM-8808AB-8	8K x 8	28	120ns	250μA	125μA	70mA	2-85
HM-8808AS-8	8K x 8	28	100ns	250μA	125μA	70mA	2-85
HM-8808-8	8K x 8	28	150ns	900μA	400μA	70mA	2-85
HM-8808B-8	8K x 8	28	120ns	250μA	125μA	70mA	2-85
HM-8808S-8	8K x 8	28	100ns	250μA	125μA	70mA	2-85
HM-8816H-8	16K x 8	28	85ns	800μA	370μA	400mA	2-94
HM-8816HB-8	16K x 8	28	70ns	800μA	370μA	400mA	2-94

CMOS RADIATION HARDENED RAMS

PART NUMBER	CONFIGURATION	PIN COUNT	ACCESS TIME	STANDBY CURRENT-ICCSB	DATA RET. CURRENT-ICCDR	OPERATING CURRENT-ICCOP
HS-6504RH	4K x 1	18	300ns	100μA	50μA	7mA/MHz
HS-6508RH	1K x 1	16	300ns	100μA	—	4mA/MHz
HS-6514RH	1K x 4	18	200ns	250μA	50μA	7mA/MHz
HS-6551RH	256 x 4	22	300ns	100μA	—	4mA/MHz
HS-6564RH RAM Module	16K x 4 or 8K x 8	40	350ns	800μA	—	32mA/MHz

CMOS Fuse Link PROMs

PART NUMBER	CONFIGURATION	PIN COUNT	ACCESS TIME	STANDBY CURRENT-ICCSB	DATA RET. CURRENT-ICCDR	OPERATING CURRENT-ICCOP	PAGE REF.
HM-6641-8	512 x 8	24	250ns	100μA	—	15mA/MHz	2-113
HM-6616-8	2K x 8	24	120/90ns	100μA	—	15mA/MHz	2-118

CMOS

Ordering and Packaging 11

PAGE

11 ORDERING & PACKAGING

Ordering Information

Harris products are designed by "Product Code". When ordering, please refer to products by the full code.

PRODUCT CODE

H M 1 — 65162 B — 9

PREFIX
- H (Harris)

FAMILY
- D : Digital
- M : Memory
- PL : Programmable Logic

PACKAGE
- 1 : Ceramic DIP
- 1B : Brazed Seal
- 3 : Plastic DIP
- 4 : Leadless Carriers
- 5 : Ceramic Substrate
- 6 : Slimline
- 0 : Chip Form

PART NUMBER
- 155XX : CMOS Manchester Encoder/Decoder
- 65XXX : CMOS RAM
- 66XX : CMOS PROM
- 9XXX : CMOS Module
- 88XX : CMOS RAM Module

PERFORMANCE GRADE
- B : High Speed
- C : Relaxed Specification
- S : Very High Speed

TEMPERATURE
- 2 : -55°C to +125°C
- 5 : 0°C to +75°C
- 6 : 100% 25°C Probe (Dice Only)
- 8 : -55°C to +125°C with burn-in
- 9 : -40°C to +85°C
- 9+ : -40°C to +85°C with burn-in

80CXX FAMILY PRODUCT CODE

M D 80C86 — 2 /B

TEMPERATURE RANGE
- C : 0°C to +75°C
- I : -40°C to +85°C
- M : -55°C to +125°C
- X : +25°C

PACKAGE TYPE
- P : Plastic DIP
- D : Ceramic DIP
- X : Unpackaged Device
- R : Leadless Chip Carrier
- S : Plastic Leaded Chip Carrier

PART NUMBER
- 80CXX: CMOS Microprocessor
- 82CXX: CMOS Peripherals

SPEED DESIGNATION

- B : -55°C to +125°C with burn-in
- + : -40°C to +85°C with burn-in

SPECIAL ORDERS

For best availability and price, it is urged that standard "Product Code" devices be specified which are available worldwide from authorized distributors. Where enhanced reliability is needed, note standard "Dash 8" screening described in this Data Book. Harris application engineers may be consulted for advice about suitability of a part for a given application.

If additional electrical parameter guarantees or reliability screening are absolutely required, a Request for Quotation and Standard Control Drawing should be submitted through the local Harris Sales Office or Sales Representative. Many electrical parameters cannot be economically tested, but can be assured through design analysis, characterization, or correlation with other parameters which have been tested to specification limits. These parameters are labeled "Sampled and guaranteed, but not 100% tested".

Harris reserves the right to decline to quote, or to request modification to special screening requirements.

MILITARY PRODUCTS

Harris offers a full line of products that are processed in full conformance to the provisions of military standards including MIL-STD-883C for Class B parts. The requirements for these products are controlled in one or two ways:

1. Government standards (such as JAN Slash Sheets or DESC Drawings)
2. Harris Standards

The Harris standard Military Products Program is based on its experience in the JAN program. JAN certifications are maintained on our production and Product Assurance operations and form the basis of our MIL-STD-883 conformance program. These areas are regularly audited by Harris and by the U.S. government to assure compliance.

Selected products have been qualified to the MIL-M-38510 requirements and are listed on the QPL. There are also a number of Harris parts which are specified by DESC Drawings. In addition, Harris offers many products as fully conformant to MIL-STD-883 via an internal standards program. Please contact the factory or your local Harris Sales Office or Representative for the latest status on military standard compliant product offerings.

The information in this catalog is intended to describe the expected part behavior under certain operating conditions. The product descriptions contained in this catalog, particularly in the area of electrical performance, do not precisely reflect those of our JAN qualified, DESC or MIL-STD-883 compliant products and are not necessarily test requirements for Harris military standard compliant products.

The actual product test requirements for JAN and DESC parts are described in the appropriate MIL-M-38510 slash sheet or DESC Drawing, respectively. In addition, Harris will be issuing product data sheets for MIL-STD-883 compliant parts which will describe actual test requirements. These compliant products will be identified by a "/883" suffix on the part number (e.g. HX1-XXXX/883). Please contact the factory or your local Harris Sales Office or Representative for details on MIL-STD-883 compliant product offerings.

Dice Information

GENERAL INFORMATION

Harris CMOS Products are available in chip form to the hybrid micro circuit designer. The standard chips are DC electrically tested at +125°C to the data sheet limits for the commercial device and are 100% visually inspected. Packaging for shipment consists of waffle pack carriers plus an anti-static cushioning strip for extra protection.

The hybrid industry has rapidly become more diversified and stringent in its requirements for integrated circuits. To meet these demands Harris has several options additional to standard chip processing available upon request at extra cost. For more information consult the nearest Harris Sales Office.

CHIP ORDERING INFORMATION

Standard and special chip sales are direct factory order only. The minimum order on all sales is $250.00 per line item. Contact the local Harris Sales Office for pricing and delivery on special chip requirements.

MECHANICAL INFORMATION

Dimensions: All chip dimensions nominal with a tolerance of ± .003". Nominal chip thickness is .011" ± .002".

Bonding Pads: Minimum bonding pad size is .004" x .004" unless otherwise specified.

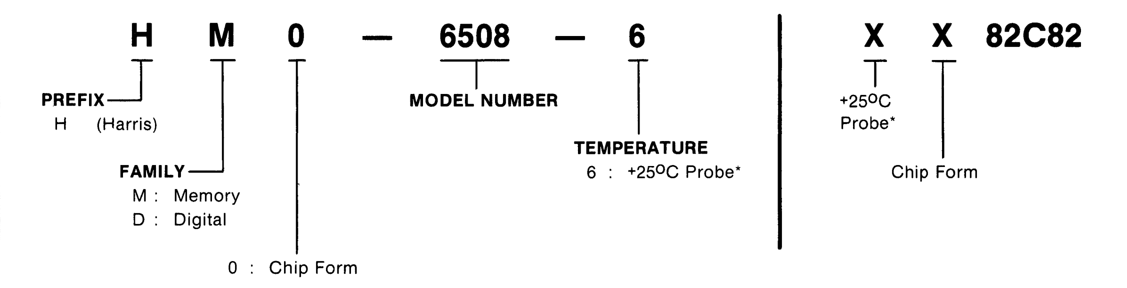
ELECTRICAL INFORMATION

CMOS: Die substrate must be electrically connected to VCC through conductive die attach, to assure proper electrical operating characteristics.

DIE GEOMETRIES AND DIMENSIONS

May be obtained by contacting the factory of your local Harris Sales Office.

PRODUCT CODE EXAMPLES



* Contact Harris for availability of -2 (-55°C to +125°C) dice.

Package Availability

PART NUMBER	CERDIP	PLASTIC DIP	CERAMIC LEADLESS CHIP CARRIER	PLASTIC LEADED CHIP CARRIER
CMOS 80C86 FAMILY				
80C86	DE, DF	FF	EA	NG
80C88	DE, DF	FF	EA	NG
82C37A	5H	FE	EA	NF
82C50A	DE	FE	—	NF
82C52	1M	FJ	LX	NE
82C54	5F	FG	EH	NE
82C55A	4H	FD	EG	NH
82C59A	1M	FJ	LX	ND
82C82	5Z	7M	EX	NB
82C83H	5M	7F	EE	NC
82C84A	4N	7W	EE	NB
82C85	DC	—	LX	ND
82C86H	5M	7F	EE	NC
82C87H	5M	7F	EE	NC
82C88	5Z	7M	ET	NB
82C89	5Z	7H	ET	NB
1K RAM				
HM-6508	5C	7I	—	—
HM-6518	5E	7D	LA	—
HM-6551	4M	FK	—	—
HM-6561	4N	7D	LA	—
4K RAM				
HM-6504	5E	7D	LB	—
HM-6514	5E	7D	LB	—
16K RAM				
HM-6516	5F, 5J	7Z	EC	—
HM-65162	5F	7Z	EC	—
HM-65262	5M	7F	EJ	—
64K RAM				
HM-65642	DD	—	ED	—
CMOS PROM				
HM-6641	5J, DC	—	LR	—
HM-6616	5J, DC	—	EC	—
CMOS HPL				
HPL-16LC8	5M, 1K*	—	EE	—
HPL-16RC8/6/4	5M, 1K*	—	EE	—
HPL-82C339	DC	—	LX	—
DATA COMMUNICATION				
HD-15530	4K	7C	LX	—
HD-15531	5H	FE	EG	—
HD-6408	—	7C	—	—
HD-6409	5Z	7M	ET	—
HD-6406	4H	FE	EA	NF
HD-6402	5H	FD	—	—
HD-4702	4Z	7H	LA	—

*Sidebrazed Dual-in-Line Package

Package Availability

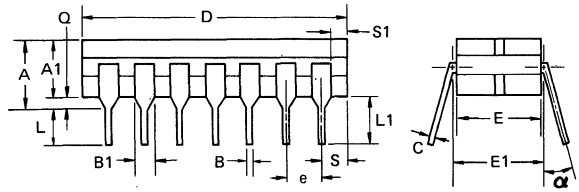
PART NUMBER	MODULE SUBSTRATE
RAM MODULE	
HM-6564	MA
HM-8808	MJ
HM-8808A	MJ
HM-8816H	MK
HM-8816	MJ
HM-92560 (32K x 8)	MD
HM-92560 (16K x 16)	MD
HM-92570	MG

11 ORDERING & PACKAGING

Package Configuration

DC, 4N, 4Z, 5C, 5E, 5M, 5Z

CERAMIC DUAL-IN-LINE .300

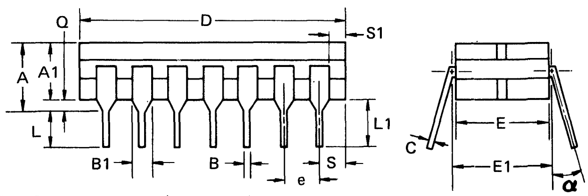


PKG. TYPE	LEAD COUNT	DIM. A	DIM. A1	DIM. **B	DIM. B1	DIM. **C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. L1	DIM. Q	DIM. S	DIM. S1	DIM. α
4Z	*16	– / .200	.140 / .170	.016 / .023	.050 / .070	.008 / .015	.753 / .785	.265 / .285	.290 / .310	.090 / .110	.125 / .180	.150 / –	.015 / .060	– / .080	.005 / –	0° / 15°
5C	*16	– / .200	.140 / .170	.016 / .023	.050 / .070	.008 / .015	.753 / .785	.285 / .305	.300 / .320	.090 / .110	.125 / .180	.150 / –	.015 / .060	– / .080	.005 / –	0° / 15°
4N,5E	*18	– / .200	.140 / .170	.016 / .023	.050 / .070	.008 / .015	.882 / .915	.285 / .305	.300 / .320	.090 / .110	.125 / .180	.150 / –	.015 / .060	– / .098	.005 / –	0° / 15°
5M,5Z	*20	– / .200	.140 / .170	.016 / .023	.050 / .070	.008 / .015	.940 / .970	.285 / .305	.300 / .320	.090 / .110	.125 / .180	.150 / –	.015 / .060	– / .080	.005 / –	0° / 15°
DC	24 SLIM	– / .200	.150 / .180	.016 / .023	.050 / .070	.008 / .015	1.240 / 1.280	.285 / .305	.300 / .320	.090 / .110	.125 / .180	.150 / –	.000 / .035	– / .098	.005 / –	0° / 15°

* End leads are half leads where B remains the same and B1 is .035 – .045
** Dimensions B and C maximum limits are increased by 0.003 for solder dip finish

4M

CERAMIC DUAL-IN-LINE .400

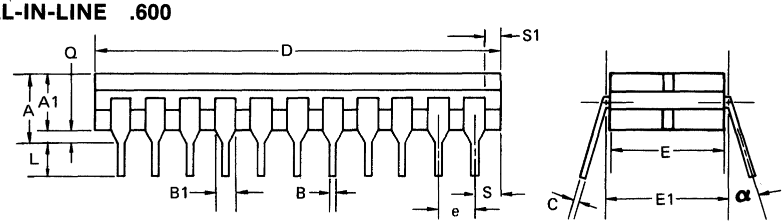


PKG. TYPE	LEAD COUNT	DIM. A	DIM. A1	DIM. *B	DIM. B1	DIM. *C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. L1	DIM. Q	DIM. S	DIM. S1	DIM. α
4M	22	– / .225	.150 / .180	.016 / .023	.050 / .070	.008 / .015	1.055 / 1.085	.375 / .390	.395 / .415	.090 / .110	.125 / .180	.150 / –	.015 / .060	– / .080	.005 / –	0° / 15°

* Dimensions B and C maximum limits are increased by 0.003 for solder dip finish

DD, DE, DF, 1M, 4H, 4K, 5F, 5H, 5J

CERAMIC DUAL-IN-LINE .600



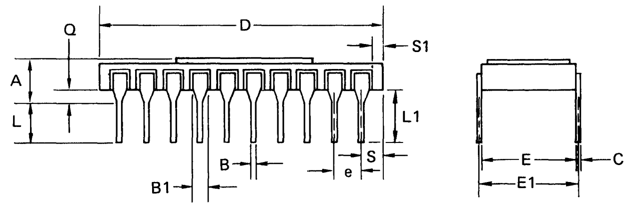
PKG. TYPE	LEAD COUNT	DIM. A	DIM. A1	DIM. *B	DIM. B1	DIM. *C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. L1	DIM. Q	DIM. S	DIM. S1	DIM. α
4K,5F 5J	24	– / .225	.150 / .180	.016 / .023	.050 / .070	.008 / .015	1.24 / 1.27	.515 / .535	.595 / .615	.090 / .110	.125 / .180	.150 / –	.015 / .060	– / .098	.005 / –	0° / 15°
DD,1M	28	– / .225	.160 / .190	.016 / .023	.050 / .070	.008 / .015	1.44 / 1.47	.515 / .535	.595 / .615	.090 / .110	.125 / .180	.150 / –	.015 / .060	– / .098	.005 / –	0° / 15°
DE,DF 4H,5H	40	– / .225	.160 / .200	.016 / .023	.050 / .070	.008 / .015	2.035 / 2.096	.515 / .535	.595 / .615	.090 / .110	.125 / .180	.150 / –	.015 / .060	– / .098	.005 / –	0° / 15°

*Dimension B and C maximum limits are increased by 0.003 for solder dip finish

NOTE: 1) All Dimensions are $\frac{\text{Min.}}{\text{Max.}}$ 2) Dimensions are in inches. BSC: Basic Standard Centers

Package Configuration

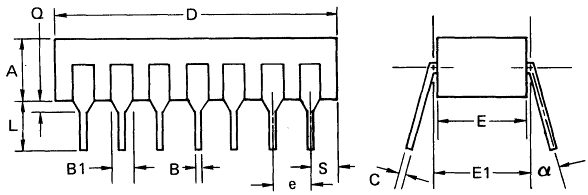
1K
SIDEBRAZE DUAL-IN-LINE .300



PKG. TYPE	LEAD COUNT	DIM. A	DIM. *B	DIM. B1	DIM. *C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. L1	DIM. Q	DIM. S	DIM. S1
1K	20	.110 .150	.016 .023	.045 .060	.008 .015	.990 1.010	.280 .300	.290 .310	.100 BSC	.125 .180	.150 –	.025 .045	– .080	.005 –

* Dimensions B and C maximum limits are increased by 0.003 for solder dip finish

7D, 7F, 7H, 7I, 7M, 7W
PLASTIC DUAL-IN-LINE .300

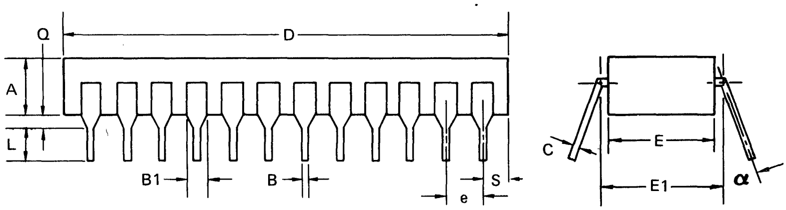


PKG. TYPE	LEAD COUNT	DIM. A1	DIM. **B	DIM. B1	DIM. **C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. Q	DIM. S	DIM. α
7H,7I	*16	.125 .140	.016 .023	.050 .070	.008 .015	.745 .785	.245 .265	.290 .310	.090 .110	.100 .150	.020 .040	.025 .035	0° 15°
7D,7W	18	.125 .140	.016 .023	.050 .070	.008 .015	.890 .930	.245 .265	.290 .310	.090 .110	.100 .150	.020 .040	.040 .060	0° 15°
7F,7M	20	.130 .145	.016 .023	.050 .070	.008 .015	1.020 1.060	.250 .270	.290 .310	.090 .110	.100 .150	.020 .040	.060 .080	0° 15°

* End leads are half leads where B remains the same and B1 is .035 – .045

** Dimensions B and C maximum limits are increased by 0.003 for solder dip finish

FK
PLASTIC DUAL-IN-LINE .400



PKG. CODE	LEAD COUNT	DIM. A1	DIM. *B	DIM. B1	DIM. *C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. Q	DIM. S	DIM. α
FK	22	.140 .170	.016 .023	.050 .070	.008 .015	1.09 1.13	.335 .355	.390 .410	.090 .110	.100 .150	.020 .040	.040 .080	0° 15°

* Dimensions B and C maximum limits are increased by 0.003 for solder dip finish

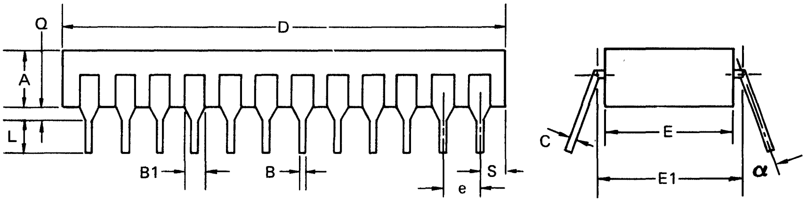
NOTE: 1) All Dimensions are $\frac{\text{Min.}}{\text{Max.}}$ 2) Dimensions are in inches.

BSC: Basic Standard Centers

Package Configuration

FD, FE, FF, FG, FJ, 7C, 7Z

PLASTIC DUAL-IN-LINE .600

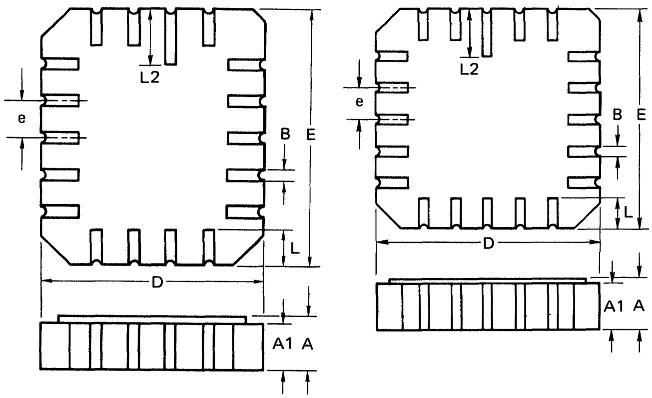


PKG. TYPE	LEAD COUNT	DIM. A1	DIM. *B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. Q	DIM. S	DIM. α
FG,7C 7Z	24	.145/.160	.016/.023	.050/.070	.008/.015	1.24/1.28	.540/.560	.590/.610	.090/.110	.100/.150	.020/.040	.045/.095	0°/15°
FJ	28	.145/.160	.016/.023	.050/.070	.008/.015	1.54/1.58	.540/.560	.590/.610	.090/.110	.100/.150	.020/.040	.110/.160	0°/15°
FD,FE FF	40	.145/.160	.016/.023	.050/.070	.008/.015	2.03/2.07	.540/.560	.590/.610	.090/.110	.100/.150	.020/.040	.070/.090	0°/15°

* Dimensions B and C maximum limits are increased by 0.003 for solder dip finish

EE, ET, EX, LA, LB

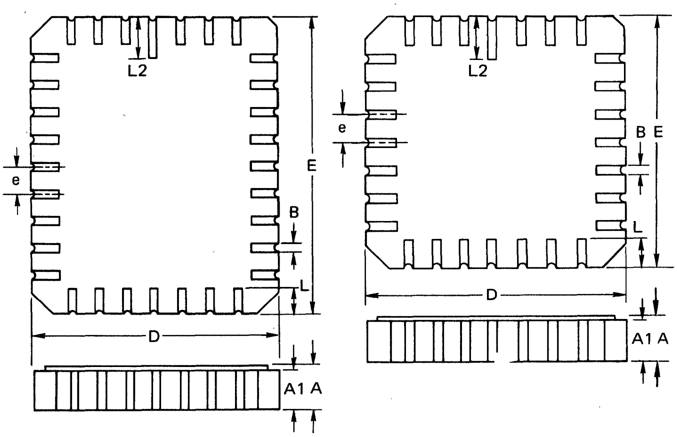
LEADLESS CHIP CARRIER 18R, 20SQ



PKG. TYPE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. D	DIM. E	DIM. e	DIM. L	DIM. L2
LA,LB	18 RECT.	.057/.075	.045/.060	.020/.030	.280/.295	.345/.360	.050 BSC	.035/.055	.090/.110
EE,ET EX	20 SQ.	.073/.089	.063/.077	.020/.030	.342/.358	.342/.358	.050 BSC	.042/.058	.075/.095

EC, ED, EH, EJ, LR, LX

LEADLESS CHIP CARRIER 20R, 28SQ, 32R



PKG. TYPE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. D	DIM. E	DIM. e	DIM. L	DIM. L2
EJ	20 RECT.	.073/.089	.063/.077	.020/.030	.284/.296	.419/.431	.050 BSC	.040/.055	.075/.110
EH,LR LX	28 SQ.	.073/.089	.063/.077	.015/.030	.445/.460	.445/.460	.050 BSC	.042/.058	.075/.095
EC,ED	32 RECT.	.073/.089	.063/.077	.022/.028	.442/.458	.545/.560	.050 BSC	.045/.055	.075/.085

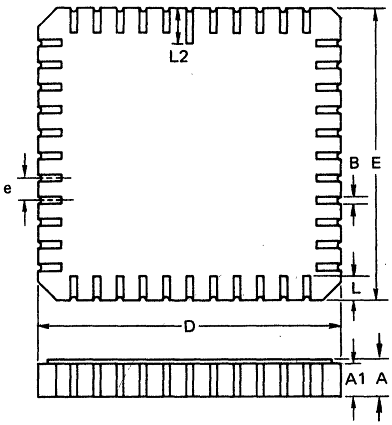
NOTE: 1) All Dimensions are Min./Max. 2) Dimensions are in inches.

BSC: Basic Standard Centers

Package Configuration

EA, EG

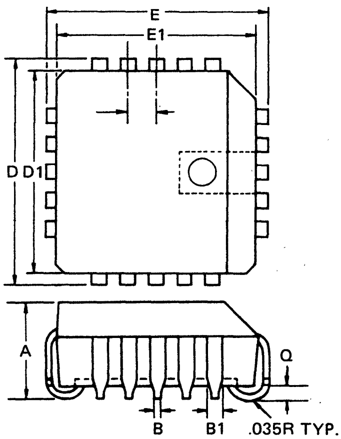
LEADLESS CHIP CARRIER 44SQ



PKG. TYPE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. D	DIM. E	DIM. e	DIM. L	DIM. L2
EA,EG	44 SQ.	.073 / .089	.063 / .077	.020 / .030	.643 / .662	.643 / .662	.050 / BSC	.042 / .058	.075 / .095

NB, NC, ND, NE, NF, NG, NH

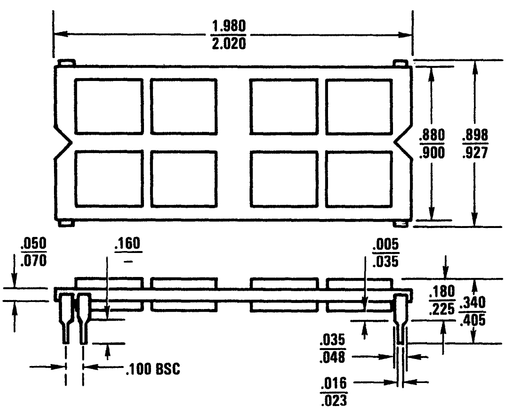
PLASTIC LEADED CHIP CARRIER ALL LEAD COUNTS



PKG. TYPE	LEAD COUNT	DIM. A	DIM. B	DIM. B1	DIM. D/E	DIM. D1/E1	DIM. e	DIM. Q
NB,NC	20 SQ.	.165 / .180	.013 / .021	.026 / .032	.385 / .395	.350 / .356	.050 / BSC	.025 / .045
ND,NE	28 SQ.	.165 / .180	.013 / .021	.026 / .032	.485 / .495	.450 / .456	.050 / BSC	.025 / .045
NF,NG NH	44 SQ.	.165 / .180	.013 / .021	.026 / .032	.685 / .695	.650 / .656	.050 / BSC	.025 / .045

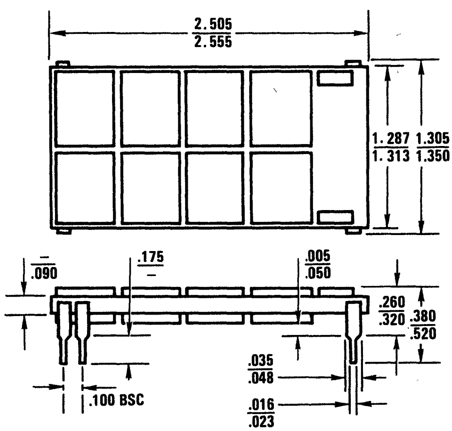
MA

MODULE SUBSTRATE HM-6564



MD

MODULE SUBSTRATE HM-92560

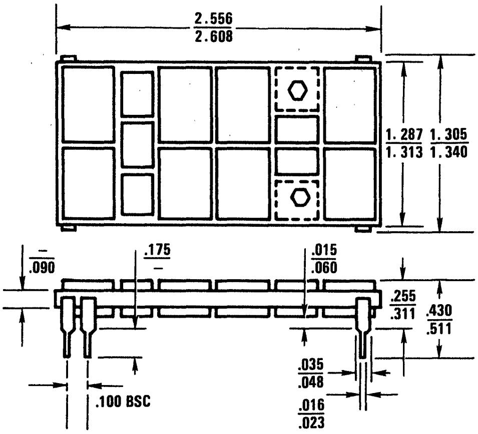


NOTE: 1) All Dimensions are Min./Max. 2) Dimensions are in inches.

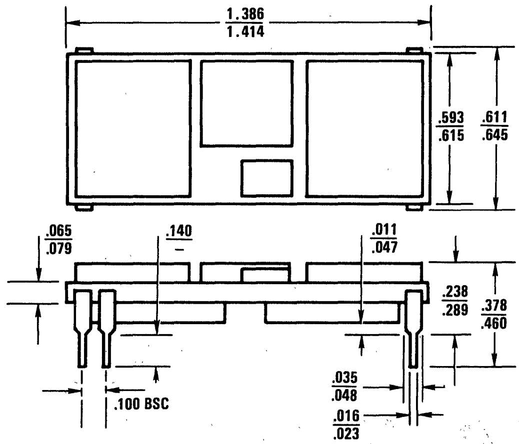
BSC: Basic Standard Centers

Package Configuration

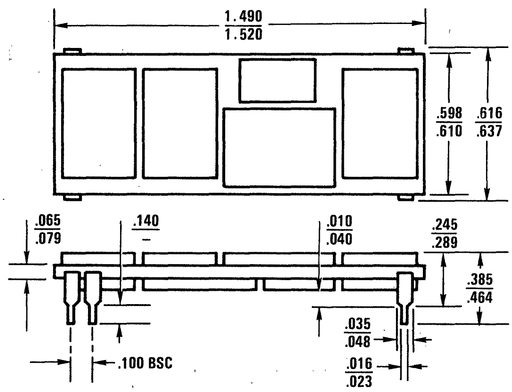
MG MODULE SUBSTRATE
HM-92570



MJ MODULE SUBSTRATE
HM-8808/08A



MK MODULE SUBSTRATE
HM-8816H



NOTE: 1) All Dimensions are $\frac{\text{Min.}}{\text{Max.}}$ 2) Dimensions are in inches. BSC: Basic Standard Centers

CMOS

Appendices 12

PAGE

Analog Products

Analog-to-Digital Converters

HI-574A	25μs, Complete 12-Bit A/D Converter with Microprocessor Interface
HI-674A	12μs, Complete 12-Bit A/D Converter with Microprocessor Interface
HI-774	8.5μs, Complete 12-Bit A/D Converter with Microprocessor Interface
HI-774A	7μs, Complete 12-Bit A/D Converter with Microprocessor Interface

Data Acquisition Module Products

HY-94741/42	Low Power Sampling 12-Bit A/D Converter with 8/16-Bit Microprocessor Interface
HY-9574	Sampling 12-Bit A/D Converter with 8/16-Bit Microprocessor Interface
HY-9590/91	Data Acquisition Front End
HY-9595/96	Programmable Gain Ampliifier with Multiplexed Inputs
HY-9674	Sampling 12-Bit A/D Converter with 8/16-Bit Microprocessor Interface
HY-9712	Complete 12-Bit Data Acquisition Subsystem

Digital-to-Analog Converters

HI-5618A/18B	8-Bit High Speed D/A Converter
HI-5610	10-Bit High Speed D/A Converter
HI-562A	12-Bit High Speed D/A Converter
HI-565A	12-Bit High Speed D/A Converter with Reference
HI-5660/60A	12-Bit High Speed D/A Converter
HI-5680	12-Bit D/A Converter with Reference (0°C to +70°C)
HI-5685/85A	12-Bit D/A Converter with Reference (-40°C to +85°C)
HI-5687	12-Bit D/A Converter with Reference (-55°C to +125°C)
HI-5811	Complete, Monolithic 12-Bit Latched D/A Converter
HI-7541	12-Bit Multiplying D/A Converter
HI-5690V	Fast 12-Bit V-DAC with Reference (0°C to +70°C)
HI-5695V	Fast 12-Bit V-DAC with Reference (-40°C to +85°C)
HI-5697V	Fast 12-Bit V-DAC with Reference (-55°C to +125°C)
HI-DAC16B/C	16-Bit D/A Converter

Multiplexers

SINGLE 8/DIFFERENTIAL 4 CHANNEL:

HI-508/509	Single 8/Differential 4 Channel CMOS Analog Multiplexer
HI-508A/509A	Single 8/Differential 4 Channel CMOS Analog MUX with Active Overvoltage Protection
HI-508LA/509LA	Latched Single 8/Differential 4 Channel CMOS Analog MUX with Overvoltage Protection
HI-518	Programmable Single 8/Differential 4 Channel CMOS High Speed Analog MUX
HI-548/549	Single 8/Differential 4 Channel CMOS Analog MUX with Active Overvoltage Protection
HI-1818A/1828A	Low Resistance Single 8/Differential 4 Channel CMOS Analog Multiplexer

SINGLE 16/DIFFERENTIAL 8 CHANNEL:

HI-506/507	Single 16/Differential 8 Channel CMOS Analog Multiplexer
HI-506A/507A	Single 16/Differential 8 Channel CMOS Analog MUX with Active Overvoltage Protection
HI-506LA/507LA	Latched Single 16/Differential 8 Channel CMOS Analog MUX with Overvoltage Protection
HI-516	Programmable Single 16/Differential 8 Channel CMOS High Speed Analog MUX
HI-546/547	Single 16/Differential 8 Channel CMOS Analog MUX with Active Overvoltage Protection

4 CHANNEL:

HI-524	4 Channel Video Multiplexer
HI-539	4 Channel Low Level Differential Multiplexer

Operational Amplifiers: High Slew-Rate

SINGLES:

HA-OP37	High Slew Rate, Precision, Low Noise Operational Amplifier
HA-2510/12/15	High Slew Rate Operational Amplifiers
HA-2520/22/25	High Slew Rate Operational Amplifiers
HA-2539	High Slew Rate, Wide Bandwidth Operational Amplifier
HA-2540	High Slew Rate, Wide Bandwidth Operational Amplifier
HA-2541	High Slew Rate, Unity Gain Stable Operational Amplifier
HA-2542	High Slew Rate, Power Operational Amplifier
HA-2620/22/25	Wide Bandwidth Operational Amplifiers
HA-5101/5111 ADVANCE	Low Noise, High Performance Operational Amplifiers
HA-5147	High Slew Rate, Precision, Low Noise Operational Amplifier
HA-5160/62	High Slew Rate, Wide Bandwidth J-FET Operational Amplifiers
HA-5190/95	High Slew Rate, Fast Settling Operational Amplifiers

DUALS:

HA-5112	Dual High Slew Rate, Low Noise Operational Amplifier

QUADS:

HA-2400/04/05	PRAM Four Channel Programmable Amplifiers
HA-2406	Digital Selectable Four Channel Operational Amplifier
HA-5114	Quad High Slew Rate, Low Noise Operational Amplifier

Operational Amplifiers: Wide Bandwidth

SINGLES:

HA-OP37	High Slew Rate, Precision, Low Noise Operational Amplifier
HA-2510/12/15	High Slew Rate Operational Amplifiers
HA-2520/22/25	High Slew Rate Operational Amplifiers
HA-2539	High Slew Rate, Wide Bandwidth Operational Amplifier
HA-2540	High Slew Rate, Wide Bandwidth Operational Amplifier
HA-2541	High Slew Rate, Unity Gain Stable Operational Amplifier
HA-2542	High Slew Rate, Power Operational Amplifier
HA-2600/02/05	General Purpose High Performance Operational Amplifiers
HA-2620/22/25	Wide Bandwidth Operational Amplifiers
HA-5147	High Slew Rate, Precision, Low Noise Operational Amplifier
HA-5160/62	High Slew Rate, Wide Bandwidth J-FET Operational Amplifiers
HA-5190/95	High Slew Rate, Fast Settling Operational Amplifiers

DUALS:

HA-5112	Dual High Slew Rate, Low Noise Operational Amplifier

QUADS:

HA-2400/04/05	PRAM Four Channel Programmable Amplifiers
HA-2406	Digital Selectable Four Channel Operational Amplifier
HA-5114	Quad High Slew Rate, Low Noise Operational Amplifier

Operational Amplifiers: Precision

HA-OP07	Precision Operational Amplifier
HA-OP27	Precision, Low Noise Operational Amplifier
HA-5134 ADVANCE	Precision Quad Operational Amplifier
HA-5147	High Slew Rate, Precision, Low Noise Operational Amplifier
HA-5170	J-FET Precision Operational Amplifier
HA-5180/80A	J-FET Precision, Low Bias Current Operational Amplifier

Analog Products

Operational Amplifiers: Low Power

SINGLES:

HA-5141	Ultra-Low Power Operational Amplifier
HA-5151/52/54	Low Power Operational Amplifiers

DUALS:

HA-5142	Dual Ultra-Low Power Operational Amplifier
HA-5151/52/54	Low Power Operational Amplifiers

QUADS:

HA-5144	Quad Ultra-Low Power Operational Amplifier
HA-5151/52/54	Low Power Operational Amplifiers

Operational Amplifiers: General Purpose

SINGLES:

HA-2600/02/05	General Purpose High Performance Operational Amplifiers
HA-5101/5111 ADVANCE	Low Noise, High Performance Operational Amplifiers

DUALS:

HA-5102	Dual Low Noise Operational Amplifier
HA-5112	Dual High Slew Rate, Low Noise Operational Amplifier

QUADS:

HA-2400/04/05	PRAM Four Channel Programmable Amplifiers
HA-2406	Digital Selectable Four Channel Operational Amplifier
HA-5104	Quad Low Noise Operational Amplifier
HA-5114	Quad High Slew Rate, Low Noise Operational Amplifier

Operational Amplifiers: High Voltage

HA-2640/45	High Voltage Operational Amplifiers

Operational Amplifiers: Addressable

HA-2400/04/05	PRAM Four Channel Programmable Amplifiers
HA-2406	Digital Selectable Four Channel Operational Amplifier

Operational Amplifiers: Current Buffers

HA-2630/35	High Performance Current Boosters
HA-5002	Wideband, High Slew Rate, High Output Current Buffer
HA-5033	Wideband, High Slew Rate Current Buffer

Operational Amplifiers: Sample and Hold

HA-2420-1	High Temperature Sample and Hold Amplifier
HA-2420/25	Fast Sample and Hold Amplifier
HA-5320	High Speed Precision Sample and Hold Amplifier
HA-5330	Very High Speed Precision Sample and Hold Amplifier

Comparators

HA-4900/02/05	Quad High Speed Comparators

Control Functions

HV-1000/1000A	Induction Motor Energy Saver

Analog Products

Switches

SPST:

HI-5040	Low ON Resistance SPST Analog Switch

2 x SPST:

HI-200	Dual SPST General Purpose CMOS Analog Switch
HI-300	Dual SPST Precision CMOS Analog Switch
HI-304	Dual SPST Precision CMOS Analog Switch
HI-381	Dual SPST Precision CMOS Analog Switch
HI-5041	Low ON Resistance Dual SPST Analog Switch
HI-5048	Low ON Resistance Dual SPST Switch

4 x SPST:

HI-201	Quad SPST General Purpose CMOS Analog Switch
HI-201HS	Quad SPST High Speed CMOS Analog Switch

SPDT:

HI-301	SPDT Precision CMOS Analog Switch
HI-305	SPDT Precision CMOS Analog Switch
HI-387	SPDT Precision CMOS Analog Switch
HI-5042	Low ON Resistance SPDT Analog Switch
HI-5050	Low ON Resistance SPDT Switch

2 x SPDT:

HI-303	Dual SPDT Precision CMOS Analog Switch
HI-307	Dual SPDT Precision CMOS Analog Switch
HI-390	Dual SPDT Precision CMOS Analog Switch
HI-5043	Low ON Resistance Dual SPDT Analog Switch
HI-5051	Low ON Resistance Dual SPDT Switch

DPST:

HI-5044	Low ON Resistance DPST Analog Switch

2 x DPST:

HI-302	Dual DPST Precision CMOS Analog Switch
HI-306	Dual DPST Precision CMOS Analog Switch
HI-384	Dual DPST Precision CMOS Analog Switch
HI-5045	Low ON Resistance Dual DPST Analog Switch
HI-5049	Low ON Resistance Dual DPST Switch

DPDT:

HI-5046/46A	Low ON Resistance DPDT Analog Switch

4PST:

HI-5047/47A	Low ON Resistance 4PST Analog Switch

Telecommunication Circuits

HC-5502A	SLIC Subscriber Line Interface Circuit
HC-5504	SLIC Subscriber Line Interface Circuit
HC-5508/09	SLICs Subscriber Line Interface Circuit
HC-5510/11	Monolithic CODECs
HC-5512/12A	PCM Monolithic Filter
HC-5512C	PCM or CVSD Monolithic Filter
HC-5512D	PCM Monolithic Filter (-55°C to +125°C)
HC-5552/53/54/57	Monolithic CMOS Serial Interface CODEC/Filter Family
HC-5560 ADVANCE	Transcoder
HC-5572 ADVANCE	2400/1200/600/300 BPS Modem
HC-5580 ADVANCE	Trunk Subscriber Line Interface Circuit (TSLIC)
HC-5581 ADVANCE	DAA Subscriber Line Interface Circuit (DAASLIC)
HC-5590 ADVANCE	Digital Line Transceiver
HC-55536	All-Digital Continuously Variable Slope Delta Demodulator (CVSD)
HC-55564	All-Digital Continuously Variable Slope Delta Modulator/Demodulator (CVSD)
HF-10	Universal Filter

CMOS Digital Products

80C86 Family: CPUs

80C86	Static 16-bit Microprocessor
80C88	Static 8/16-bit Microprocessor

80C86 Family: Peripherals

82C37A	High Performance Programmable DMA Controller
82C50A	Asynchronous Communication Element
82C52	Serial Controller Interface
82C54	Programmable Interval Timer
82C55A	Programmable Peripheral Interface
82C59A	Priority Interrupt Controller
82C82	Octal Latching Bus Driver
82C83H	Octal Latching Inverting Bus Driver
82C84A	Clock Generator Driver
82C85	Static Clock Controller/Generator
82C86H	Octal Bus Transceiver
82C87H	Octal Bus Transceiver (Inverting)
82C88	Bus Controller
82C89	Bus Arbiter

Data Communications

HD-15530	Manchester Encoder-Decoder
HD-15531	Manchester Encoder-Decoder
HD-4702	Programmable Bit Rate Generator
HD-6402	Universal Asynchronous Receiver Transmitter
HD-6406	Programmable Asynchronous Communication Interface
HD-6408	Asynchronous Manchester Adapter
HD-6409	Manchester Encoder-Decoder

CMOS Memory

HM-6504	4K x 1 Synchronous RAM
HM-6508	1K x 1 Synchronous RAM
HM-6514	1K x 4 Synchronous RAM
HM-6516	2K x 8 Synchronous RAM
HM-65162	2K x 8 Asynchronous RAM
HM-6518	1K x 1 Synchronous RAM
HM-65262	16K x 1 Asynchronous RAM
HM-6551	256 x 4 Synchronous RAM
HM-6561	256 x 4 Synchronous RAM
HM-6564	64K Synchronous RAM Module
HM-6616	2K x 8 Fuse Link PROM
HM-6641	512 x 8 Fuse Link PROM
HM-8808A	8K x 8 Asynchronous RAM Module
HM-8808	8K x 8 Asynchronous RAM Module
HM-8816H	16K x 8/32 x 8 Asynchronous RAM Module
HM-92560	256K Synchronous RAM Module
HM-92570	256K Buffered Synchronous RAM Module

CMOS Programmable Logic

HPL-16LC8	Programmable Logic
HPL-16RC4	Programmable Logic
HPL-16RC6	Programmable Logic
HPL-16RC8	Programmable Logic
HPL-82C339	Programmable Chip Select Decoder (PCSD)
HPL-82C338	Programmable Chip Select Decoder (PCSD)
HPL-82C139	Programmable Chip Select Decoder (PCSD)
HPL-82C138	Programmable Chip Select Decoder (PCSD)
Mini-HPL Family	Programmable Logic (16-Pin)

CICD Radiation Hardened Products

Memories

HS-6508RH	1K x 1 CMOS Static RAM (Synchronous)	Rad Hard
HS-6551RH	256 x 4 CMOS Static RAM (Synchronous)	Rad Hard
HS-6504RH	4K x 1 CMOS Static RAM (Synchronous)	Rad Hard
HS-6514RH	1K x 4 CMOS Static RAM (Synchronous)	Rad Hard
HS-6564RH	64K CMOS RAM Module (8K x 8 or 16K x 4)	Rad Hard
HS-65262RH	16K x 1 CMOS Static RAM (Asynchronous)	Rad Hard

80C85 Microprocessor Family

HS-80C85RH	8-Bit CMOS Microprocessor	Rad Hard
HS-81C55RH	256 x 8 CMOS RAM with I/O Ports and Timer	Rad Hard
HS-83C55RH	2K x 8 CMOS ROM with I/O Ports	Rad Hard
HS-54C138RH	3-8-Bit CMOS Decoder	Rad Hard
HS-82C08RH	8-Bit CMOS Bus Transceiver	Rad Hard
HS-82C12RH	8-Bit CMOS Latch	Rad Hard
HS-3374RH	CMOS/TTL Bi-directional Level Shifter	Rad Hard

Multiplexers

HS-508ARH	8 Channel CMOS Analog Multiplexer	Rad Hard
HS-1840RH	16 Channel CMOS Analog Multiplexer	Rad Hard

OP AMPs

HS-3516RH	Wide Band OP AMP	Rad Hard
HS-3530RH	Low Power OP AMP	Rad Hard
HS-5104RH	Quad Low Noise OP AMP	Rad Hard

Analog Switches

HS-302RH	CMOS Analog Switch Dual DPST	Rad Hard
HS-303RH	CMOS Analog Switch Dual SPDT	Rad Hard
HS-306RH	CMOS Analog Switch Dual DPST	Rad Hard
HS-307RH	CMOS Analog Switch Dual SPDT	Rad Hard
HS-384RH	CMOS Analog Switch Dual DPST	Rad Hard
HS-390RH	CMOS Analog Switch Dual SPDT	Rad Hard

Communications

HS-15530RH	CMOS Manchester Encoder/Decoder	Rad Hard
HS-3182	ARINC 429 Bus Interface Line Driver	Rad Hard
HS-3282	CMOS ARINC 429 Bus Interface Circuit	
HS-3273	CMOS MIL-STD-1553 Bus Interface Circuit	
HS-3447	CMOS Data Encription/Decription Device Cypher I™	

Semicustom

HS-G0600RH	CMOS Gate Array 600 Gates	Rad Hard
HS-G1200RH	CMOS Gate Array 1200 Gates	Rad Hard
HS-G2500RH	CMOS Gate Array 2500 Gates	Rad Hard
HS-DXXXXRH	CMOS Standard Cell 2.5 Micron	Rad Hard
HS-CXXXXRH	CMOS Standard Cell 2.5 Micron	Rad Hard

CICD Future Radiation Hardened Products

Memories

HS-65142RH	1K x 4 CMOS Static RAM High Speed (Asynchronous)	Rad Hard
HS-6616RH	2K x 8 CMOS PROM (Synchronous)	Rad Hard

80C86 Microprocessor Family

HS-80C86RH	16-Bit CMOS Microprocessor	Rad Hard
HS-82C37ARH	CMOS DMA Controller	Rad Hard
HS-82C52RH	CMOS Full Duplex UART	Rad Hard
HS-82C54RH	CMOS Programmable Interval Timer	Rad Hard
HS-82C55RH	CMOS Programmable Peripheral Interface	Rad Hard
HS-82C59ARH	CMOS Programmable Interrupt Controller	Rad Hard
HS-82C85RH	CMOS Static Clock Controller/Generator	Rad Hard

Semicustom

HS-G5000RH	CMOS Gate Array 5000 Gates	Rad Hard

Harris Microwave/Gallium Arsenide Products

GaAs FETs

HMF-0300	125 mW GaAs FET — Chip
HMF-0301	125 mW GaAs FET — Packaged
HMF-0302	125 mW GaAs FET — Flange
HMF-0310	High Gain GaAs FET — Chip
HMF-0314	High Gain GaAs FET — Package
HMF-0600	250 mW GaAs FET — Chip
HMF-0602	250 mW GaAs FET — Flange
HMF-0610	High Gain Power GaAs FET — Chip
HMF-0620	High Gain GaAs FET — Chip
HMF-1200	500 mW GaAs FET — Chip
HMF-1202	500 mW GaAs FET — Flange
HMF-2400	1 W GaAs FET — Chip
HMF-2402	1 W GaAs FET — Flange

GaAs Integrated Circuits

HMD-11011-2	Divide by 10/11 Variable Modulus Divider
HMD-11016-1	Divide by 2/4/8 Binary Counter
HMD-11101-2	5-Input NOR/OR Gate
HMD-11104-2	5-Input NAND/AND Gate
HMD-11131-2	Master/Slave D Flip-Flop
HMD-11301-2	Divide by Two Prescaler
HMD-12141-1	Four-Bit Universal Shift Register

IC Evaluation Kits

HMK-11MSI-1	MSI Evaluation Kit
HMK-11SSI-2	SSI Evaluation Kit

GaAs Programs and Services

Monolithic Microwave Integrated Circuits (MMICs)
Custom Analog Integrated Circuits
Custom Digital Integrated Circuits
Semicustom Digital Integrated Circuits
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TWX: 400622

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